A Sub-1.0-V On-Chip CMOS Thermometer With a Folded Temperature Sensor for Low-Power Mobile DRAM

Hyunjoong Lee, *Member, IEEE*, Daeyong Shim, Cyuyeol Rhee, Mino Kim, and Suhwan Kim, *Senior Member, IEEE*

***Abstract*—As Dynamic Random Access Memory (DRAM) supply voltages drop below 1 V with the scaling down of the process, it becomes increasingly difficult to construct a temperature sensor with sufficient accuracy to control self-refresh, without occupying significant area or consuming increased power. In this brief, we propose an on-chip CMOS thermometer with a temperature sensor, the output of which is divided into segments by a folding scheme. The slopes of these segments can be arranged to be the same or adjusted separately, as desired for the output. Implemented in a 29-nm DRAM process, the sensor operates from −40 °C to 95 °C at the supply voltage of 0.8 V, with a temperature sensitivity of −3.1 mV/°C between −40 °C and 35 °C, and −2.1 mV/°C between 35 °C and 95 °C. It has an area of 0.0016 mm^2 and consumes less than 0.144 μW.**

***Index Terms*—Folding, low voltage, mobile DRAM, self-refresh, temperature sensor, thermometer.**

I. Introduction

As high-end smartphones and tablets become smaller and thinner, thermal and power management in mobile DRAMs becomes challenging issues in deep submicron circuit design. Temperature-based self-refresh period control, often called auto temperature-compensated self-refresh, is one possible approach to temperature-dependent power management. An on-chip thermometer with a temperature sensor can be used to measure the temperature of the chip, and then, the longest refresh period which will ensure that the chip loses no data is chosen [1], [2].

In the standard CMOS process, temperature sensors can readily be realized using Bipolar Junction Transistors (BJTs) or MOSFETs. An on-chip thermometer constructed from one of these conventional CMOS temperature sensors, together with an Analog-to-Digital Converter (ADC), provides very adequate performance [3]–[5]. However, obtaining an accurate digital output from the small analog signal produced by such a sensor requires a complicated high-resolution ADC, which can be expected to draw a lot of power or to require a large chip area to compensate for the process variations of CMOS. Furthermore, to be accurate, a thermometer of this sort requires calibration at one or more known temperatures, which adds significant cost.

Aside from these conventional approaches, many research works have been done on temperature sensors based on concepts of measuring the temperature dependence on the time domain. They mostly rely on the temperature-dependent propagation delay of a chain of inverters and a time-to-digital converter [6]–[12]. As evolutions of this concept, various all-digital CMOS temperature sensors have also been developed, and some of them are aimed at the thermal monitoring of a microprocessor or a DRAM [10], [11]. The performance of these sensors is comparable to that of conventional CMOS temperature sensors with better efficiency. However, time-domain circuitry still consumes a considerable area or power and requires a costly calibration process to mitigate the susceptibility to process variation.

While the temperature sensors in both categories described earlier provide accurate measurements of every temperature in the operating range, a thermometer for use in the self-refresh control of DRAM only requires the detection of specific temperatures with respect to a fixed set of reference temperatures [1], [13]. Considering the high density of DRAM, it is also preferred to have a small circuit area, a relatively low power consumption, and a low-cost calibration method, even at some cost in accuracy. With these requirements, an alternative type of thermometer, with a temperature sensor that only requires two NMOS transistors together with n+ active resistors, has recently been proposed [13]. It is area efficient and tolerant of process variations and aging issues such as negative bias temperature instability while experimentally achieving good linearity and high sensitivity between 35 °C and 105 °C. The thermometer successfully addresses calibration, area, and power consumption issues, making it highly suitable for DRAM applications.

Nevertheless, the continuing scaling down of the DRAM process is reducing supply voltages below 1 V, so the design of on-chip thermometers remains challenging; with the reduced supply voltage, the resolution and linearity of the sensor around room temperature become insufficient [13], resulting in a suboptimal refresh rate which may cause either a malfunction or an excessive power consumption. Some of the aforementioned temperature sensors, including all-digital-type ones, operate around or well below 1 V [5], [8], [11], but it is still overkill to

Manuscript received August 13, 2015; revised October 27, 2015; accepted December 13, 2015. Date of publication February 16, 2016; date of current version May 25, 2016. This work was supported in part by the Information Technology (IT) Research and Development program of Ministry of Trade, Industry and Energy (MOTIE)/Korea Evaluation Institute of Industrial Technology (KEIT) (10044497, Development of (Bipolar, CMOS and Double-diffused MOS (DMOS) (BCDMOS)) Technology Process and IPs based on AEC-Q100 for Automotive Applications; 10048843, Automotive Electronic Control Unit (ECU), System on Chip (SoC) and Embedded Software (SW) for Multidomain Integration) and in part by SK Hynix. This brief was recommended by Associate Editor E. Bonizzoni.

H. Lee is with the Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-744, South Korea, and also with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada.

D. Shim is with the SK Hynix, Icheon 467-701, South Korea.

C. Rhee, M. Kim, and S. Kim are with the Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-744, South Korea (e-mail: suhwan@snu.ac.kr).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2016.2530803

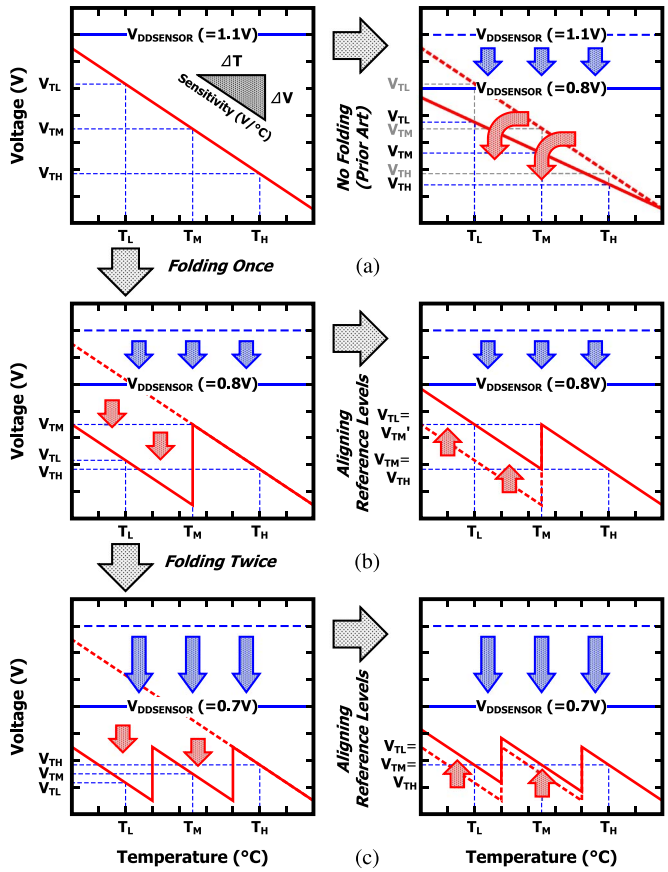

Fig. 1. Explanation of our folding schemes. (a) Output voltage of a temperature sensor without folding scheme [13] at $V_{\mathrm{DDSENSOR}} = 1.1$ V (left) and 0.8 V (right). Output voltage from a scheme (b) with one fold at $V_{\mathrm{DDSENSOR}} = 0.8$ V and (c) with two folds at $V_{\mathrm{DDSENSOR}} = 0.7$ V.

have accurate measurements of every temperature, at the cost of area or power. Considering realistic constraints such as the turnaround time for the design, area occupied in the DRAM chip, and quick applicability to next technology nodes, it can be a good choice to improve the scheme proven by the previous successful product [13].

These considerations motivated us to design an on-chip CMOS thermometer with a folded temperature sensor, specifically designed for refresh control in the mobile DRAM operating with a supply of less than 1 V. The resulting circuits exhibit a near linear response between -40 °C and 95 °C.

The remainder of this brief is organized as follows. In Section II, the concept of the folded temperature sensor circuit is explained and compared with our previous work. In Section III, the architecture and the operation of the thermometer are described. In Section IV, we present experimental results, and this brief is summarized in Section V.

II. Folded Temperature Sensor Circuit

A. Folding Scheme

The temperature sensor circuit by Shim *et al.* achieves good linearity and high sensitivity over a wide temperature range without requiring NMOS, PMOS, and BJTs to be mixed in the same circuit [13]. Its output characteristic is the left graph of Fig. 1(a), whose V_{TL}, V_{TM}, and V_{TH} are the reference levels used as thresholds for detecting temperatures T_L, T_M, and T_H for example purposes; these reference levels are easily generated by a resistor ladder, using the same supply voltage as the sensor, which is V_{DDSENSOR}. As long as the highest reference level, V_{TL} in Fig. 1(a), is below the supply voltage, a good sensitivity can easily be achieved within a reasonable temperature range. However, the right graph in Fig. 1(a) shows how the maximum sensitivity of the sensor is inevitably limited by the supply voltage, and this sensitivity is continually declining as the technology shrinks. Furthermore, reducing the supply voltage narrows the gap between the two reference levels, so a resistor ladder of higher precision soon becomes necessary.

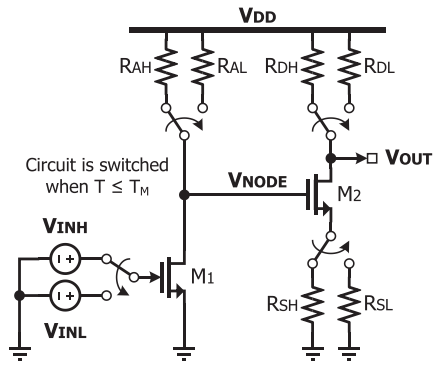

Fig. 2. Circuit for a temperature sensor with one fold. The second subscript L indicates the low subrange ($T \leq T_M$), and H indicates the high subrange ($T > T_M$).

Fig. 1(b) and (c) describes the folding scheme which we use to solve this problem. The left graph in Fig. 1(b) shows how the output voltage of the sensor is folded at T_M to compensate for the reduced supply voltage. Although the ramping of the output voltage is now separated into two segments, it is possible to arrange that the slope of the segments remains the same. Therefore, this scheme can maintain the sensitivity and the linearity of the equivalent unfolded sensor, at a reduced supply voltage. A further reduction in the supply voltage may be accommodated by folding the sensor twice, as shown in the left graph in Fig. 1(c).

Meanwhile, the slope or the level of each segment can also be adjusted separately. By arranging the slope of each segment to be different, we can fine-tune the balance between the sensitivity and the detectable temperature range separately for each segment.

By shifting the level of each segment and aligning reference levels additionally, we can simplify the peripheral circuits that generate the reference levels and compare them with the output voltage: Appropriate levels are aligned by shifting the level of each segment of the folded curve. The aligned reference levels required for a single fold and for two folds are shown in the right graphs of Fig. 1(b) and (c), respectively; the latter is an extreme case, in which all the reference levels for T_L, T_M, and T_H are aligned to a single reference voltage. Reducing the number of reference levels relaxes the precision required from the resistor ladder.

B. Analysis of the Folded Temperature Sensor Circuit

A temperature sensor circuit that uses the folding scheme with one fold is shown in Fig. 2; the folding scheme is implemented by changing the values of resistors or adjusting the bias voltage of transistors. The circuit consists of two parts: The

n+ active resistor R_A and the NMOS transistor M_1 operating in its deep triode region form a temperature-dependent voltage divider that generates a voltage $V_{\rm NODE}$, which is proportional to absolute temperature, and the NMOS transistor M_2 operating in its saturation region and the n+ active resistors R_D and R_S form a common source amplifier with source degeneration that linearly amplifies $V_{\rm NODE}$ to $V_{\rm OUT}$, which is complementary to absolute temperature. The switching capability between two sets of the resistors and the voltage $V_{\rm IN}$ to bias M_1 is now added to perform the folding scheme. The characteristics of all the resistors and transistors are temperature dependent; the transconductance parameter β, the threshold voltage $V_{\rm TH}$, and the resistance R can be expressed in terms of temperature as follows [14]:

$$\begin{aligned}\beta(T) &= \beta_0\left(\frac{T}{T_0}\right)^{-m}\\ V_{\rm TH}(T) &= V_{\rm TH0} - \alpha_{\rm VTH}(T-T_0)\\ R(T) &= R_0\left[1+\alpha_R(T-T_0)\right]\end{aligned} \tag{1}$$

where $\beta_0 = \mu_{N0}C_{\rm OX}(W/L)$, T is the temperature being measured, T_0 is the reference temperature, μ_{N0} is the mobility at T_0, $C_{\rm OX}$ is the gate capacitance, and W/L is the device dimension.

Based on the linearized expressions of $V_{\rm NODE}$ and $V_{\rm OUT}$ from our previous study [13], implementing the capability to switch between two settings gives us expressions for $V_{\rm NODE}$ and $V_{\rm OUT}$ in each temperature range as follows:

$$V_{\rm NODE}(T) \simeq \begin{cases} M_H(T-T_0)+N_H, & T > T_M \\ M_L(T-T_0)+N_L, & T \le T_M \end{cases} \tag{2}$$

$$V_{\rm OUT}(T) \simeq \begin{cases} U_H(T-T_0)+W_H, & T > T_M \\ U_L(T-T_0)+W_L, & T \le T_M \end{cases} \tag{3}$$

where the expression of $V_{\rm OUT}$ for each temperature range in (3) is a function of $V_{\rm NODE}$ as follows:

$$V_{\rm OUT}(T) \simeq V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[V_{\rm NODE}(T) + P(T-T_0) + Q\right]. \tag{4}$$

The subscripts H and L correspond to the subranges $T > T_M$ and $T \le T_M$, and the subscript 0 in the resistances denotes values evaluated at T_0. Assuming that the device dimensions and other characteristics of M_1 and M_2 are predetermined, temperature-dependent expressions for the coefficients M, N, P, Q, U, and W in each temperature range depend on the corresponding values of R_A, R_D, R_S, and $V_{\rm IN}$ as follows:

$$\begin{aligned} M &= \alpha_{\rm VTH1} + f(V_{\rm IN}, R_{A0})\\ N &= V_{\rm IN} - V_{\rm TH10} + g(V_{\rm IN}, R_{A0})\\ P &= \alpha_{\rm VTH2} + h(V_{\rm NODE}, R_{S0})\\ Q &= -V_{\rm TH20} + k(V_{\rm NODE}, R_{S0})\\ U &= -\frac{R_{D0}}{R_{S0}}(M+P)\\ &= -\frac{R_{D0}}{R_{S0}}(\alpha_{\rm VTH1}+\alpha_{\rm VTH2}+f+h)\\ W &= V_{\rm DD} - \frac{R_{D0}}{R_{S0}}(N+Q)\\ &= V_{\rm DD} - \frac{R_{D0}}{R_{S0}}\left[V_{\rm IN} - (V_{\rm TH10}+V_{\rm TH20}) + g + k\right] \end{aligned} \tag{5}$$

TABLE I
SIGNS OF THE PARTIAL DERIVATIVES OF M, N, U, AND W

	∂M	∂N	∂U	∂W
$\partial V_{\rm IN}$	+	−	−	++*
$\partial R_{\rm A0}$	−	−	+	++*
$\partial V_{\rm NODE}$	·	·	+	−
$\partial R_{\rm D0}$	·	·	−−*	−
$\partial R_{\rm S0}$	·	·	++*	+

*Double signs indicate that the corresponding controllable value has a more significant effect than those corresponding to single signs.

where the subscripts 1 and 2 signify that their associated values are properties of M_1 and M_2 and the subscript 0 denotes values evaluated at T_0.

To allow the temperature sensor to fold its output voltage following (2) and (3), the coefficients W, which depend on N and Q, need to be correctly chosen and switched between W_H and W_L, while the coefficients U, which depend on M and P, should ideally remain the same in each temperature subrange, so as not to affect the temperature sensitivity, regardless of switching between W_H and W_L.

The previously proposed temperature sensor, which operates at a higher supply voltage without a folding scheme, shifts the output voltage by changing W. In this case, the trailing terms $f+h$ and $g+k$ in U and W may be ignored on the basis that they have only a small effect on the controllable parameters $V_{\rm IN}$, R_{A0}, and R_{S0} [13]. However, we cannot ignore these terms because our folding scheme has to cope with a lower supply voltage, and W must be switched between two or more significantly different values, which affects U substantially. Therefore, we need to examine the partial derivatives of M, N, U, and W with respect to $V_{\rm IN}$, R_{A0}, $V_{\rm NODE}$, R_{D0}, and R_{S0}. The derivatives are expressed in terms of the partial derivatives of f, g, h, and k.

From the derivatives of M, N, U, and W, we can determine the direction in which the controllable values should be adjusted when the output of the temperature sensor is folded. Although the derivatives have complicated dependence on the controllable values and on the operating temperature, we can obtain their signs within the operating ranges of the controllable values and temperature. These signs are presented in Table I. As can be inferred from the table, switching R_A or $V_{\rm IN}$ can mainly shift the level of the output voltage, and then, switching R_D and R_S can compensate for the slight change in the slope.

III. ARCHITECTURE AND OPERATION OF THE THERMOMETER

The thermometer is composed of a folded temperature sensor, a resistor ladder, seven 32 : 1 selectors, a voltage regulator, a comparator, six latches, a temperature sensor controller, a fold controller, and a controller for fuse and test modes, all shown in Fig. 3(a). The operation of the thermometer is similar to that of our previous one [13], except some details to implement the folding scheme. The resistor ladder generates seven reference voltages corresponding to designated temperatures. Some of the reference voltages are arranged to have the same value before

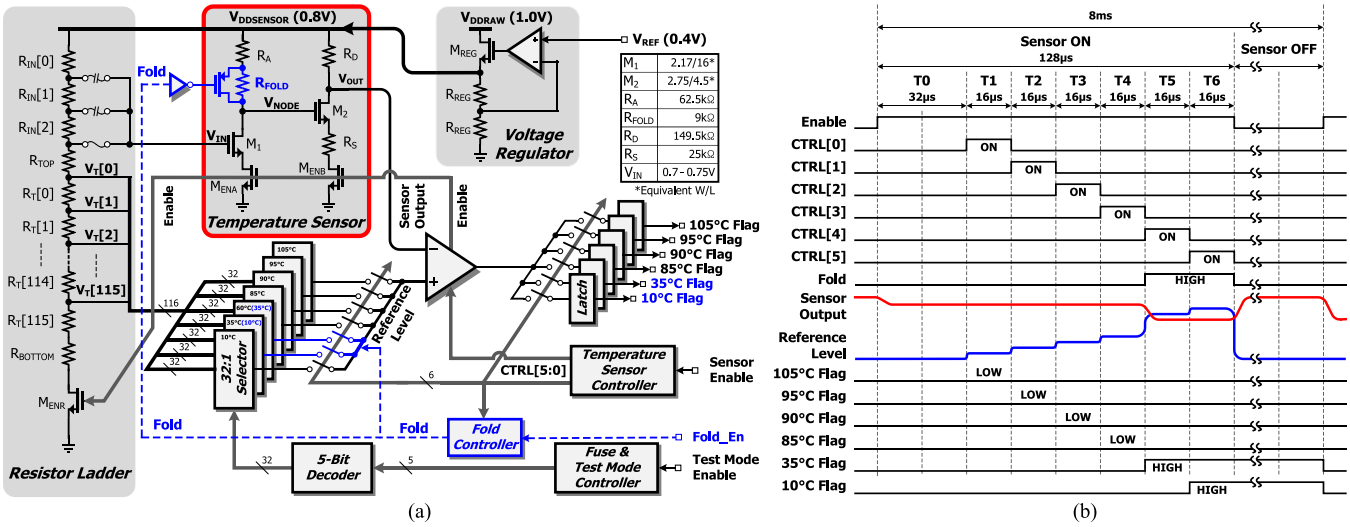

Fig. 3. Folded on-chip thermometer. (a) Block diagram of the thermometer and (b) the timing diagram of the signals of the thermometer, operating at a temperature between 35 °C and 85 °C.

and after the folding, as described in Section II-A. The lowest voltage among the seven reference voltages is only for testing purposes. The temperature sensor controller sequentially selects each reference voltage for comparison with the sensor output. Then, the comparator compares the sensor output and the selected reference voltage and generates an output flag. The fold controller modifies the sensor output at temperatures below 35 °C to achieve folding; R_{FOLD} is bypassed by turning on the FOLD signal to reduce the effective value of R_A. The other elements R_D, R_S, and V_{IN} are not changed here since the slight deviation between the two slopes does not need to be compensated considering the accuracy required in this implementation. The voltage regulator receives a temperature-independent bandgap reference voltage of 0.4 V from the main DRAM block and maintains the corresponding thermometer bias voltage of 0.8 V, isolated from the supply noise. The fuse and test mode controller allows the seven reference levels to be trimmed for one-point calibration.

Fig. 3(b) depicts the temperature readout procedure that takes place in the thermometer when it is operating at a temperature between 35 °C and 85 °C. The thermometer is turned on for 128 μs in every 8-ms cycle. As the Enable signal goes high, there is an initial setup period $T0$, during which all the analog blocks are powered on and the signals settle. Then, temperature measurement starts. The FOLD signal is on at the periods of $T5$ and $T6$. During the six periods from $T1$ to $T6$, the sensor output is compared to a reference voltage selected from the six predetermined levels by means of the switch control signals *CTRL*[5 : 0]. The temperature sensor controller sequentially selects each of the reference voltages for comparison with the sensor output. The results of these comparisons are latched to set one of six temperature flags. These flags are routed to the DRAM controller to set the appropriate refresh period. Assuming that the temperature does not change abruptly, there is negligible variation in output voltage and no noticeable two-state hysteresis near 35 °C, over the whole 128-μs sensing time in every 8-ms cycle. During the remaining time of the cycle, the temperature sensor and the other analog circuits in the thermometer are turned off to reduce any static power consumption.

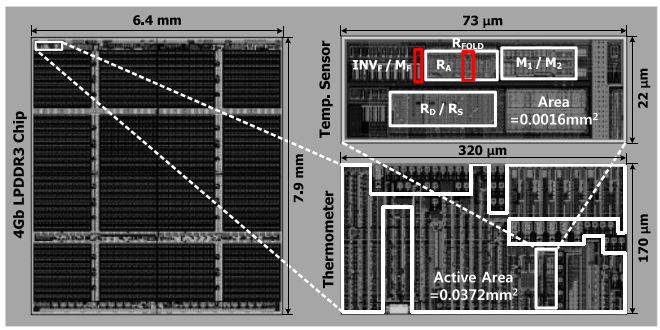

Fig. 4. Microphotograph of a 4-Gb LPDDR3 mobile DRAM chip, with magnified layouts of the thermometer and temperature sensor.

IV. Experimental Results

A microphotograph of a 4-Gb LPDDR3 mobile DRAM chip (fabricated in a 29-nm DRAM process), together with magnified layouts of the thermometer and temperature sensor, is shown in Fig. 4. The sensor has an area of 0.0016 mm^2, and on average, it consumes less than 0.144 μW at 0.8 V.

Fig. 5 shows the thermometer outputs and their errors measured over 107 samples. The improved linearity of the folded design permits one-point calibration, after which the errors in 107 sample circuits with a 0.8-V supply ranged from -4.31 °C to $+3.82$ °C. Since the deviation in the self-refresh period at higher temperature should be minimized among the chips to avoid any significant yield loss in mass production, the target temperature for the calibration is chosen to be at 95 °C.

The overall performance of the sensor is summarized in Table II. As can be seen from the magnified view in Fig. 4, the areal overhead of the additional circuitry to enable the folding scheme is almost negligible. The temperature sensitivity of the

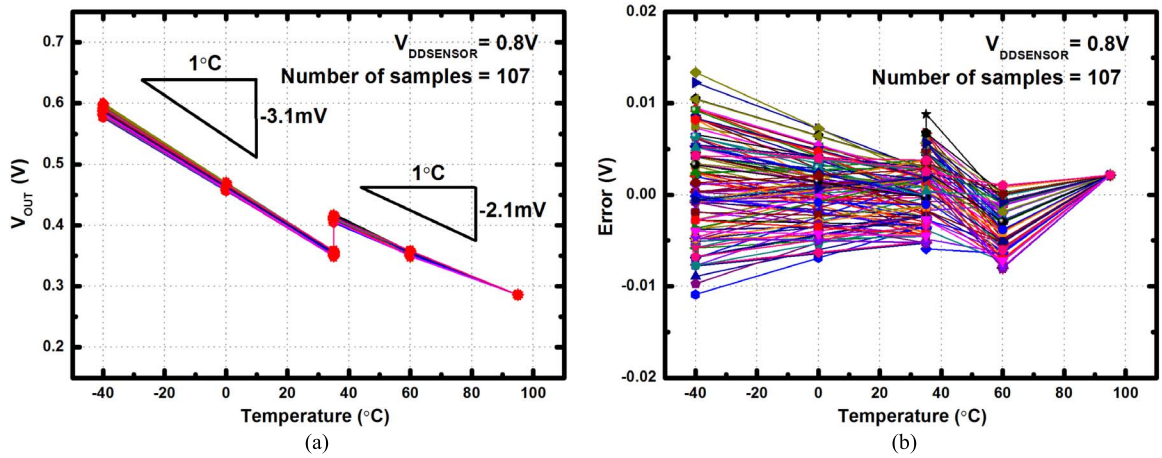

Fig. 5. Measured results of the thermometer. (a) Output and (b) the error voltages.

TABLE II
PERFORMANCE SUMMARY OF THE THERMOMETER AND SENSOR FABRICATED IN A 29-nm DRAM PROCESS

Process technology	29nm DRAM
Operating range	−40°C − 95°C
$V_{DDSENSOR}$ (supply voltage)	0.8V (V_{DDRAW} = 1.0V)
Temperature sensitivity (−40°C − 95°C)	−3.1mV/°C (−40°C − 35°C)
	−2.1mV/°C (35°C − 95°C)
Resolution (with a 4.5mV step)	1.45°C (−40°C − 35°C)
	2.14°C (35°C − 95°C)
Calibration (−40°C − 95°C)	One-point (@ 95°C)
Max. inaccuracy (°C) (107 samples after calibration)	−4.31 − +3.51 (−40°C − 35°C)
	−4.20 − +3.82 (35°C − 95°C)
Temperature sensor area	0.0016mm^2 (73μm x 22μm)
Average power dissipation (sensor)	0.144μW (@ 0.8V)

sensor is −3.1 mV/°C at 0.8 V over the range of −40 °C to 35 °C. Its resolution is 1.45 °C, which is only limited by the 4.5-mV steps of the resistor ladder. These results suggest that the proposed sensor is sufficiently accurate, even with one-point calibration, for refresh control in ultralow-power DRAM, and its power requirements are also low enough for this application.

V. CONCLUSION

We have presented an on-chip CMOS thermometer with a folded temperature sensor with sufficient resolution and linearity for temperature measurement in low-power mobile DRAM, operating with a supply of less than 1 V. We describe how to design a folded temperature sensor of this type and present an analysis which facilitates the design process of the folding scheme. We validated our thermometer in a 29-nm DRAM process and demonstrated that its accuracy, linearity, and power efficiency are suitable for refresh control in ultralow-power DRAM.

REFERENCES

[1] J. P. Kim, W. Yang, and H.-Y. Tan, "A low-power 256-Mb SDRAM with an on-chip thermometer and biased reference line sensing scheme," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 329–337, Feb. 2003.

[2] Y. Kagenishi *et al.*, "Low power self refresh mode DRAM with temperature detecting circuit," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, 1993, pp. 43–44.

[3] A. Bakker and J. H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 933–937, Jul. 1996.

[4] S. H. Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A micropower battery current sensor with ±0.03% (3σ) inaccuracy from −40 to +85 °C," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 386–387.

[5] K. Souri, Y. Chae, F. Thus, and K. A. A. Makinwa, "A 0.85 V, 600 nW all-CMOS temperature sensor with an inaccuracy of ±0.4 °C (3σ) from −40 to 125 °C," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 222–223.

[6] E. Saneyoshi, K. Nose, M. Kajita, and M. Mizuno, "A 1.1 V 35 μm × 35 μm thermal sensor with supply voltage sensitivity of 2 °C/10%-supply for thermal management on the SX-9 supercomputer," in *Proc. IEEE Symp. VLSI Circuits*, 2008, pp. 152–153.

[7] C.-C. Chen and H.-W. Chen, "A low-cost CMOS smart temperature sensor using a thermal-sensing and pulse-shrinking delay line," *IEEE J. Sens.*, vol. 14, no. 1, pp. 278–284, Jan. 2014.

[8] S. Hwang, J. Koo, K. Kim, H. Lee, and C. Kim, "A 0.008 mm^2 500 μW 469 kS/s frequency-to-digital converter based CMOS temperature sensor with process variation compensation," *IEEE Trans. IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 9, pp. 2241–2248, Sep. 2013.

[9] S. Jeong *et al.*, "A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, Aug. 2014.

[10] D. Ha *et al.*, "Time-domain CMOS temperature sensors with dual delay-locked loops for microprocessor thermal monitoring," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 9, pp. 1590–1601, Sep. 2012.

[11] C.-C. Chung and C.-R. Yang, "An autocalibrated all-digital temperature sensor for on-chip thermal monitoring," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 2, pp. 105–109, Feb. 2011.

[12] P. Chen, S.-C. Chen, Y.-S. Shen, and Y.-J. Peng, "All-digital time-domain smart temperature sensor with an inter-batch inaccuracy of −0.7 °C − +0.6 °C after one-point calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 913–920, May 2011.

[13] D. Shim *et al.*, "A process-variation-tolerant on-chip CMOS thermometer for auto temperature compensated self-refresh of low-power mobile DRAM," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2550–2557, Oct. 2013.

[14] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 48, no. 7, pp. 876–884, Jul. 2001.