A Low-Cost and Low-Power Time-to-Digital Converter Using Triple-Slope Time Stretching

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***Abstract*—In this brief, we present a time-to-digital converter (TDC) in which a single interpolator is used to improve the resolution by time stretching. The interpolator is based on a triple-slope conversion. Without slowing down the measured event, this approach extensively reduces the chip area and the corresponding power consumption, as compared with the prior arts with two parallel time interpolators. A prototype was designed and fabricated in a 0.35-μm CMOS digital process, and its core area merely occupies 0.126 mm^2. Measurements show that our TDC achieves a resolution of 357 ps while consuming 1.22 mW with a 2.5-V supply. The dynamic range of the TDC exceeds 1.46 μs. The measurement rate can achieve above 400 kS/s.**

***Index Terms*—Dual-slope conversion, interpolator, time stretcher, time-to-digital converter (TDC).**

I. Introduction

TIME-TO-DIGITAL converters (TDCs) are widely used in various industrial applications, including all-digital phase-locked loops, laser range finders, on-chip time-signal measurement, and biochemical sensor readout [1]. The interval between asynchronous timing signals can be measured analogically, digitally, or using an interpolating method. The analog method is usually based on the measurement of the voltage changes in a capacitor that is (dis)charged by a constant current over the time interval. The precision of the analog ones is excellent, but it suffers from poor stability and linearity; thus, its measurement range is usually short. The digital method is based on synchronous counting clock cycles of a reference oscillator. It is linear over a wide measurement range, but its precision is limited by the uncertainty attached to ± 1 clock cycle. A higher resolution can be obtained by raising the clock frequency, but more power is consumed.

The clock-cycle uncertainty can be improved by interpolating time signals within the reference clock period. This improves the measurement resolution and reduces the need for a very high frequency reference oscillator, resulting in a low-power consumption. A TDC based on analog interpolation (or dual-slope time stretching) was first suggested by Turko [2] to achieve an accurate precision and reduce the power consumptions. Many modifications have been introduced [3]–[5]. At least two parallel dual-slope time stretchers are commonly required for stretching the time fractions at both ends of each measured time interval. The cost, the space, and the power consumption of the interpolator itself are particularly important parameters [6].

To extensively reduce the chip area and the corresponding power consumption of prior arts, a novel approach is proposed in this brief to unify two parallel dual-slope time stretchers without sacrificing the rate of the measured events.

The remainder of this brief is organized as follows. In Section II, we explain the structure and the operational principles of a conventional TDC based on time stretching. In Section III, we introduce our unified dual-slope (or triple-slope) time-stretcher TDC. The measurements conducted with the prototype of our fabricated TDC are presented in Section IV. Section V summarizes the results of this work.

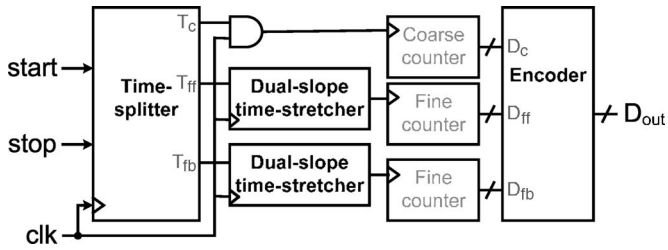

Fig. 1. Block diagram of the dual-slope time-stretcher-based TDC.

II. Dual-Slope Time-Stretcher-Based TDC

The operating principle and the block diagram of the TDC based on the dual-slope time stretching technique are shown in Fig. 1. It consists of a time splitter, a coarse counter, two parallel interpolators (or two parallel dual-slope time stretchers), two fine counters, and an encoder. In [6], two parallel dual-slope time stretchers themselves occupy more than 80% of the TDC. The asynchronous events to be timed are the rising edges of the start and stop signals, and the interval between them is divided into three parts by the time splitter, as shown in Fig. 2. The synchronized part of the interval is the coarse time T_c, and the residual parts are the front fine time $T_{\rm ff}$ and the back fine time $T_{\rm fb}$.

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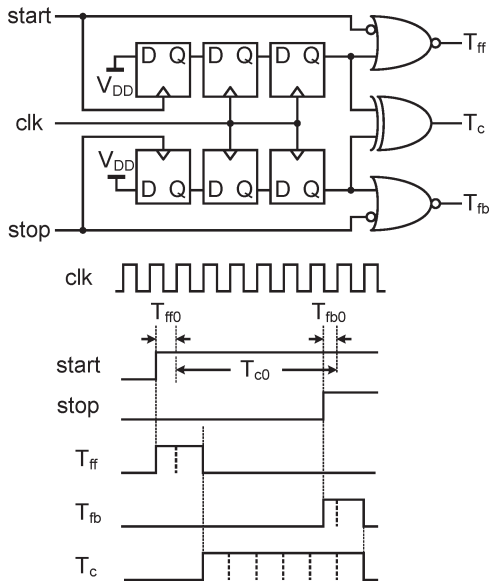

Fig. 2. Time-splitter and timing diagrams for a dual-slope time-stretcher-based TDC.

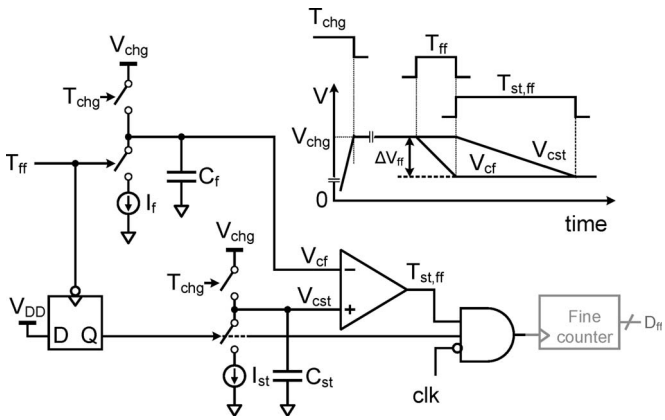

Fig. 3. Block diagram of a single dual-slope time stretcher and its timing diagram ($T_{\rm ff}$).

The coarse time T_c is measured by a simple counter, and the fine times $T_{\rm ff}$ and $T_{\rm fb}$ are passed to dual-slope time stretchers so as to achieve a resolution that is finer than the period of the reference clock. To guarantee proper time measurements in the dual-slope conversion, two identical time stretchers are required. The length of each fine time, which may be either the front fine time $T_{\rm ff}$ or the back fine time $T_{\rm fb}$, is amplified by the stretching factor of its own dual-slope time stretcher, which has the structure shown in Fig. 3. This factor is determined by the ratio between currents I_f and $I_{\rm st}$ multiplied by the ratio between capacitances C_f and $C_{\rm st}$. Initially, both capacitors are charged up to the precharging voltage level $V_{\rm chg}$. When the fine time $T_{\rm ff}$ (or $T_{\rm fb}$) begins, the fine capacitor C_f at the input of the dual-slope time stretcher begins to discharge. After time $T_{\rm ff}$ (or $T_{\rm fb}$), the voltage across the fine capacitor $V_{\rm cf}$ becomes $\Delta V_{\rm ff}$ (or $\Delta V_{\rm fb}$) less than the precharge voltage $V_{\rm chg}$. As soon as the fine time $T_{\rm ff}$ (or $T_{\rm fb}$) finishes, the stretching capacitor $C_{\rm st}$ begins to discharge, and the stretched time $T_{\rm st,ff}$ (or $T_{\rm st,fb}$) begins. It ends when voltage $V_{\rm cst}$ across the stretching capacitor is equal to $V_{\rm chg} - \Delta V_{\rm ff}$ (or $\Delta V_{\rm fb}$), which is the voltage across the fine

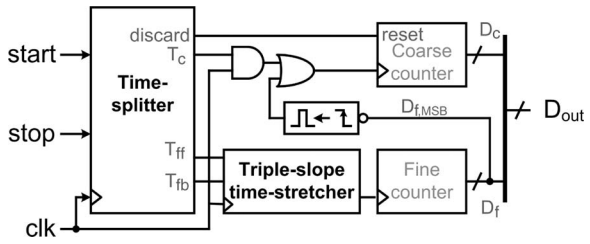

Fig. 4. Block diagram of a TDC utilizing a triple-slope time stretcher.

capacitor. The stretched time $T_{\rm st}$ depends on the fine time $T_{\rm ff}$ (or $T_{\rm fb}$), the values of the capacitors, and the current sources as follows:

$$T_{\rm st,ff} = \frac{C_{\rm st}}{I_{\rm st}}\Delta V_{\rm ff} = \frac{C_{\rm st}}{C_f}\frac{I_f}{I_{\rm st}}T_{\rm ff} = MNT_{\rm ff}$$
$$T_{\rm st,fb} = \frac{C_{\rm st}}{I_{\rm st}}\Delta V_{\rm fb} = \frac{C_{\rm st}}{C_f}\frac{I_f}{I_{\rm st}}T_{\rm fb} = MNT_{\rm fb} \quad (1)$$

where $C_{\rm st} = MC_f$ and $I_{\rm st} = I_f/N$.

Three separate counters in the TDC measure the coarse time, the stretched front fine time, and the stretched back fine time. Each counter produces a digital code, i.e., D_c is the coarse data, $D_{\rm ff}$ is the stretched front fine data, and $D_{\rm fb}$ is the stretched back fine data. These outputs are combined as follows by a digital encoder:

$$D_{\rm out} = 2^L D_C + (D_{\rm ff} - D_{\rm fb}) \quad (2)$$

where L is the number of bits used to represent each of the fine times, which can be expressed as

$$L = \log_2 MN = \log_2\left(\frac{C_{\rm st}}{C_f}\frac{I_f}{I_{\rm st}}\right). \quad (3)$$

III. Triple-Slope Time-Stretcher-Based TDC

Compared with a TDC with a single counter, a TDC with two parallel dual-slope time stretchers has a lower power consumption for the same resolution. However, it requires a coarse counter and two dual-slope time stretchers, each of which has a pair of capacitors, a comparator, and a fine counter. These occupy a relatively large area of silicon, which is mainly taken up by the time stretchers and the corresponding fine counters. Our triple-slope time-stretcher-based TDC, shown in Fig. 4, requires less area because it only needs a coarse counter, a single triple-slope time stretcher, and a fine counter. In addition, the triple-slope time stretcher provides a single fine digital output D_f, while the two fine outputs $D_{\rm ff}$ and $D_{\rm fb}$ in Fig. 1 need to be arithmetically encoded. Compared with the dual-slope design, our design effectively eliminates one of the two time stretchers, a fine counter, and an encoder. Overall, our new TDC can achieve a maximum of 40% reduction in the core size even if the area of a single dual-slope time stretcher is approximately similar to or slightly less than that of our triple-slope time stretcher. Considering that the number of comparators, capacitors, and fine counters in the time-stretcher part has been cut by half, the power requirement is also significantly mitigated by a similar percentage comparable with that of the area reduction.

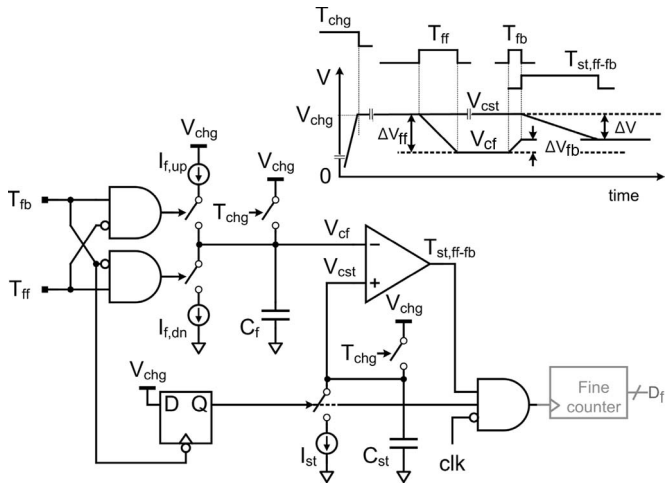

Fig. 5. Block diagram of a triple-slope time stretcher and its timing diagram $(T_{\rm ff} - T_{\rm fb})$.

From the timing diagram in Fig. 5, the total charge needed to precharge $C_{\rm st}$ and C_f for a triple-slope time stretcher's single cycle of operation can be expressed as

$$Q_{\rm precharge,triple} = C_{\rm st}(\Delta V_{\rm ff} - \Delta V_{\rm fb}) + C_f \Delta V_{\rm ff} \qquad (4)$$

where $\Delta V_{\rm ff}$ is drop-off in the voltage as C_f is discharged during $T_{\rm ff}$ and $\Delta V_{\rm fb}$ is the pickup in the voltage as C_f is charged during $T_{\rm fb}$. In comparison with the proposed time stretcher, the dual-slope time-stretcher-based TDC uses two dual-slope time stretchers. With the same run-down currents, the capacitors would need to be precharged by an amount of $\Delta V_{\rm ff}$ and $\Delta V_{\rm fb}$; thus, the total charge would be

$$Q_{\rm precharge,dual} = \underbrace{(C_{\rm st} + C_f)\Delta V_{\rm ff}}_{\text{stretcher for } T_{\rm ff}} + \underbrace{(C_{\rm st} + C_f)\Delta V_{\rm fb}}_{\text{stretcher for } T_{\rm fb}}. \qquad (5)$$

The triple-slope time stretcher is area efficient because it stretches the front fine time $T_{\rm ff}$ and the back fine time $T_{\rm fb}$ sharing the same part of the circuit, which has the structure shown in Fig. 5. The fine capacitor C_f and the stretching capacitor $C_{\rm st}$ are precharged to $V_{\rm chg}$. For the duration of the front fine time $T_{\rm ff}$, the fine capacitor C_f is discharged by a down-charge pump with current $I_{f,\rm dn}$. Then, voltage $V_{\rm cf}$ across the fine capacitor reaches a certain value. For the duration of the back fine time $T_{\rm fb}$, the fine capacitor C_f is charged up by an up-charge pump with current $I_{f,\rm up}$. These charge pumps maintain the voltage across the fine capacitor C_f within $\Delta V (= \Delta V_{\rm ff} - \Delta V_{fb})$ of $V_{\rm chg}$.

Unlike that of the dual-slope time stretcher, the stretched time $T_{\rm st,ff-fb}$ of our triple-slope time stretcher depends on the time difference between $T_{\rm ff}$ and $T_{\rm fb}$, the values of the capacitors, and the current sources as follows:

$$T_{\rm st,ff-fb} = \frac{C_{\rm st}}{I_{\rm st}}\Delta V = \frac{C_{\rm st}}{C_f} \cdot \frac{I_f}{I_{\rm st}}(T_{\rm ff} - T_{\rm fb}) = MN(T_{\rm ff} - T_{\rm fb}) \qquad (6)$$

where $C_{\rm st} = MC_f$ and $I_{\rm st} = I_f/N$.

However, this equation allows the stretched time $T_{\rm st,ff-fb}$ to be negative if the front fine time $T_{\rm ff}$ is smaller than the back fine time $T_{\rm fb}$. It would have to be dealt with by polarity-distinction

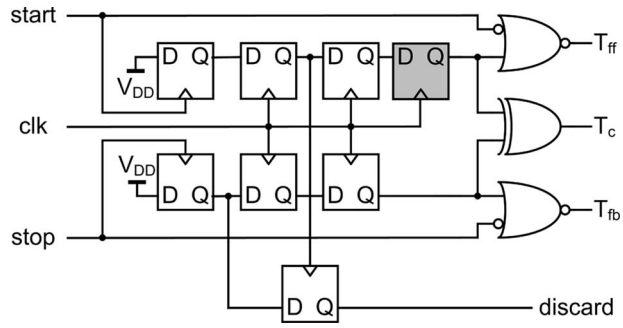

Fig. 6. Time splitter in a triple-slope time-stretcher TDC.

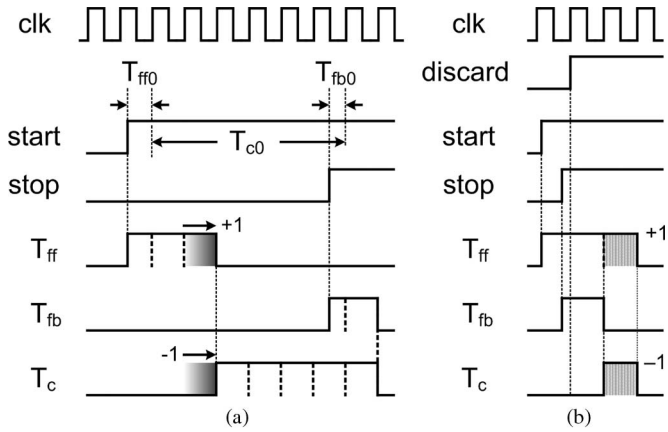

Fig. 7. Timing diagrams for (a) time borrowing and (b) the exceptional case.

logic, and also, it makes ΔV negative. This problem can be solved by a time borrowing scheme, which guarantees that the front fine time $T_{\rm ff}$ is always greater than the back fine time $T_{\rm fb}$. This is achieved by a time splitter with asymmetric flip-flop chains, as shown in Fig. 6, instead of the symmetric flip-flop chain in the dual-slope TDC. The front fine time $T_{\rm ff}$ is always one clock period longer than that of the dual-slope time-stretcher-type TDC because of the flip-flop, emphasized in gray in Fig. 6. This extra cycle is borrowed from the coarse time T_c, which is thus one clock period less than the original coarse time T_{c0}, as shown in Fig. 7(a). Thus, the coarse time T_c, the front fine time $T_{\rm ff}$, and the back fine time $T_{\rm fb}$ are slightly modified by the time splitter as follows:

$$\begin{aligned} \Delta T &= T_{c0} + (T_{\rm ff0} - T_{\rm fb0}) \\ &= (T_{c0} - T_{\rm clk}) + [(T_{\rm ff0} + 2T_{\rm clk}) - (T_{\rm fb0} + T_{\rm clk})] \\ &= T_c + (T_{\rm ff} - T_{\rm fb}) \end{aligned} \qquad (7)$$

where $T_{\rm clk}$ is one clock period.

The sum of the fine times to be stretched cannot exceed two clock cycles. When the sum of the fine times to be stretched is less than one clock cycle, the TDC simply concatenates the outputs of the coarse and fine counters to generate an output code for the total time interval. When the sum of the fine time is longer than or equal to one clock cycle, the falling edge of the most significant bit of the fine counter provides an additional pulse that increments the coarse counter by 1, as depicted in Fig. 4. This pulse is created by the falling-edge-to-glitch generator.

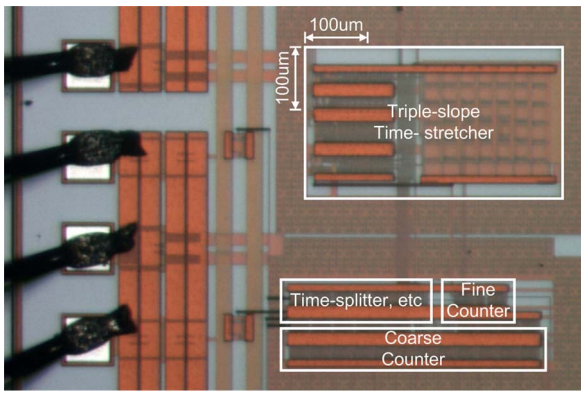

Fig. 8. Microphotograph of the TDC.

Finally, the situation when the time difference to be measured is shorter than one clock period should be considered. When both the start and stop signals rise between two consecutive rising edges of the operation clock, the original coarse time T_{c0} is zero. This case can be expressed by replacing T_{c0} with zero in (7) as follows:

$$\begin{aligned}\Delta T &= (0 - T_{\rm clk}) + [(T_{\rm ff0} + 2T_{\rm clk}) - (T_{\rm fb0} + T_{\rm clk})] \\ &= -T_{\rm clk} + (T_{\rm ff} - T_{\rm fb}) \\ &= -T_{\rm clk} + [(T_{\rm ff0} - T_{\rm fb0}) + T_{\rm clk}] \\ &= T_{\rm ff0} - T_{\rm fb0} \end{aligned} \tag{8}$$

where $T_{\rm clk} < T_{\rm ff} - T_{\rm fb} < 2T_{\rm clk}$. Hence, the edge-to-glitch generator always outputs a pulse for the coarse counter to tick up once. This single count-up is conceptually cancelled by the coarse time T_c, which is $-T_{\rm clk}$ because of the time borrowing scheme described above. However, the real output T_c from the time splitter in Fig. 6 cannot be $-T_{\rm clk}$, but it is $+T_{\rm clk}$. The occurrence of this exceptional case is indicated by a discard signal from the time splitter, as shown in Fig. 7(b). This signal resets the coarse counter and prevents it from ticking up by one clock pulse from the output T_c of time splitter and by the single pulse from the edge-to-glitch generator because the original coarse time is zero. Then, only the fine data $T_{\rm ff0} - T_{\rm fb0}$ is processed by the fine counter.

IV. Experimental Results

We designed and fabricated our triple-slope time-stretcher-based TDC in a 0.35-μm CMOS technology. Fig. 8 is a microphotograph of the TDC. Its active core occupies 0.126 mm^2 and consumes 1.22 mW with a 2.5-V supply voltage. We choose a reference clock frequency of 175 MHz. At this speed, one sample of the time difference can be processed within 2.5 μs, which corresponds to a measurement rate of 400 kS/s. The two capacitors $C_f = 4$ pF and $C_{\rm st} = 16$ pF are discharged with currents of $I_f = 5$ μA and $I_{\rm st} = 1.25$ μA, which result in a stretching factor of 16, which is equivalent to a 4-bit increase in resolution.

We used an Agilent 81150A signal generator and a synchronized Agilent 81110A signal generator to provide start, stop, and reset signals for testing the prototype chip. The output characteristics of the TDC were obtained using two clocks with slightly different periods of 40 and 40.001 μs as the start and stop signals, respectively. Fig. 9 shows the output of the TDC as the phase difference between the two signals gradually changes. The resolution of the TDC is 357 ps, and its dynamic range exceeds 1.46 μs, which effectively corresponds to 12 bits.

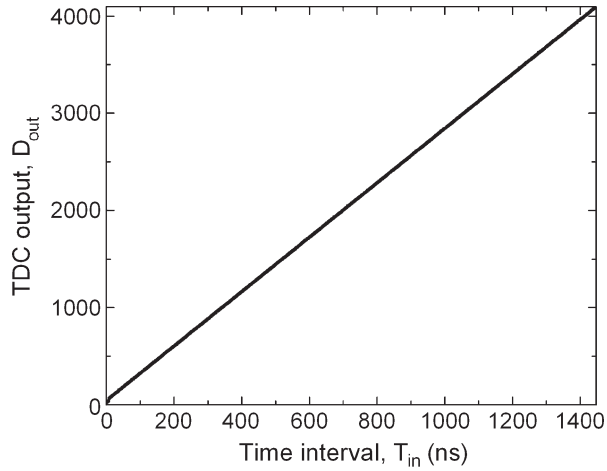

Fig. 9. Measured full-range output characteristics of the triple-slope-based TDC.

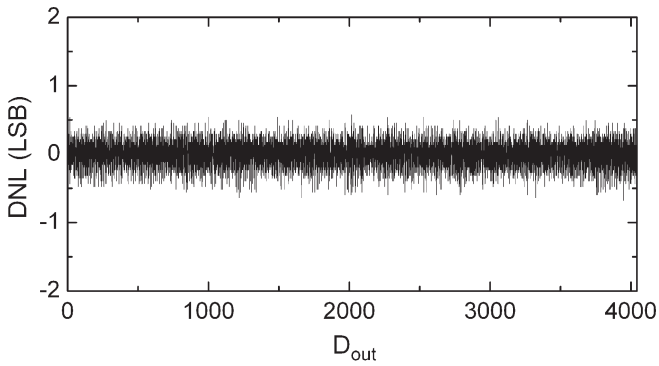

Fig. 10. Measured full-range DNL of the triple-slope-based TDC.

The start signal is a 10-kHz square-wave clock, and the stop signal is a 10-kHz clock with a 0.1-Hz down-ramp phase modulation. The phase difference between the start and stop signals are carefully tuned to achieve the full-range integral nonlinearity (INL) and differential nonlinearity (DNL). The code density test and the fast Fourier transform are performed, and the measured DNL and INL are found to be within 0.68 and 0.79 least significant bit (LSB), respectively, as shown in Figs. 10 and 11. Since the clock jitter can be as large as 40 ns, we average 20 measurements to ensure the validity of the output. The limitation of the INL is due to the metastability of the time splitter and the momentary mismatch of the coarse gain and the fine gain during the continuous operation [7].

In order to see the noise contribution in the TDC [8], a single-shot histogram of the proposed TDC is provided in Fig. 12. Two coupled clocks with fixed delays of 40 ns and 1 μs were provided to the start and stop signals. A total of 8192 outputs were measured for each input. The jitter in the start and stop

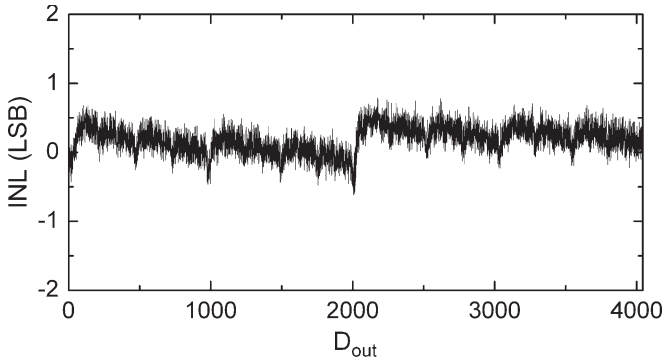

Fig. 11. Measured full-range INL of the triple-slope-based TDC.

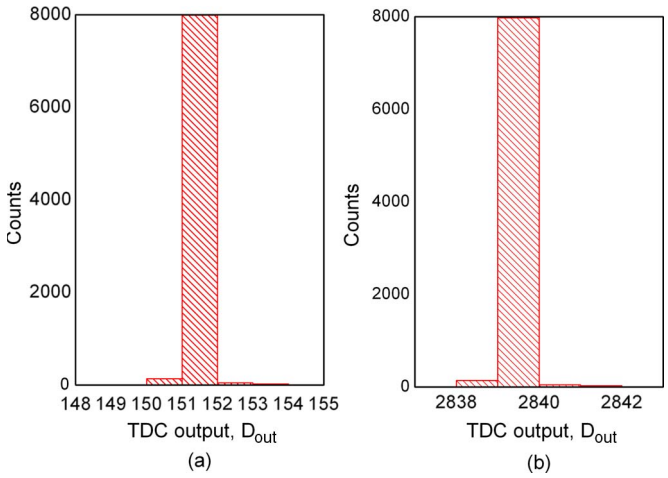

Fig. 12. Measured single-shot histograms of the triple-slope-based TDC for intervals of (a) 40 ns and (b) 1 μs.

TABLE I
SUMMARIZED PERFORMANCE OF THE TDC

Parameter	Value
Technology	0.35μm CMOS, 2.5V
LSB width	357ps
Input measurement range	>1.46 μs
Differential non-linearity	-0.68/+0.58 LSB
Integrated non-linearity	-0.62/+0.79 LSB
Power consumption	1.22mW (excluding I/O power)
Core area	0.126 mm^2

signals is mutually cancelled when the clocks are coupled in this way. The standard deviations of the two histograms are 0.18 and 0.19 LSB, respectively.

V. CONCLUSION

We have designed and fabricated a CMOS TDC for low-cost low-power portable devices. The input time interval has been coarsely measured by a main counter with a 175-MHz reference clock, and the fractional portions at the front and the back of the input time have been amplified by a time stretcher to improve the overall resolution of the TDC. This design achieves the same functionality as the previous dual-slope-based TDC with two parallel dual-slope time stretchers, but the use of a single triple-slope time stretcher saves chip area and power. The resolution of this new TDC is around 357 ps, the area of its core is 0.126 mm^2, and the power consumption is 1.22 mW. Our measurements of the performance of the TDC are summarized in Table I.

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