A Delta–Sigma Interface Circuit for Capacitive Sensors With an Automatically Calibrated Zero Point

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***Abstract*—We present a low-complexity interface circuit for capacitive sensors that are integrated into sensor microsystems. To reduce hardware cost while keeping high resolution, a first-order delta–sigma modulator (DSM), which balances the charge from the capacitive difference between sense and reference capacitors with the charge from a fixed-quantity capacitor, is employed. A charge-mode digital-to-analog converter and a successive approximation register are utilized to automatically calibrate the zero point of the interface circuit, which may shift further than a dynamic range. A prototype circuit fabricated in a 0.35-μm CMOS process has an active area of 0.048 mm^2. Its DSM operates at a sampling frequency of 1 MS/s with an oversampling ratio of 128. Experiments show that this circuit can read a capacitive difference from -0.5 to $+0.5$ pF with a 0.49-fF resolution. A capacitive offset that causes the zero point to shift can be canceled in the range from -2 to 2 pF with a 31.25-fF resolution. Measured power consumption was 1.44 mW at a 3.3-V supply.**

***Index Terms*—Capacitance, delta–sigma modulation, readout integrated circuit, sensors, successive approximation register (SAR).**

I. Introduction

CAPACITIVE sensors, consisting of a reference capacitor C_R and a sense capacitor C_S, are adopted in many recent studies on a sensor microsystem. Reading a capacitive difference is the fundamental job of an interface circuit for such capacitive sensors. Several circuits to read out the capacitive difference have already been published, which include a capacitance-to-voltage converter and a delta–sigma modulator (DSM) for converting analog voltage to digital codes [1], [2]. These circuits are complicated and large in area and thus increase hardware cost when incorporated in a monolithic sensor microsystem.

Interface circuits that utilize delta–sigma modulation and directly convert capacitance to digital codes [3]–[5] are a promising alternative. They utilize a switched-capacitor technique, which balances a signal charge from C_S with a reference charge from C_R using an integrating capacitor C_I, on which the average charge is zero. However, if a capacitive difference that is tiny compared with C_R is to be read, this technique requires a high-order DSM, which increases hardware cost. In most of applications, a capacitive difference varies usually in a small range compared with C_R. Therefore, if a charge from the difference between C_S and C_R is processed, this charge can be balanced with a charge from a fixed-quantity capacitor C_Q that is smaller than C_R. Such modification allows a first-order DSM to read a tiny difference that it could not read before.

Decreasing the magnitude of a balancing capacitor, however, disables a DSM to handle a large shift of the zero point in a way of subtracting it from digital codes: the zero point corresponds to a capacitive difference from no stimulus. In many practical situations, a capacitive offset, which causes the zero point to shift, is larger than the dynamic range of a capacitive difference. A shift of this magnitude can be canceled by adding or subtracting a calibrated charge with additional capacitors during readout operation [3], [4]. However, whenever a capacitive sensor is placed in a new environment or a specimen on the sensor is replaced by another, the zero point has to be recalibrated. This requires additional circuitry outside the interface circuit or user intervention. To provide a handy and compact solution to this problem, we have introduced a successive approximation register (SAR) and a charge-mode digital-to-analog converter (DAC) into our interface circuit. Together with an operational amplifier (op amp) of the integrator in the DSM, the SAR and the charge-mode DAC perform as a successive approximation capacitance-to-digital converter (SAR–CDC) during calibration mode. This SAR–CDC measures the capacitive difference between C_S and C_R. Then, in readout mode, the charge-mode DAC adds or subtracts a calibrated amount of charge. Switching between the two modes can be simply achieved by controlling two digital signals. In this brief, we present an interface circuit designed for use in a wide variety of mechanical and chemical applications [6]. This circuit employs a first-order DSM and a zero-point calibrator and monitors subfemtofarad change in a capacitive difference at time intervals of submilliseconds.

II. Proposed Interface Circuit for Capacitive Sensors

A. Delta–Sigma Interface Circuit

A schematic diagram of our interface circuit is shown in Fig. 1. The capacitive sensor under measurement also takes a part of a DSM so that the charge from $C_S - C_R$ is directly integrated at C_I. All capacitors including C_S, C_R, C_I, C_Q,

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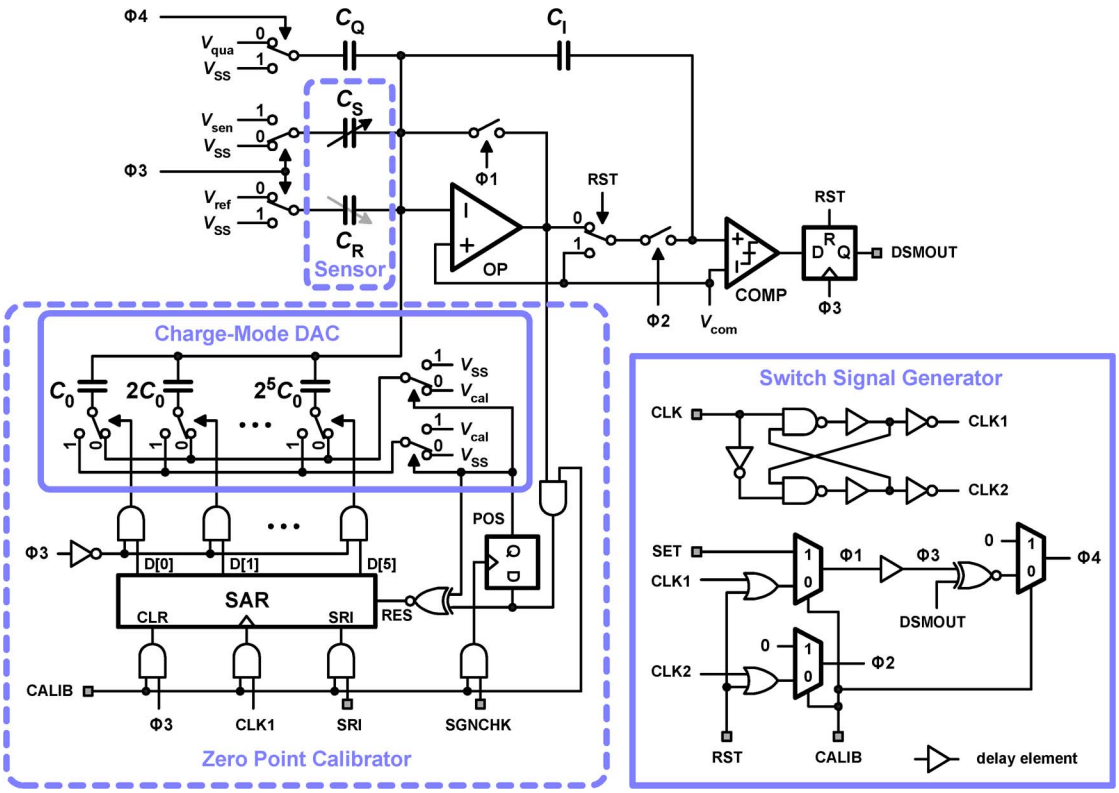

Fig. 1. Schematic of the proposed delta–sigma interface circuit.

and the capacitors in the charge-mode DAC share a common electrode at the negative input of the op amp OP.

During a readout, the zero-point calibrator is disabled by low CALIB. The SAR in the calibrator is reset to all zero by high CALIB and Φ3 before measurement, and thus, the Φ3 clock of the charge-mode DAC is masked out. Φ1 and Φ2 are, respectively, connected to the outputs CLK1 and CLK2 of the nonoverlapping clock generator. Φ3 is a delayed version of Φ1, and Φ4 is XNOR of Φ3 and DSMOUT.

If Φ1 or Φ2 is high, the output of OP is fed back to the common electrode by direct connection or through C_I. Thus, the common electrode is set to $V_{\rm com}+V_{\rm OS}$ by the feedback operation of OP, where $V_{\rm OS}$ means the input offset voltage of OP. When Φ1 and Φ3 are high, C_S and C_R are, respectively, charged to $V_{\rm sen}-(V_{\rm com}+V_{\rm OS})$ and $V_{\rm SS}-(V_{\rm com}+V_{\rm OS})$ with reference to the common electrode. Then, they are, respectively, discharged to $V_{\rm SS}-(V_{\rm com}+V_{\rm OS})$ and $V_{\rm ref}-(V_{\rm com}+V_{\rm OS})$, when Φ2 is high and Φ3 is low. Because the common electrode is floated during discharging operation, the charges $-C_S(V_{\rm sen}-V_{\rm SS})$ and $-C_R(V_{\rm SS}-V_{\rm ref})$, which are taken off from C_S and C_R, are transferred to C_I. Therefore, if the charge from C_Q is ignored, the integrator output increases by $[C_S(V_{\rm sen}-V_{\rm SS})-C_R(V_{\rm ref}-V_{\rm SS})]/C_I$ regardless of the input offset voltage $V_{\rm OS}$. When $V_{\rm sen}$ is set equal to $V_{\rm ref}$, this integrator processes C_S-C_R. As a result, we use an autozero technique for canceling $V_{\rm OS}$, which samples $V_{\rm OS}$ with C_S, C_R, and C_Q and also reduces $1/f$ noise at low frequencies [7].

The comparator COMP compares the integrator output with $V_{\rm com}$, and the result is sampled by a D flip-flop (FF). Because the integrator output is initially set to $V_{\rm com}$ by RST, the output of the D FF, which is DSMOUT, tells us whether C_I is more positively or negatively charged than it was initially. If DSMOUT is low, C_Q is switched in the same direction as C_S, and therefore, αC_Q is subtracted from C_R, where α is $(V_{\rm qua}-V_{\rm SS})/(V_{\rm ref}-V_{\rm SS})$. Otherwise, C_Q is switched in the same direction as C_R, and αC_Q is added to C_R. Because the charge from C_Q is added or subtracted in this way, the charge from C_S-C_R is balanced with that from C_Q regardless of its polarity. The number of low or high values at DSMOUT, respectively, corresponds to the number of $-\alpha C_Q$ or $+\alpha C_Q$ values, required for balancing C_S-C_R. Therefore, C_S-C_R can be expressed as follows:

$$N_0(C_S-C_R+\alpha C_Q)+N_1(C_S-C_R-\alpha C_Q)=0$$

and thus

$$C_S-C_R=\alpha C_Q(N_1-N_0)/(N_1+N_0) \tag{1}$$

where N_0 and N_1, respectively, are the number of low and high values. This equation shows that our DSM can read a capacitive difference from $-\alpha C_Q$ to $+\alpha C_Q$. Provided that αC_Q is larger than the maximum magnitude of C_S-C_R, a smaller αC_Q allows a smaller capacitive difference to be read, for an integer ratio $(N_1-N_0)/(N_1+N_0)$ with same precision.

B. Automatic Calibration of the Zero Point

The offset or initial value of C_S-C_R is canceled by the capacitors in the charge-mode DAC during readout mode. However, a combination of those capacitors is determined by

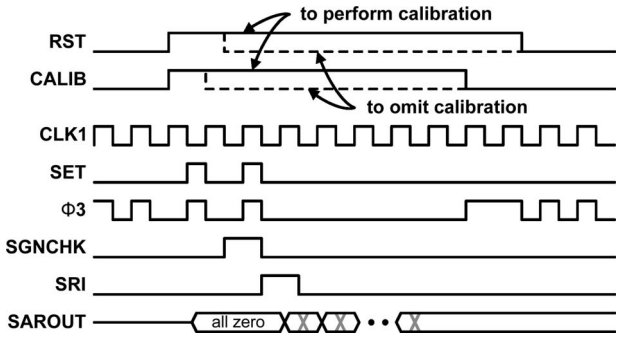

Fig. 2. Timing diagram of the zero-point calibrator.

successive approximation during calibration mode and stored in the SAR. The timing diagram of our calibrator is shown in Fig. 2. Note that the calibration mode can be omitted by controlling CALIB and RST appropriately.

During calibration, $\Phi 2$ and $\Phi 4$ are set to low by high CALIB, whereas $\Phi 1$ is connected to SET. Hence, COMP is disconnected from OP, C_Q is not switched, and C_I is serially connected to the parasitic capacitance at the positive input of COMP.

When SET is high, the common electrode is driven at $V_{\rm com}+V_{\rm OS}$ by OP. Therefore, C_S and C_R are, respectively, charged with $C_S(V_{\rm sen}-V_{\rm com}-V_{\rm OS})$ and $C_R(V_{\rm SS}-V_{\rm com}-V_{\rm OS})$ when $\Phi 3$ is also high. At the same time, the SAR is reset to all zero. When SET is low, the common electrode is floated. Then, the electrodes of C_S and C_R that are on the other side of the common electrode are, respectively, switched to $V_{\rm SS}$ and $V_{\rm ref}$ by low $\Phi 3$. However, the charge-mode DAC remains still. If the common electrode were kept at $V_{\rm com}+V_{\rm OS}$, then C_S and C_R would be charged with $C_S(V_{\rm SS}-V_{\rm com}-V_{\rm OS})$ and $C_R(V_{\rm ref}-V_{\rm com}-V_{\rm OS})$, and charges of $-C_S(V_{\rm sen}-V_{\rm SS})$ and $-C_R(V_{\rm SS}-V_{\rm ref})$ might remain at the common electrode. These extra charges are redistributed over the capacitors that share the common electrode. If the total capacitance of those capacitors is $C_{\rm tot}$, then the voltage V_- of the common electrode can be expressed as follows:

$$V_-=\left[C_R(V_{\rm ref}-V_{\rm SS})-C_S(V_{\rm sen}-V_{\rm SS})\right]/C_{\rm tot}+(V_{\rm com}+V_{\rm OS}). \tag{2}$$

When $V_{\rm sen}$ is set equal to $V_{\rm ref}$, OP tells the polarity of C_S-C_R regardless of its input offset voltage: if C_S-C_R is positive, OP produces a high level.

By using the first SET pulse, the polarity of C_S-C_R is stored as POS at a D FF controlled by SGNCHK. This sets the direction in which the capacitors in the charge-mode DAC are switched by the SAR. They are switched in the same direction as C_R if POS is high or switched oppositely if otherwise. Therefore, the values of those capacitors are added to or subtracted from C_R after multiplication by $(V_{\rm cal}-V_{\rm SS})/(V_{\rm ref}-V_{\rm SS})$.

After the second SET pulse, the extra charge at the common electrode is measured by canceling it successively with the DAC capacitors. When an SRI pulse is input, the SAR, which is shown in Fig. 3, switches D[5] to high at the first rising edge of CLK1 and updates D[5] with the value of RES at the next falling edge. This operation is subsequently performed on D[4] to D[0]. If OP indicates a polarity change after cancelation, RES is set to low by an XNOR. Otherwise, RES is set to high.

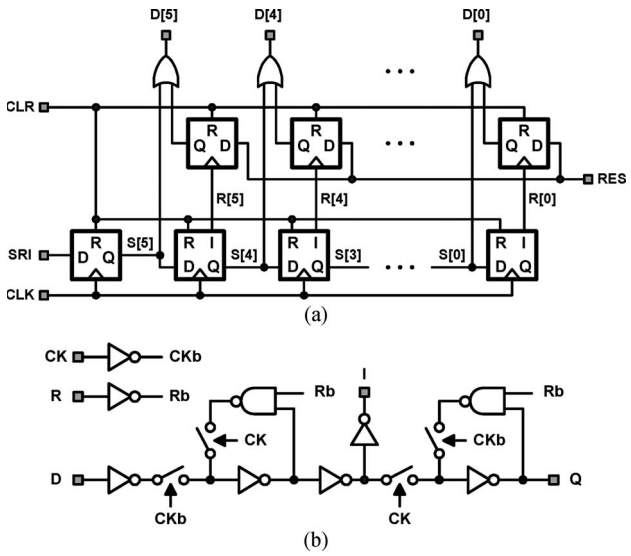

Fig. 3. (a) SAR and (b) its D FF with an intermediate signal output.

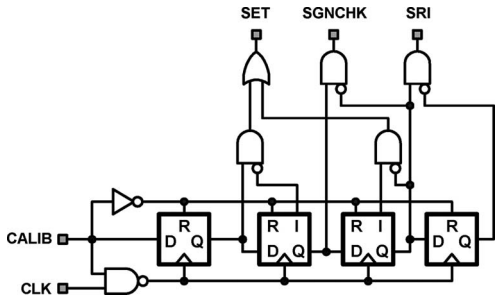

Fig. 4. Circuit to generate input signals of the calibrator.

It should be noted that the SAR switches in the opposite direction of $\Phi 3$ during cancelation. Therefore, the capacitors chosen by the SAR are switched by an inverted version of $\Phi 3$ during readout mode. As aforementioned, our calibrator requires the additional signals SET, SGNCHK, and SRI besides CALIB, but they can be generated by a simple circuit, as shown in Fig. 4. With the D FF shown in Fig. 3(b), signals without glitches can be obtained.

III. Experimental Results

A prototype circuit was designed in a 0.35-μm CMOS process. In this design, C_Q, C_I, and C_0 in Fig. 1 are sized at 0.5 pF, 2 pF, and 31.25 fF, respectively. Since this circuit processes charges from capacitors, its performance can be fully investigated by measuring voltage signals instead of measuring capacitance changes. For this purpose, C_S and C_R of 2 pF were also integrated in the circuit. However, the signal generation circuit shown in Fig. 4 has been omitted to avoid restricting the timing conditions during the experiment. The circuit has an active circuit area of 0.048 mm^2, and Fig. 5 is a photograph of it.

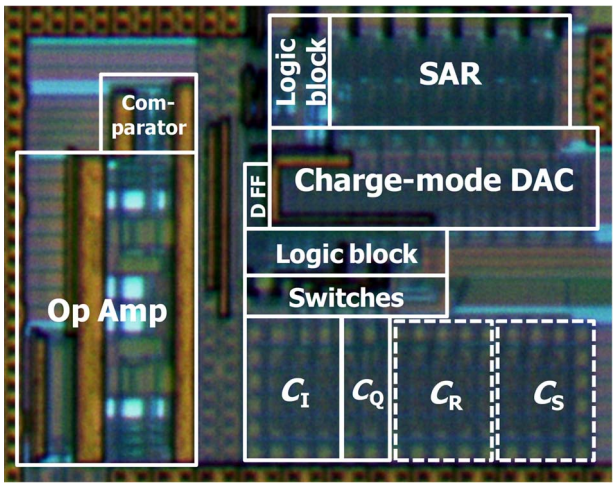

Fig. 5. Die photograph of the delta–sigma interface circuit.

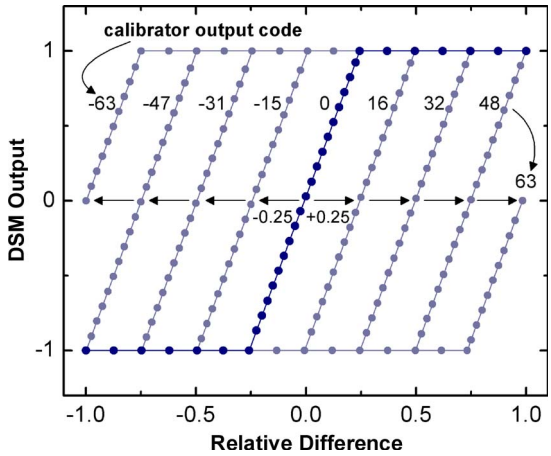

Fig. 6. Measured output characteristics of the interface circuit.

Our DSM operates at a sampling frequency of 1 MS/s with an oversampling ratio (OSR) of 128. In the experiments, $V_{\rm ref}$, $V_{\rm qua}$, and $V_{\rm cal}$ were set to half the value of $V_{\rm DD}$, and a signal was applied to $V_{\rm sen}$. Then, the interface circuit measured $V_{\rm sen} - V_{\rm ref}$. The output characteristics of the interface circuit are shown in Fig. 6. Relative differences were estimated by dividing the difference by $V_{\rm ref} - V_{\rm SS}$, where $V_{\rm SS}$ is grounded. The DSM outputs were decimated using a $\rm Sinc^2$ filter. As the initial offset measured by the zero-point calibrator shifts by multiples of 0.25, the input range of the DSM tracks it. The calibrator compensated for offsets from -1 to 1. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) values of the calibrator are, respectively, within ± 0.32 least significant bit (LSB) and ± 0.22 LSB, as shown in Fig. 7. The DNL and INL values were measured with a SAR–CDC, which is configured in calibration mode and operates with a 1-MHz clock. The SAR–CDC can be invoked repetitively by repeating CALIB, SET, SGNCHK, and SRI pulses while RST is high. Fig. 8 shows an output spectrum of the DSM for a sinusoidal input at 1.236 kHz. This was obtained for circuit operation without a calibration mode. The measured signal-to-noise ratio (SNR) and effective number of bits (ENOB) were respectively 63.3 dB and 10.2 bit. This means that the DSM achieves an 11-bit resolution, i.e., 0.49 fF in capacitance.

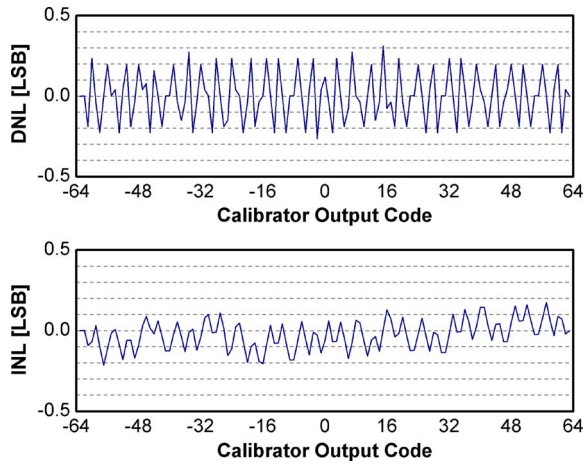

Fig. 7. Measured DNL and INL values of the zero-point calibrator.

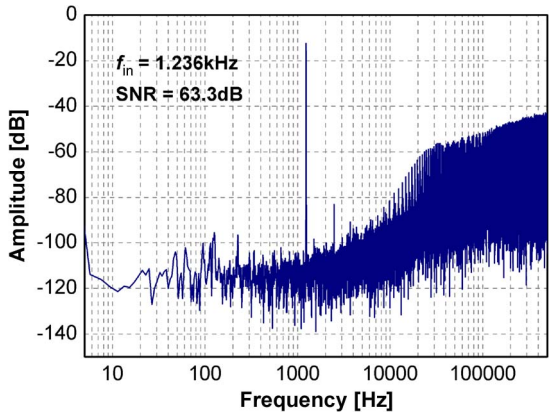

Fig. 8. Measured output spectrum of the DSM.

IV. Conclusion

We have presented an interface circuit for capacitive sensors that incorporates a first-order DSM and a SAR–CDC. The DSM only deals with a capacitive difference between sensor capacitors and thus can read a capacitive difference from -0.5 to $+0.5$ pF, with a resolution as fine as 0.49fF. The sampling frequency of this circuit is 1 MS/s with an OSR of 128. The SAR–CDC measures the initial offset of the capacitive sensor, and a set of capacitors selected by that circuit compensates for the offset. Then, the zero point of the interface circuit is calibrated. This procedure is automatically conducted by controlling only two digital signals. The SAR–CDC can read the offsets from -2 to 2 pF with a resolution of 31.25 fF. By employing simplified architectures for the DSM and SAR–CDC and letting them share an op amp, a circuit active area as small as 0.048 $\rm mm^2$ has been achieved. The measured power consumption was 1.44 mW with a 3.3-V supply.

References

[1] V. Petkov and B. E. Boser, "A fourth-order $\Sigma\Delta$ interface for micromachined inertial sensors," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1602–1609, Aug. 2005.

[2] W. Bracke, P. Merken, R. Puers, and C. V. Hoof, "Ultra-low-power interface chip for autonomous capacitive sensor systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 130–140, Jan. 2007.

[3] H. Matsumoto, H. Shimizu, and K. Watanabe, "A switched-capacitor charge-balancing analog-to-digital converter and its application to capacitance measurement," *IEEE Trans. Instrum. Meas.*, vol. IM-36, no. 4, pp. 873–878, Dec. 1987.

[4] J. O'Dowd, A. Callanan, G. Banarie, and E. Company-Bosch, "Capacitive sensor interfacing using sigma–delta techniques," in *Proc. IEEE Sensors*, Oct. 2005, pp. 951–954.

[5] B. George, S. Agrawal, and V. J. Kumar, "Switched-capacitor sigma–delta capacitance to digital converter suitable for differential capacitive sensors," in *Proc. IEEE Instrum. Meas. Technol. Conf.*, May 2007, pp. 1–3.

[6] M. Cha, J. Shin, J.-H. Kim, I. Kim, J. Choi, N. Lee, B.-G. Kim, and J. Lee, "Biomolecular detection with a thin membrane transducer," *Lab Chip*, vol. 8, no. 6, pp. 932–937, Jun. 2008.

[7] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.