A 0.3–1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller

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***Abstract*—A 0.3–1.4 GHz all-digital phase locked loop (ADPLL) with an adaptive loop gain controller (ALGC), a 1/8-resolution fractional divider and a frequency search block is presented. The ALGC reduces the nonlinearity of the bang-bang phase-frequency detector (BBPFD), reducing output jitter. The fractional divider partially compensates for the large input phase error caused by fractional-N frequency synthesis. A fast frequency search unit using the false position method achieves frequency lock in 6 iterations that correspond to 192 reference clock cycles. A prototype ADPLL using a BBPFD with a dead-zone-free retimer, an ALGC, a fractional divider, and a digital logic implementation of a frequency search algorithm was fabricated in a 0.13-μm CMOS logic process. The core occupies 0.2 mm^2 and consumes 16.5 mW with a 1.2-V supply at 1.35-GHz. Measured RMS and peak-to-peak jitter with activating the ALGC are 3.7 ps and 32 ps respectively.**

***Index Terms*—Adaptive gain control, all-digital phase locked loop (ADPLL), bang-bang phase and frequency detector (BBPFD), false position method, fractional divider, frequency search.**

I. Introduction

NOWADAYS many digital circuits depend on phase-locked loops (PLL) to generate clocks for system synchronization or to recover timing information from incoming data streams [1]–[3]. A conventional PLL consisting of analog circuits and passive elements is sensitive to process, voltage and temperature (PVT) variations; thus it requires low-leakage devices, a large chip area and ample voltage headroom [4]. As CMOS technology advances, we cannot continue to meet these requirements, and we need a new design of PLL that is compatible with modern nano-CMOS processes and suitable for massive and noisy digital systems.

The emerging all-digital phase-locked loop (ADPLL) is a practical alternative to an analog PLL. An ADPLL consists of purely digital components or digital equivalents, and thus all the states of these components can be represented as the combination of digital signals. Because there is no requirement for large passive elements in the loop filter, an ADPLL is stable at a lower supply voltage, more tolerant of PVT variations, and able to benefit from the reduction in area and power consumption associated with a scaled-down technology [5], [6]. Since all the internal signals are represented as digital values, internal states of an ADPLL can be stored and restored relatively easily in the registers, allowing signals to be processed flexibly with various techniques [7]–[9]. Moreover, we can subsequently reuse a large part of a proven circuit for other applications, and therefore an ADPLL design can be migrated to different technologies more efficiently. These advantages of robustness, flexibility and reusability have caused rapidly growing interest in the ADPLL, which has already replaced analog PLL in some high-performance applications [5]–[12].

In this paper, we present an all-digital fractional-N PLL with a digital gain control scheme. This uses a bang-bang phase-and-frequency detector (BBPFD) and an adaptive loop gain controller (ALGC), both of which can readily be migrated to advanced processes. The nonlinear phase detector of intuitive design would be expected to increase the output jitter, but a gain controller calibrates the open-loop gain to be proportional to the average phase error, so that the closed-loop bandwidth changes dynamically and the output jitter decreases. Although a similar technique has been applied to an analog PLL presented in [13], the frequency response of a digital filter in our scheme is not affected by PVT variations, which makes the calibration easier. Several adaptive gain control methods have already been presented in [14]–[16], but our proposed ALGC requires neither an external computational power nor a highly complex hardware. Another potential source of jitter is dithering between division factors, and thus is controlled by the use of a fractional divider in the feedback loop. Fractional division factors are incorporated through the sequential multiplexing of multiphase clocks.

The remainder of this paper has four sections. Section II describes some considerations and the motivation of this work. In Section III, we present our ADPLL architecture, and explain the detailed operation of each building block. An implementation is described and measured performance data are given in Section IV. Section V concludes the paper and summarizes the potential benefits of our approach.

II. Design Consideration

To optimize performance and to lessen structural complexity, the design of an ADPLL should be carefully examined over the trade-offs between performance and complexity. The most complicated parts of an ADPLL are the phase detector and oscillator, which usually require custom optimization. From this point of view, it is worthwhile to pay attention to the type of phase detector used in an ADPLL.

Phase detectors (PDs) can be classified into linear or nonlinear types. A time-to-digital converter (TDC) is a linear PD that produces a digital output proportional to the input phase

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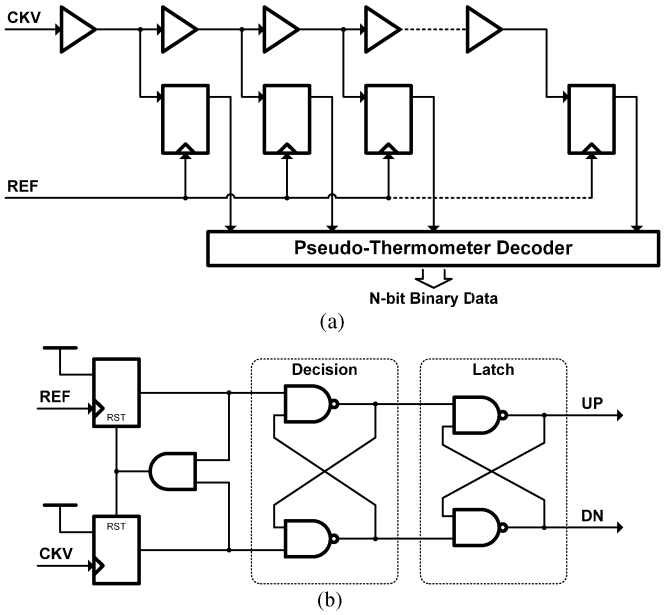


Fig. 1. Typical structure of (a) a linear and (b) a nonlinear TDC.

error. The time resolution of a TDC is generally related to the buffer delay, which is subject to PVT variations. Therefore, a high-resolution TDC requires precise analog circuitry, which increases the overall design complexity remarkably [17]. A nonlinear PD is much simpler and more robust, because it only consists of logic gates and merely indicates the direction of the phase error [5]. Naturally a bang-bang decision loses some information, but digital circuits can be used to supplement that result and these are insensitive to PVT variations.

A linear TDC is used for phase detection in many ADPLL circuits because of its fine resolution. Fig. 1(a) shows the typical structure of a linear TDC, which consists of many cascaded inverters and flip-flops. Input signals go through the inverter chain, and a series of D-flip flops (DFFs) clocked by a reference signal samples the delayed inputs. The thermometer-like output from the DFF array is translated to binary form by a decoder. The time resolution and detection range of a conventional TDC are respectively determined by the inverter delay and the length of the inverter chain. The improved performance of a high-resolution TDC is bought at the expense of an excessive number of inverters, which soak up power and area. Even a high-resolution TDC has limited frequency-detection capability, and a further aid to frequency locking may be required.

A BBPFD is effectively a nonlinear PD. Intuitive design yields the structure shown in Fig. 1(b) [18], in which a conventional PFD is followed by a decision circuit. The decision circuit resolves the priorities of the signals and the output latch holds that result until the next decision is delivered. Although the BBPFD is easy to design, it has a limit cycle problem [19], and the quantization effect of the DCO increases the output jitter. It is difficult to manage these nonlinearities effectively in an analog design, since that will require dealing with analog quantities. However, in an ADPLL, all traversing signals between building blocks are digital, and its core behavior of an ADPLL is described in VHDL or Verilog-HDL codes. Thus, the nonlinear effects can easily be controlled, and furthermore the RTL codes can be reused without major modifications. Consequently, employing the binary decision is a natural approach especially in an all-digital design. Therefore, we used a simple BBPFD in the proposed architecture and focused on how to deal with the nonlinearity of the bang-bang design.

III. Architecture

As shown in Fig. 2, the proposed ADPLL consists of a BBPFD, an adaptive loop gain controller, a digital loop filter (DLF), a first-order delta-sigma $(\Delta\Sigma)$ modulator, a multiphase digitally controlled oscillator (MDCO), a fractional divider, a PFD-based TDC, and a digital logic implementation of a frequency search algorithm. The BBPFD compares the arrival time of the reference clock edge with that of the divided DCO clock edge, and produces an early or a late signal. The DLF filters the phase error obtained from the BBPFD, and the resulting values are fed into the $\Delta\Sigma$ modulator. The gain of the DLF is changed by the ALGC to reflect the average phase error. The ALGC consists of a cascaded second-order IIR filter with two leaky integrators. The output of the $\Delta\Sigma$ modulator is sent to the MDCO and dithers the output clock signal of the MDCO to improve the frequency resolution. The MDCO contains a differential 4-stage ring oscillator with a supply voltage that is adjusted by a digitally controlled resistor [10]. The fractional divider receives 8-phase clock signal from the MDCO, and provides a division ratio between 7 and 16, in steps of 1/8. This small step size suppresses the input phase error caused by the alternating modulus of the feedback divider. A PFD-based linear TDC [18] is included only to verify the effectiveness of the ALGC, and the output of these two phase detectors can be multiplexed. The frequency search unit that implements the false position method achieves coarse frequency lock within 7 iterations. The computational overload of the frequency search unit is reduced because the use of a 1/8-resolution fractional divider allows some multiplications and divisions to be replaced by arithmetic shifts. The spread spectrum profile generator (SSPG) produces a triangular profile and modulates the output frequency. When the spread spectrum output is off, the SSPG behaves like a first-order $\Delta\Sigma$ modulator for the fractional-N synthesis.

A. Bang-Bang Phase-and-Frequency Detector

A linear TDC benefits from a delay line composed of many cascaded inverters, but the trade-off between time resolution and detection range of conventional one forces a wide-range fine-resolution TDC to require excessive hardware and become complex. We use the BBPFD shown in Fig. 3 to simplify the design and implementation of the proposed ADPLL. It detects phase and frequency errors to generate the output signals representing only the sign of errors. Unlike previous BBPFDs [5], ours generates two sets of results; one is a typical bang-bang output to control the overall gain for low jitter generation, and the other is a retimed output that is fed into the DLF. A conventional PFD composed of two flip-flops at the front part of the BBPFD produces UP and DN signals by comparing the rising edges of two input clocks. Then, a simple arbiter [20] which can resolve a timing difference of a few picoseconds in simulation, determines which event occurs earlier, and a following output

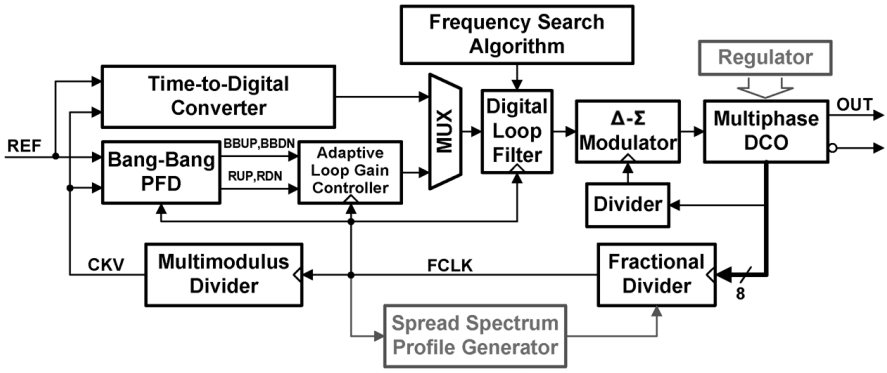


Fig. 2. Block diagram of the proposed ADPLL.

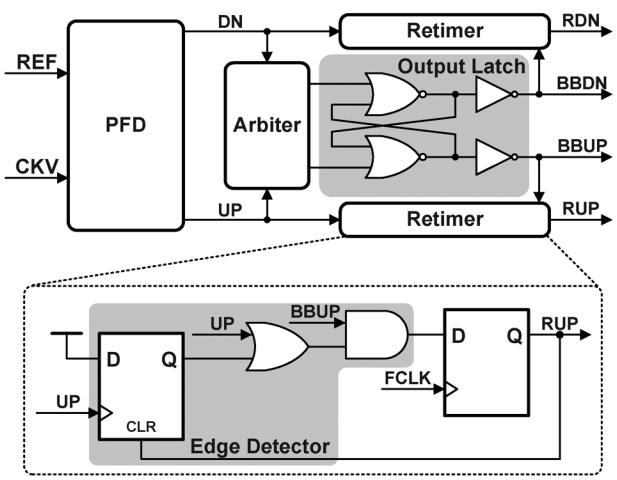


Fig. 3. Proposed BBPFD.

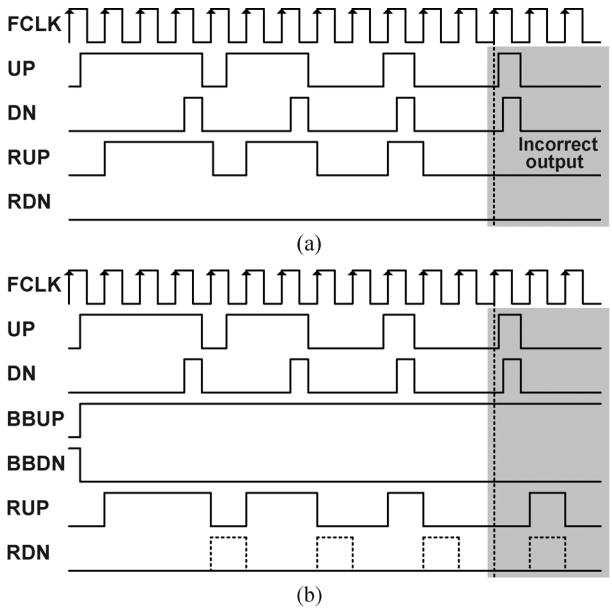


Fig. 4. Comparison of timing waveform from (a) a simple DFF and (b) the proposed retimer.

latch maintains BBUP or BBDN signal until a reverse direction event is detected. Because bang-bang signals are maintained for a relatively long period until the polarity of input phase error changes, the phase offset resulting from the bang-bang quantization is integrated over a considerable time, which makes the output peak-to-peak jitter increase. To shorten the integration period and reduce the output jitter, the implemented BBPFD in this work produces outputs controlled by the retimer. Simultaneously with the pulsewidth control, the retimer synchronizes the output of the BBPFD to the internal system clock (FCLK).

Fig. 4 shows a comparison of the timing waveform resulting from a simple D flip-flop (DFF) and the proposed retimer. The retimed signals are generated by sampling UP and DN outputs from the conventional PFD using the FCLK. As shown in Fig. 4(a), a DFF can perform as a simple retimer. However, the phase error information can be lost when the duration of the UP or DN pulse is shorter than the period of the FCLK signal, which causes a dead zone in the transfer characteristic. As a result, the output phase of the ADPLL wanders over the dead-zone and the output jitter increases proportionally. The proposed retimer, consisting of an edge detector and a sampling flip-flop, eliminates the dead zone. The edge detector extends the width of the UP or DN pulse until the next FCLK edge arrives, and the sampling flip-flop converts this extended output to a one-cycle-long pulse, so that no signal transitions are missed as shown in Fig. 4(b). In the steady state, the UP and DN pulses become quite short, so we intentionally inserted delay on the reset path in the tri-state PFD in order not to smear out the outputs by the latches. When either RUP or RDN is asserted, the corresponding BBUP or BBDN inhibits the retimer from generating opposite retimed pulses. For example, in Fig. 4(b), when BBUP is high, the RDN signal shown as a dotted line is not asserted.

B. Adaptive Loop Gain Controller

Although a BBPFD is easy to implement, its nonlinear characteristics and relatively large gain can cause significant output jitter. Lowering the loop bandwidth is a typical solution to getting better jitter performance, but that increases the lock time considerably. Instead, in our design, the ALGC dynamically adjusts the closed-loop bandwidth to reduce the output jitter without seriously affecting the lock time. Fig. 5 shows the structure of the DLF and ALGC. The DLF is separated into a proportional and an integral path, and its overall gain is controlled by

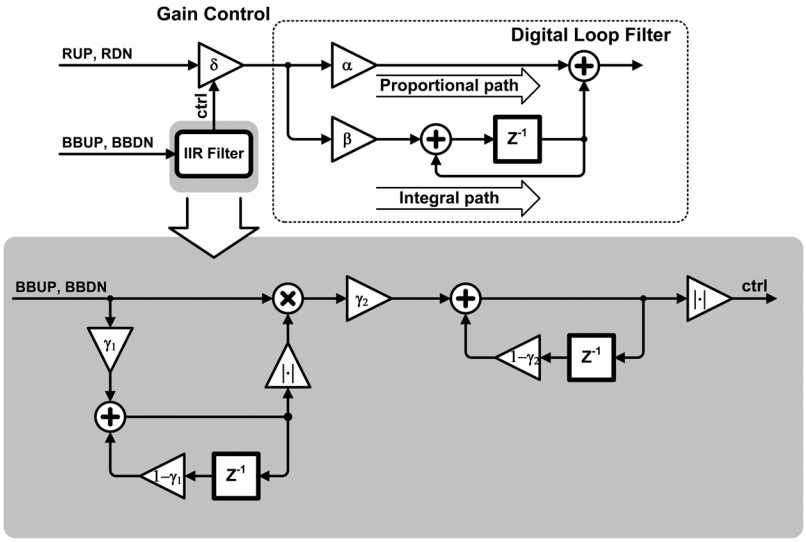


Fig. 5. Structure of the DLF and ALGC.

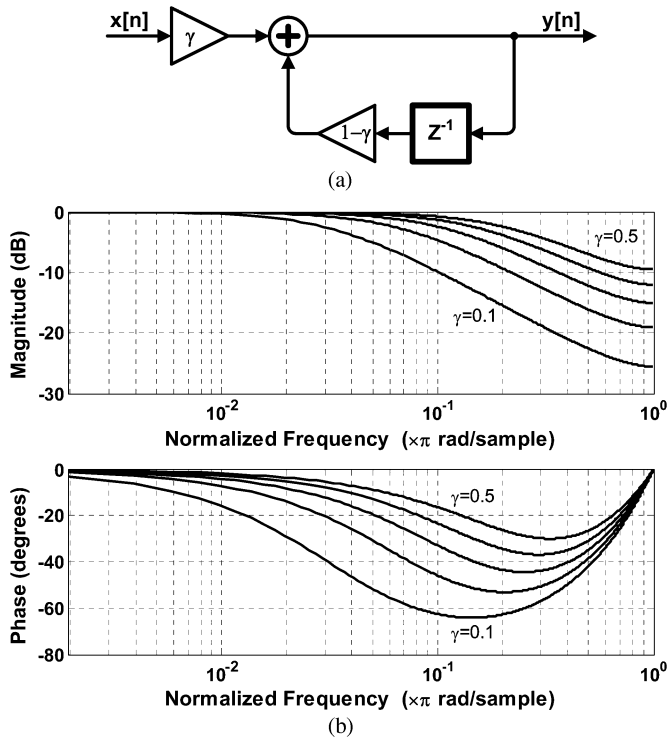


Fig. 6. Leaky integrator: (a) Z-domain model. (b) Frequency response.

the ALGC using a 2-stage IIR filter. This filter, which is composed of two leaky integrators and a multiplier, effectively averages the bang-bang output from the BBPFD. The phase delay of a typical cascaded 2-stage IIR filter is considerable, and it seriously affects the stability of the loop. In this work, the bang-bang output is fed into not only the first stage but also the second stage of the IIR filter through a multiplier to reduce the phase delay. Because the bang-bang output is 1 or -1, the multiplier either passes or negates the integrator output which can be readily realized with an adder and a few multiplexers in two's complement system.

C. Operation of the ALGC

As we have already stated, each stage of the IIR filter is based on a leaky integrator. Fig. 6(a) shows the z-domain model of the leaky integrator. The transfer function of this integrator can be expressed as follows:

$$\frac{Y(z)}{X(z)} = \frac{\gamma}{1-(1-\gamma)z^{-1}}, \quad (0<\gamma<1). \tag{1}$$

An integrator is commonly unstable and its output diverges for some inputs. But this circuit has a forgetting factor γ and forms a kind of low-pass filter with the frequency response shown in Fig. 6(b). If the input value is constant, the gain will be one and the output will approach the input value. On the other hand, the gain of this circuit will decrease for a fast switching input sequence.

$$x[n] = 1, -1, 1, -1, \cdots = \cos(\pi n)u[n]. \tag{2}$$

Equation (2) is an example of the fastest alternation, and it can be represented by a cosine function. u[n] expresses the unit step sequence. The z-transform of (2) is given as

$$X(z) = \frac{1-z^{-1}\cos(\pi)}{1-2z^{-1}\cos(\pi)+z^{-2}} = \frac{1}{1+z^{-1}}. \tag{3}$$

By combining (1) and (3), we can obtain the z-transform of the output sequence as follows:

$$Y(z) = \frac{\gamma}{1-(1-\gamma)z^{-1}} \cdot \frac{1}{1+z^{-1}}. \tag{4}$$

In this extreme case, the output sequence of the leaky integrator does not converge to a specific value because the region of convergence (ROC) for $Y(z)$ does not include the unit circle. Although the leaky integrator effectively averages the input, the output for (2) is not zero. Instead, the resulting sequence will have the alternating signs analogous to the input and the small magnitude determined by γ. This sequence is not suitable for the gain control because its sign keeps changing. Actually, the absolute value function follows the leaky integrator as shown in

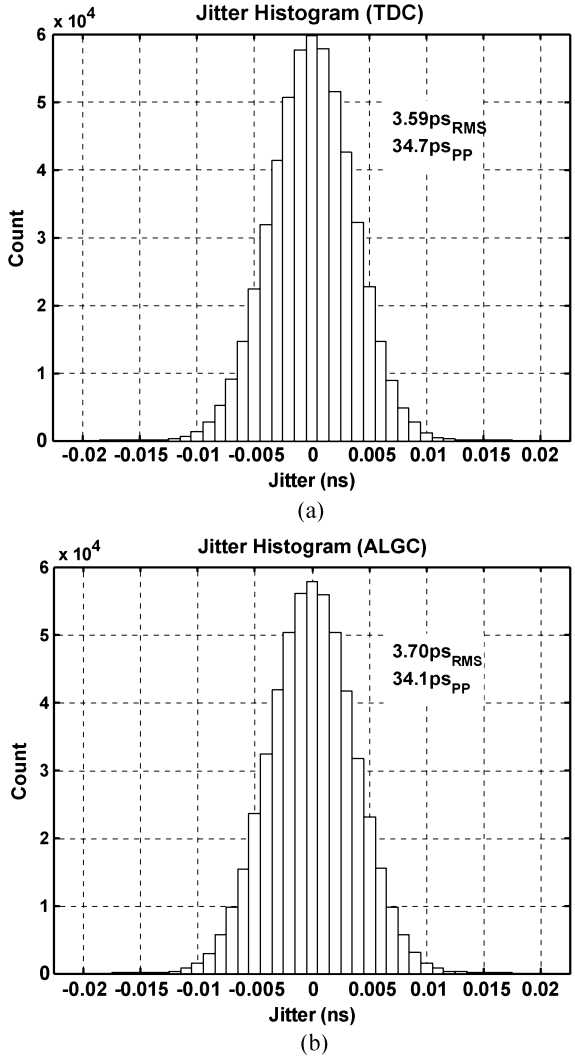


Fig. 7. Output jitter histograms: (a) using a linear TDC and (b) using a BBPFD with an ALGC.

Fig. 5, and we take the absolute value for controlling the overall gain of the loop filter. Because all poles of $(1-z^{-1})\cdot Y(z)$ are not inside the unit circle, we can not apply the final value theorem to calculate the gain in this case. If $y[n]=0$ for $n<0$, the nth number of the output sequence equals to

$$y[n]=\begin{cases}\sum_{k=0}^{n}\gamma(\gamma-1)^k, & \text{n is even.}\\ -\sum_{k=0}^{n}\gamma(\gamma-1)^k, & \text{n is odd.}\end{cases} \tag{5}$$

This equation also confirms that the polarity of the output sequence continuously changes. After some trivial calculation, the final value can be expressed as follows:

$$|y[\infty]|=\left|\lim_{n\to\infty}\sum_{k=0}^{n}\gamma(\gamma-1)^k\right|=\frac{\gamma}{2-\gamma}. \tag{6}$$

This equation tells us that the gain of a leaky integrator for a fast alternating sequence obtained from (6) is less than unity.

This result gives us an insight into how the IIR filter works. If the ADPLL is in an unlocked state, the BBPFD will make constant up or down signals during the frequency tracking. Therefore, the gain of the IIR filter will be about one, and the closed-loop bandwidth will not be significantly affected. As the ADPLL approaches a locked state, the output of the BBPFD alternates between up and down more quickly, and the average input phase error drops. As a result, the absolute output value of the IIR filter will decrease and the closed-loop bandwidth and the output jitter will be reduced accordingly. The IIR filter consists of two cascaded leaky integrators, therefore the final value approaches

$$|y[\infty]|=\frac{\gamma_1\gamma_2}{(2-\gamma_1)(2-\gamma_2)}\approx\frac{\gamma_1\gamma_2}{4} \tag{7}$$

for sufficiently small γ_1 and γ_2. In other words, the ALGC makes the open-loop gain proportional to the average phase error, and we can fulfill adaptive gain control according to the loop condition. With the dynamically changing closed-loop bandwidth, moderate lock time and low jitter can be achieved.

We verified the effect of the ALGC by means of an HDL simulation. The core RTL code used in this simulation is synthesizable except the DCO and TDC models. The DCO behavioral model includes 2.5 $\mathrm{ps_{RMS}}$ random timing jitter and 80 $\mathrm{fs_{RMS}}$ random timing wander [21]. The resolution of the TDC model used in this simulation is 30 ps. The output jitter histogram of the ADPLL using a linear TDC and a BBPFD with the ALGC are shown in Fig. 7(a) and (b), respectively. The ADPLL using a linear TDC has shown slightly better performance. However, the ALGC is fully synthesizable, and this advantage makes it more appropriate for an all-digital design than a full-custom linear TDC.

D. Digital Loop Filter

The proposed ADPLL uses a typical loop filter structure with a proportional and an integral path. The dynamics and the noise of the digital bang-bang PLLs using this filter have already been discussed in the literature [19], [22]–[25]. The jitter can be expressed as follows [25]:

$$\sigma_j\approx\frac{1+D}{\sqrt{3}}\cdot N\alpha K_{DCO} \tag{8}$$

where σ_j is the standard deviation of the jitter, D is the filter latency, N is multiplication factor, α is the proportional path gain, and $\mathrm{K_{DCO}}$ is the DCO gain. A proper value of α can be obtained from this equation if the target jitter is given. The integral path gain β is given by

$$\frac{\alpha}{\beta}\geq\sqrt{\frac{2\pi}{3}}\cdot(1+D)\cdot\tan\left(\sqrt{\frac{3}{2\pi}}\cdot\frac{D}{1+D}+\varphi_{m0}\right) \tag{9}$$

where φ_{m0} is the minimum phase margin [25]. For the stable operation, β should be much smaller than α. Equation (9) is derived from the case when the DLF operates at the reference clock rate. In the proposed architecture, however, the DLF operates at the FCLK rate which is faster than the reference clock rate, and, thus, the DLF integrates the phase error more frequently, while the proportional path of the DLF remains steady. Therefore, we set β to be smaller than the value calculated from (9) at least by the ratio of the FCLK frequency to the reference frequency.

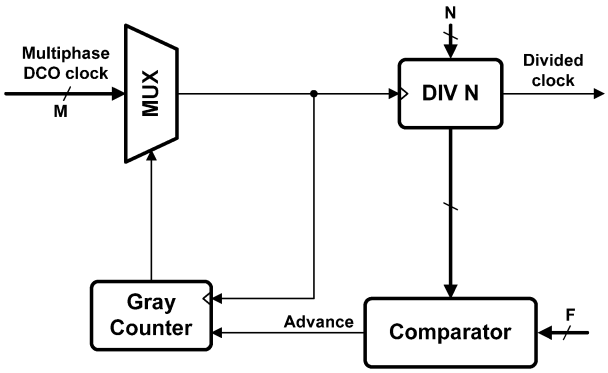


Fig. 8. Block diagram of the fractional divider.

Since this scheme reduces the effective latency, the output jitter performance is improved according to (8).

E. Fractional Divider

A typical fractional-N frequency synthesizer adopts a dual-modulus divider. The fractional-N PLL generates a fraction of the input frequency by alternating the modulus between two consecutive integers. This usually results in large phase error, due to the modulation of the feedback divider. In our architecture, a fractional divider is used to reduce the large phase error resulting from the changes of division ratio. The fractional divider consists of an 8-to-1 phase multiplexer (MUX), a divider, a 4-bit comparator and a 3-bit Gray-code counter, as shown in Fig. 8. It uses multiphase clock from the MDCO, and its operation is based on the sequential input clock multiplexing. The differential output of the MDCO is multiplexed and fed into the divider to generate the output clock signal. The 4-bit comparator produces an advance signal by comparing the fractional part (F) with the internal count of the divider. The Gray-code counter is activated and the count increases one by one while the advance signal is high. The MUX control input is changed according to the value of the counter, and then the leading clock signal, right ahead of current multiplexed output, is selected by the MUX so that the output phase can advance forward. Repeating this process achieves the fractional division, which may also be achieved by moving the output phase backward as shown in Fig. 9. In that case, however, glitches will appear in the multiplexed output, and the divider will malfunction [26]–[28].

Albeit using the known architecture, we implemented the fractional divider with a Gray-code counter to further minimize unwanted glitches in switching MUX selection signals. Generally, the number of phases determines the control step of the fractional divider. If the fractional divider uses M-phase clock and F times of phase advance taking place every N input cycles $(\mathrm{N} \geq \mathrm{F})$, its division ratio becomes (N-F/M). Fig. 10 shows an operation example of the fractional divider using 8-phase clock. During the operation, N and F are 8 and 3 respectively, and the resulting division ratio is (8-3/8). In this design, the division ratio ranges from 7 to 16 in steps of 1/8.

F. Digitally Controlled Oscillator

The MDCO consists of a differential 4-stage ring oscillator and a digitally controlled resistor (DCR) [10]. Fig. 11 shows the

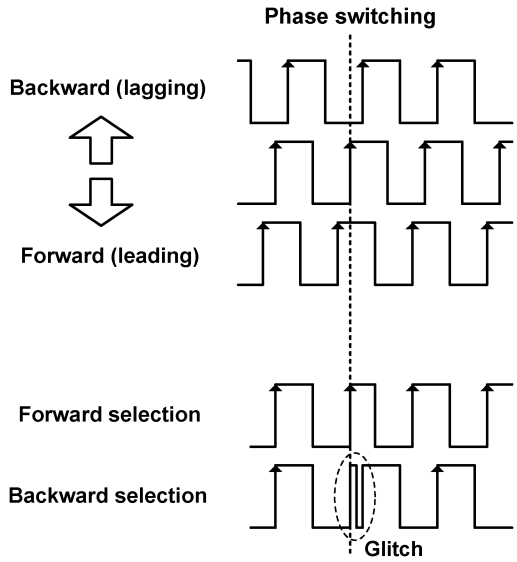


Fig. 9. Forward and backward phase switching.

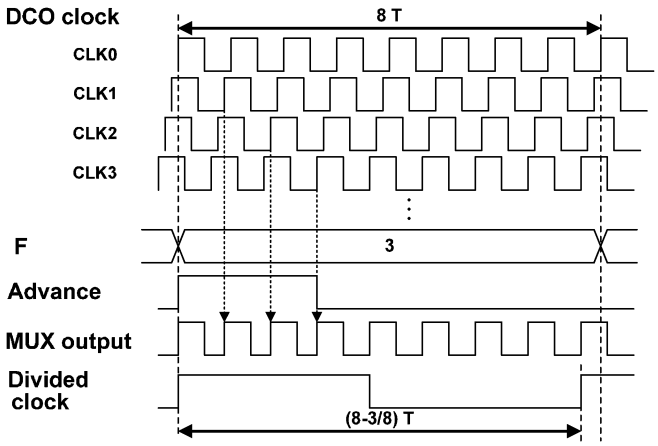


Fig. 10. Example operation of the fractional divider using an 8-phase clock.

block diagram of the MDCO, which generates the 8-phase clock required to operate the fractional divider. Each stage of the ring oscillator is the typical starved-inverter-based delay cell plus a pseudo-differential output buffer. The supply voltage of the ring oscillator, which is controlled by the DCR, changes the output frequency. The DCR is composed of many digitally controllable pMOS transistors arranged in a 32×32 matrix. Some of these transistors are always turned on to guarantee minimum current path. The input code to the DCR is dithered by a first-order $\Delta\Sigma$ modulator operating at the quarter of the output frequency. The $\Delta\Sigma$ modulator generates the 1-bit dither sequence from the 18-bit fractional part of the DLF output. This sequence is added to the 10-bit integer part of the DLF output, and fed into a decoder. We implement the segmented-thermometer control scheme in the DCR to obtain better linearity than the binary control scheme using relatively small hardware [10].

The noise of the MDCO operating at 1.4 GHz is smaller than the quantization noise of the phase detector [29] or the effect of the fractional spur. Therefore, the output jitter performance is

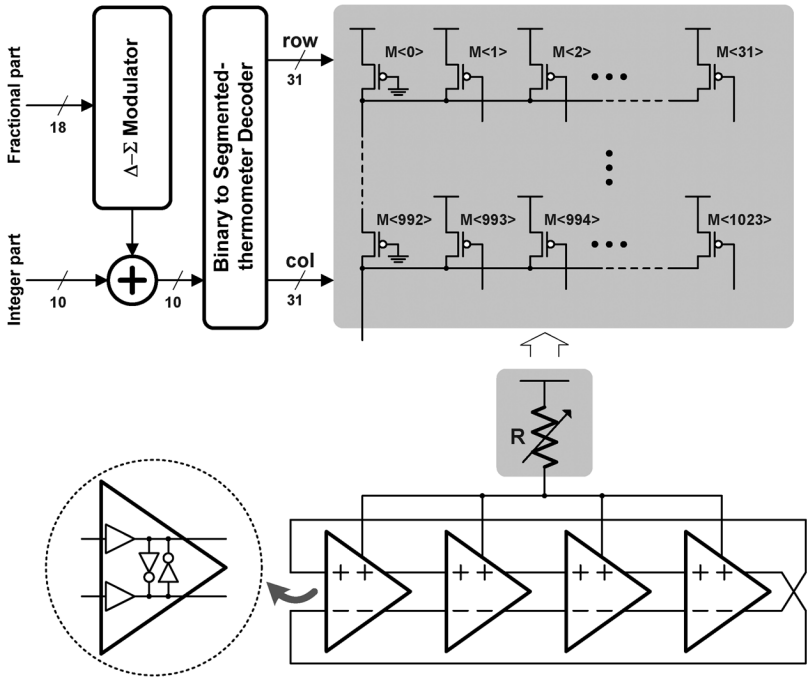


Fig. 11. MDCO.

dominated by the noise from the phase detector. With the proposed adaptive gain control technique, the phase detector noise is effectively low-pass filtered by the loop.

G. PFD-Based Time to Digital Converter

As mentioned earlier, we employed the BBPFD and ALGC to design a simple ADPLL with reduced output jitter in this work. To assess the effectiveness of the ALGC, we also implement a PFD-based linear TDC [30] for comparison of performance. Its output is proportional to the input phase error around the lock point, and it is tied to the minimum or maximum code except in the linear region. Since the PFD-based TDC can detect not only phase error but also frequency error, a long delay line is not necessary to increase the detection range. This TDC generates a 15-bit thermometer code, and its resolution changes with PTV variations between 20 ps and 40 ps in a transistor-level simulation.

H. Frequency Search

Because the phase detectors that we use are based on a PFD, an additional aid to frequency locking is not usually necessary. However, some applications may require a fast lock time despite the narrow closed-loop bandwidth. If the tuning range of the DCO is wide, depending solely on the PFD is a restrictive solution, and it is better to implement a frequency search function. In an ADPLL, several frequency search algorithms can be easily applied to shorten the lock time [31], [32].

A frequency search circuit usually includes some counters to measure the output frequency. Binary search is a popular way of using such counters, and the size of the code set containing the final solution is halved every iteration. To increase the convergence rate, Newton's method can be applied, but it requires excessive computational overhead to calculate derivatives. We use the false position method [33] rather than binary search to accelerate the convergence with relatively small hardware overhead. The false position method is a linear interpolation technique to estimate the final code. At first, the code is set to the minimum and the lowest output frequency of the DCO is found. Next, the highest output frequency is found with the code maximum. We can calculate the code corresponding to the target frequency from these two initial points by assuming that the frequency characteristic is a linear function. Generally, the output frequency of the DCO does not linearly depend on the input code, and there occurs some frequency error. As we repeat above process several times, the error becomes smaller, and if the error is less than 2%, the frequency search finishes.

IV. Experimental Results

The output clock jitter of the ADPLL was measured using a Tektronix TDS8200 digital sampling oscilloscope. The ADPLL was operated with a 1.2-V supply at room temperature. The input frequency was from 10 to 50 MHz and the output frequency was from 0.3 to 1.4 GHz. Table I is a performance summary which compares our ADPLL with previously published four other designs using low cost standard CMOS technologies.

A. Circuit Implementation

The test chip was implemented in a 0.13 μm CMOS process, and Fig. 12 is its microphotograph. The digital blocks were synthesized automatically, while the MDCO, the TDC, the fractional divider and other high-speed dividers were designed through manual layout. Since we could describe the function of the fractional divider using a synthesizable HDL code, a gate-level circuit of the divider could be easily produced by automated placement and routing (P&R) if the operational frequency was low. However, the divider requires being able to operate at the fastest clock speed in this ADPLL. This makes

TABLE I
COMPARATIVE PERFORMANCE OF FIVE ADPLLS

		This work	[11]	[35]	[36]	[37]
Process		0.13 μm	65 nm	0.18 μm	0.18 μm	65 nm
DCO type		Ring	LC	Ring	Ring	Ring
Power supply (V)		1.2	1.2	1.8	1.8	1.1
Reference frequency (MHz)		50	25	59.375	25	25
Multiplication factor		27	120	16	60	120
Tuning range (GHz)		0.3–1.4	3	0.033–1.04	1.1–2.2	0.19–4.27
RMS jitter	(ps)	3.7 (@ 1.35 GHz)	0.4* (@ 3 GHz)	13.8 (@ 950 MHz)	4 (@ 1.5 GHz)	1.4 (@ 3 GHz)
	(%)	0.5	0.12	1.31	0.6	0.42
Peak-to-peak jitter (ps)		32 (@ 1.35 GHz)	N/A	86.7 (@ 950 MHz)	28.4 (@ 1.5 GHz)	15 (@ 3 GHz)
Area (mm^2)		0.2	0.4	0.32	0.2	0.04
Power dissipation (mW)		16.5 (@ 1.35 GHz)	10 (@ 3 GHz)	15.7 (@ 1.04GHz)	15 (@ 1.5 GHz)	11.8 (@ 3 GHz)

*Estimated from the phase noise plot

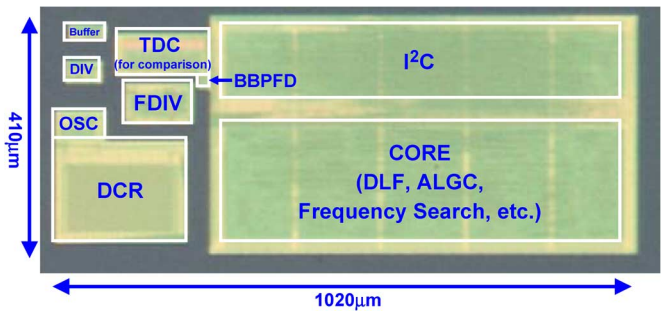


Fig. 12. Microphotograph.

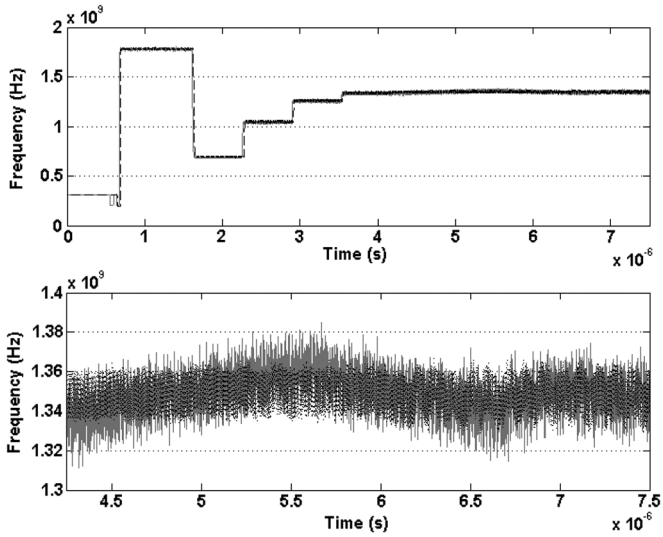


Fig. 13. Frequency-locking behavior.

it vital to minimize the critical path delay, and therefore we handle the layout of the divider manually.

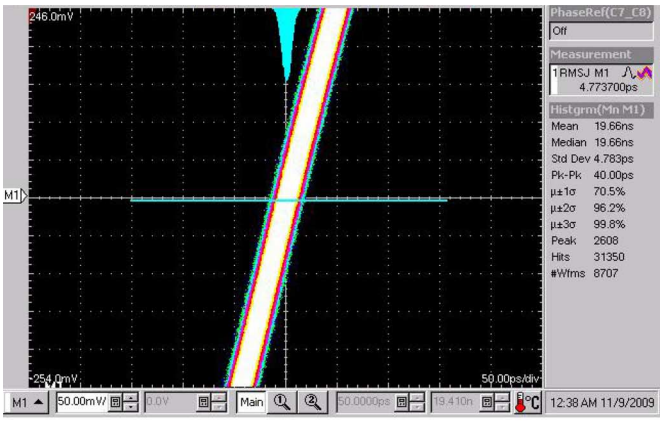
Fig. 12 shows that the BBPFD is much smaller than the TDC, and the BBPFD requires least custom optimization. It was designed using CMOS gates from a standard cell library, except for the simple arbiter which is composed of several transistors. Since the structure is simple, the BBPFD is more reusable and we need little effort to design it compared with designing the TDC. Conversely, the PFD-based linear TDC requiring 15 samplers and 16 delay cells can realize finer resolution, but the gain of TDC which is related with its resolution changes depending on the PVT variation. The contents of the digital core include an ALGC, a DLF, a $\Delta\Sigma$ modulator, and a multi-modulus divider. The core has many controllable parameters, which allow the circuit to be configured in many different ways, and an I^2C interface was implemented to manage these parameters.

B. Frequency-Locking Behavior

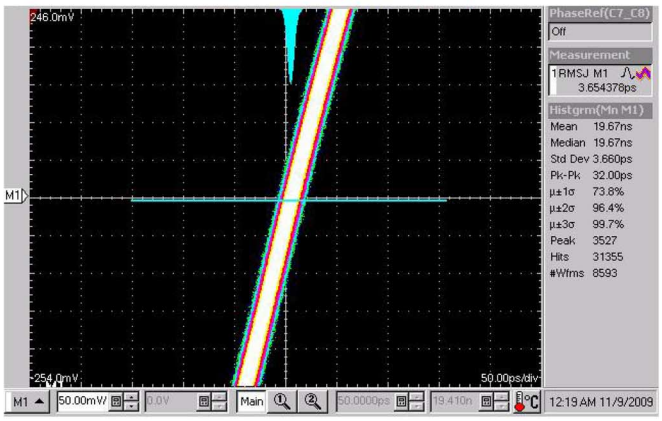
We measured the frequency-locking behavior of the proposed ADPLL by using LeCroy WaveRunner 6200 A digital oscilloscope. Fig. 13 shows the change of output frequency when the reference frequency is 50 MHz and the output frequency is 1.35 GHz. This figure shows that frequency search is completed after 6 iterations, and the duration of each iteration is 32 reference cycle. The locking behavior with the ALGC is shown in a solid line and the lock-time is about 7.5 μs. The locking behavior with the TDC is shown in a dotted line and the lock-time is about 6 μs. In the steady state, the output frequency is 1.35 GHz, but large frequency fluctuation arising from period jitter has been observed due to the noise injected from the measurement environment.

C. Effect of ALGC on Jitter

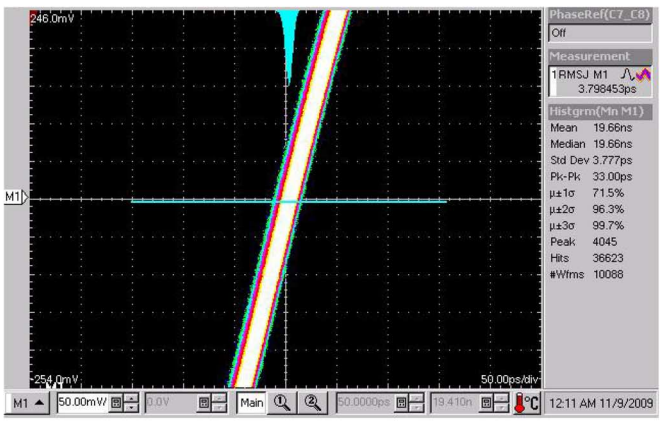
We assessed the effectiveness of the ALGC by measuring the output jitter. The multiplication factor is 27 with the reference frequency of 50 MHz and the output frequency of 1.35 GHz for the measurement. The FCLK frequency is 150 MHz and the ratio of the FCLK frequency to the reference frequency is 3 in



(a)



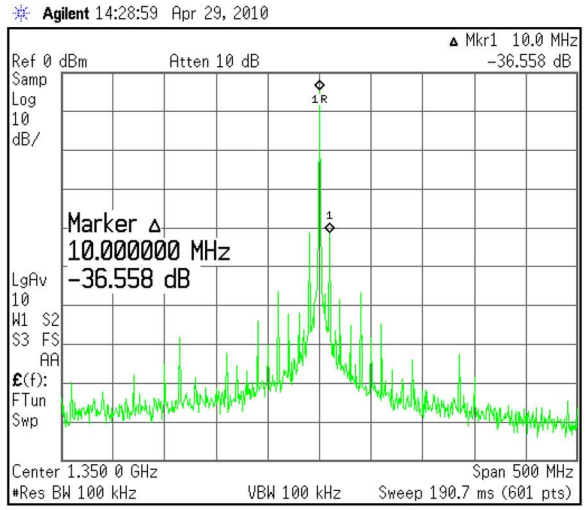
(b)



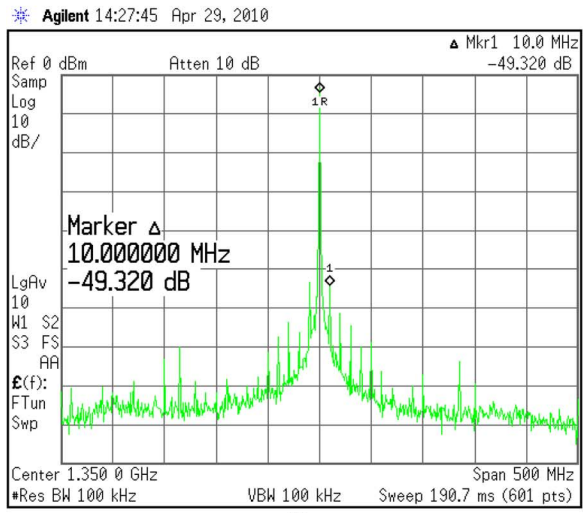
(c)

Fig. 14. Measured output jitter histogram: (a) using the BBPFD without the ALGC (4.8 ps_{RMS}); (b) using the BBPFD with the ALGC (3.7 ps_{RMS}); and (c) using the TDC (3.8 ps_{RMS}).

this case. Fig. 14(a) shows a histogram of output clock jitter, measured with the BBPFD and the ALGC deactivated. When the filter coefficients α and β were respectively 2^{-4} and 2^{-14}, the RMS and the peak-to-peak jitter were measured as 4.8 ps and 40 ps, respectively. Fig. 14(b) shows the equivalent histogram with the same filter coefficients and with the ALGC activated. The ALGC coefficients γ_1 and γ_2 were 2^{-2} and 2^{-1}, respectively. In the locked state, the gain of the ALGC approaches 2^{-5} according to (7) and the effective α and β approach 2^{-9} and 2^{-19}, respectively. However, β is limited to 2^{-18} because the fractional part of the DLF output is 18-bits wide. The RMS



(a)



(b)

Fig. 15. Measured output spectrum: (a) using the BBPFD without the ALGC; (b) using the BBPFD with the ALGC.

and the peak-to-peak jitter were 3.7 ps and 32 ps, respectively. The application of the ALGC shows about 30% improvement on the jitter performance. The output spectrum of each case is shown in Fig. 15. We can observe that the spurs are reduced and the jitter performance is improved when the ALGC is turned on. As explained in Section III, we can confirm that the ALGC suppresses the nonlinear property of the BBPFD and can reduce the jitter in its locked state.

Beside the BBPFD, the PFD-based linear TDC was implemented in the proposed ADPLL to compare the performance of the BBPFD supported by the ALGC with that of a linear TDC. Fig. 14(c) shows a measured output clock jitter histogram when the TDC is selected for a phase detector and resulting RMS and peak-to-peak jitter were 3.8 ps and 33 ps. The filter coefficients α and β were 2^{-6} and 2^{-14}, respectively. Although the steady-state output jitter is around the minimum resolution of the TDC, the output of the TDC will not become a mere bang-bang signal due to the phase error generated by the dual-modulus divider in a fractional-N synthesizer. In this case, the quantization noise is smaller than that of the BBPFD, so the TDC will

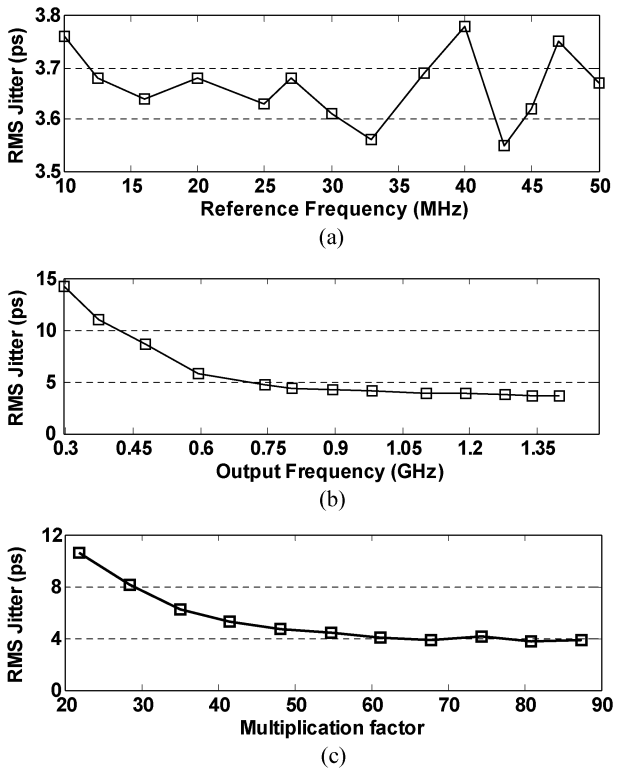


Fig. 16. Jitter performance: (a) with the fixed output frequency (1.35 GHz); (b) with the fixed multiplication factor (29.79); (c) with the fixed reference frequency (16 MHz).

show better jitter performance. In an integer-N case, the TDC can turn into bang-bang mode. However, the transient behavior of the BBPFD is restricted due to its limited output range, and there occurs a trade-off between the lock time and the jitter performance. Therefore, using the BBPFD may require increasing the loop parameters in some case, and the TDC can show better performance than the BBPFD depending on the condition. The output clock jitter histogram when the BBPFD is used with the ALGC is already shown in Fig. 14(b). These two measurements show almost the same result and agree with the HDL simulation in Section III. Consequently, the BBPFD cooperated with the ALGC is a good substitute for a linear TDC so that subtle custom optimization can be avoided.

D. Jitter Performance

The jitter performance as a function of the input frequency is shown in Fig. 16(a). The output frequency is fixed at 1.35 GHz and the multiplication factor is changed accordingly. Although we can find some fluctuation in jitter performance, total variation is restricted within 10%. Fig. 16(b) shows the jitter performance when the multiplication factor is fixed at 29.79 and the output frequency is varied for the same loop parameters. Fig. 16(c) shows the jitter performance when the reference frequency is fixed at 16 MHz. Although the jitter increases as the output frequency decreases, the ratio of the jitter to the output period is better at low frequencies.

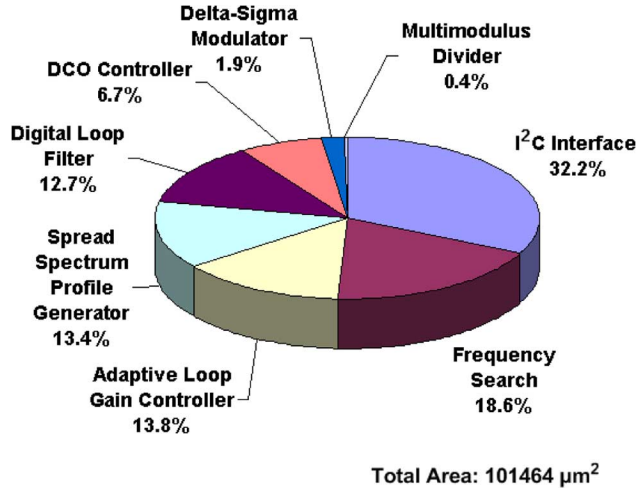


Fig. 17. Active area of each synthesized block.

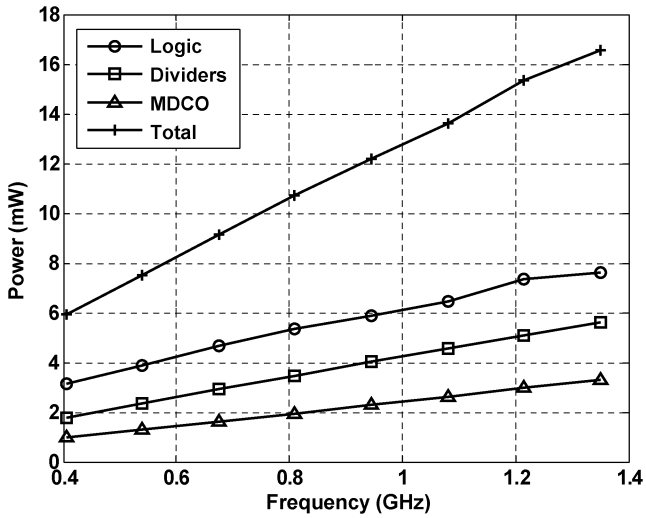


Fig. 18. Power dissipation of each circuit block.

E. Area and Power Consumption

The size of the ADPLL is 1.02 mm × 0.41 mm but the core area related with the operation of the ADPLL excluding the TDC for comparison, the I^2C interface, and decoupling capacitors is only 0.2 mm^2. The active area of each synthesized block is shown in Fig. 17. In this figure, only the area of the logic gates is taken into account, and the overhead caused by timing and routing constraints that come out during P&R are not considered. Practically, the size of digital block increases after P&R. We set the core utilization to 50% at the floor planning step, and thus realized circuits occupied about twice larger area than shown in this figure. The area of the BBPFD plus the ALGC is about 0.029 mm^2 whereas that of the TDC is only about 0.012 mm^2 because we keep the number of the delay elements as small as possible without any margin.

The ADPLL consumes 16.5 mW with a 1.2-V supply. Fig. 18 shows the power dissipation of each circuit block as a function of the output frequency. To change the output frequency, the division ratio of feedback divider is fixed, and the input frequency is varied from 15 to 50 MHz. The total power consumption of

the ADPLL was proportional to the output frequency. Because the fractional divider and other dividers operate at the fastest clock frequency, they consume considerable amount of the total power. The logic power marked with circles includes the power consumption of the BBPFD, the TDC, the digital core and the buffers of digital input/output pads. In a simulation, the power consumption of the BBPFD is 0.028 mW and that of the ALGC is 0.3 mW, while that of the TDC is 0.31 mW when the reference frequency is 50 MHz and the FCLK frequency is 150 MHz.

Our priority in designing the digital blocks was flexibility, and thus the circuits are somewhat over-specified. In the present design, the digital blocks take relatively large area and the logic power dissipation is more than 50% of the total, but it could readily be reduced in line with a more defined specification.

V. Conclusion

We have presented an ADPLL with a BBPFD incorporated with an ALGC, a fractional divider, and a fast frequency search algorithm. Simulated and measured results show how the ALGC is able to suppress the nonlinearity of the bang-bang design. The 1/8-resolution fractional divider reduces the large phase error at the input of the ADPLL and fast frequency lock is achieved by applying the false position method. The measurements show acceptable performances, and this demonstrates the practical applicability of the proposed architecture.

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