A Fast-Acquisition PLL using Split Half-Duty Sampled Feedforward Loop Filter

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Abstract — *We reduce the pattern jitter and acquisition time of a phase-locked loop (PLL) by adopting the split half-duty sampled feedforward loop filter. A prototype designed and fabricated in a 0.18μm standard CMOS technology has a 40% lower acquisition time than a PLL without operating in fast acquisition mode. Its peak-to-peak jitter is 26% less than that of a PLL with a conventional 2nd-order RC loop filter.*[1]

Index Terms — Acquisition time, loop filter, pattern jitter, phase locked loop (PLL).

I. Introduction

Phase-locked loops are key components of integrated circuits and consumer electronics products, providing a stable clock source to digital, analog circuits and systems. Timing jitter is inherent in PLLs, and this needs to be minimized if circuits are to operate properly. In a charge-pump PLL, the main source of jitter, excluding the inherent oscillator phase noise and any supply noise, is the pattern jitter caused by the non-ideal nature of the charge pump. Several techniques have been proposed to reduce pattern jitter [1], [2]. In particular, a half-duty sampled feedforward loop filter can achieve a low pattern jitter, and it only requires a simple control method, and imposes no circuit overhead [2].

In recent consumer electronics products, PLLs are commonly turned off when the system enters sleep mode, in order to reduce overall power consumption. This makes it important that the output clock of the PLL has a short acquisition time when emerging from the sleep mode. This can be achieved by gear-shifting techniques which change the charge-pump current or the capacitance of the loop filter [3]-[5]. However, these techniques are required to change at least two of PLL parameters because their techniques are based on 3rd-order PLL. This requires a complicated architecture which takes up a lot of area. To solve this problem, in this paper, we present a new design of PLL circuit adopting the split half-duty sampled feedforward loop filter.

The remainder of this paper has four sections. Section II provides an overview of the pattern jitter problems. Section III describes our new PLL architecture. In Section IV, we present measured results from an experimental prototype PLLs, designed and fabricated using a 0.18μm CMOS technology. Section V concludes the paper and summarizes the potential benefits of our approach.

II. The Problem of Pattern Jitter

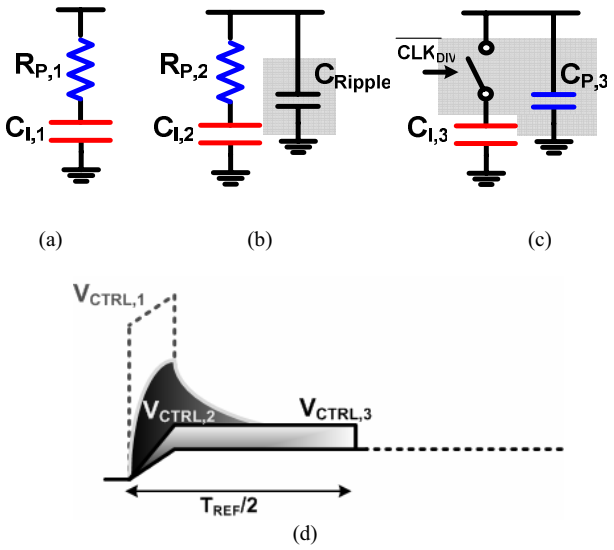

Fig. 1. Loop filter networks and the ripple of VCTRL:, (a) 1st-order RC loop filter, (b) 2nd-order RC loop filter, (c) half-duty sampled feedforward loop filter and (d) ripple of VCTR.

Charge-pump PLL needs both proportional gain and integral gain for stable feedback. In a conventional charge-pump PLL, as shown in Fig. 1(a), a resistor in the loop filter makes proportional gain and a capacitor makes integral gain. However, the resistor causes a lot of ripple in V_{CTRL} of the voltage-controlled oscillators (VCO), as shown in Fig. 1(d). This ripple causes frequency fluctuations in the VCO and pattern jitter in the PLL. In many designs, this ripple in V_{CTRL} is filtered by an additional capacitor, C_{Ripple}, as shown in Fig. 1(b). However, the insertion of C_{Ripple} tends to degrade the stability of the PLL, and careful design is required to ameliorate this problem. Moreover, filtering V_{CTRL} with C_{Ripple} does not totally eliminate fluctuations in V_{CTRL}. To alleviate this problem, proportional gain spreading techniques have been proposed [1], [2]. By spreading the proportional gain across either a full reference period or half of a reference period, these feedforward loop filters dramatically reduce pattern jitter. In particular, as shown in Fig. 1(c), a half-duty sampled feedforward loop filter has a straightforward

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architecture, a simple control method, and almost no overhead. A half-duty sampled feedforward loop filter works in the following way: First, it samples the charge from the charge pump using the proportional capacitor $C_{P,3}$, and the voltage across $C_{P,3}$ achieves the proportional gain. Then, when CLK_{DIV} is low, the sampled charge in $C_{P,3}$ is shared with the integral capacitor $C_{I,3}$. Eventually, this shared voltage produces integral gain. A half-duty sampled feedforward loop filter does not rely on C_{Ripple} to provide filtering, but acts as a 1st-order RC loop filter (Fig. 1 (a)), with the following characteristics:

$$R_{P,1} = \frac{T_{REF}}{2} \cdot \frac{1}{C_{P,3}} \qquad C_{I,1} = C_{P,3} + C_{I,3} \tag{1}$$

We can also show that a half-duty sampled feedforward loop filter has less effect on stability than a 2nd-order RC loop filter shown in Fig.1(b), because the additional pole in the open-loop transfer function that would be created by C_{Ripple} is eliminated.

III. Proposed Loop Filter

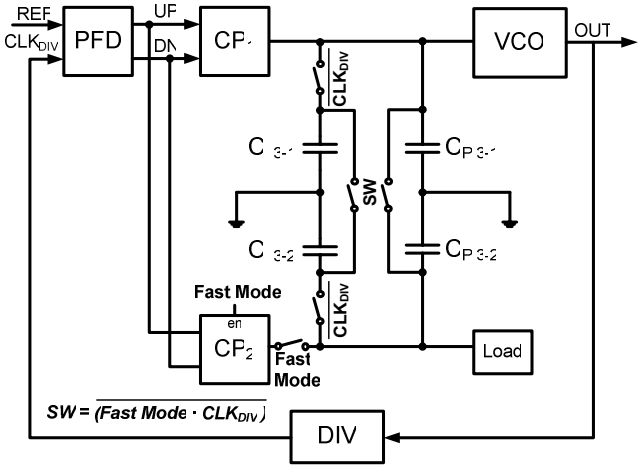


Fig. 2. Block diagram of the proposed PLL with a split half-duty sampled feedforward loop filter.

Figure 2 shows PLL architecture with proposed split half-duty sampled feedforward loop filter. Because this type of loop filter has 1st-order characteristics, we do not have to adjust several parameters to achieve a sufficient phase margin [4]. Instead, we split the capacitances C_I and C_P of the half-duty sampled feedforward loop filter into two equal parts.

Our new loop filter operates as follows: In fast acquisition mode, both CP_1 and CP_2 turn on transfer charge into the split loop filter. In the sampling phase of the fast acquisition mode, when CLK_{DIV} is high, charge from CP_1 is sampled by $C_{P,3\text{-}1}$, while charge from CP_2 is simultaneously sampled by $C_{P,3\text{-}2}$. After CLK_{DIV} goes low, sharing phase of the fast acquisition mode starts. Charge sampled at $C_{P,3\text{-}1}$ and $C_{P,3\text{-}2}$ is shared across all the capacitors: $C_{P,3\text{-}1}$, $C_{P,3\text{-}2}$, $C_{I,3\text{-}1}$, and $C_{I,3\text{-}2}$. This step makes our design tolerant of any mismatch in size between the upper and lower capacitors. As $C_{P,3\text{-}1}$ and $C_{P,3\text{-}2}$ are charged at the same time, and $C_{I,3\text{-}1}$ and $C_{I,3\text{-}2}$ are sharing their charge, the effective capacitance of the PLL during fast acquisition mode can be expressed as follows:

$$C_{P,fast} = C_{P,3-1} = C_{P,3-2} = \frac{C_{P,3}}{2} \qquad C_{I,fast} = C_{I,3-1} = C_{I,3-2} = \frac{C_{I,3}}{2} \tag{2}$$

In a charge-pump PLL, the acquisition time mainly consists of pull-in time and lock time [6]. The pull-in time of a PLL is not explained by an s-domain linear model or by s-domain loop transfer analysis. Pull-in time is only related to the large signal behavior of the PLL, and follows this equation:

$$T_{pull\_in} \propto \frac{I_{CP}}{C_{I,1}} = \frac{I_{CP}}{C_{I,3} + C_{P,3}} \tag{3}$$

However, the lock-time of a PLL exactly depends on its loop bandwidth in the s-domain linear model:

$$T_{lock} \propto BW = \frac{K_{VCO} I_{CP} R_{P,1}}{2\pi \cdot N} \propto R_{P,1} \propto \frac{1}{C_{P,3}} \tag{4}$$

When our PLL is in fast acquisition mode, the effective capacitances of both C_P and C_I are halved, reducing both pull-in time and lock time by half. This allows the system to wake-up quickly from sleep mode.

When the PLL gets frequency acquistion, it is switched from fast acquisition mode to normal operation mode. In normal operation mode, CP_2 is turned off and the charge from CP_1 is transferred to both $C_{P,3\text{-}1}$ and $C_{P,3\text{-}2}$. Then, the sampled charge is shared across all the capacitors. Therefore, the equivalent loop filter capacitances are as follows:

$$C_{P,normal} = C_{P,3-1} + C_{P,3-2} = C_{P,3} \qquad C_{I,normal} = C_{I,3-1} + C_{I,3-2} = C_{I,3} \tag{5}$$

In normal operation mode, the loop bandwidth of the PLL stabilizes, and the magnitude of the fluctuation in V_{CTRL} is reduced because of the larger capacitance of the loop filter.

IV. Experimental Results

The proposed PLL was designed and fabricated in a standard 0.18μm CMOS process. Its microphotograph is shown in Fig. 3. To assess the relative jitter, a PLL with 2nd-order loop filter were also designed and fabricated on the same die.

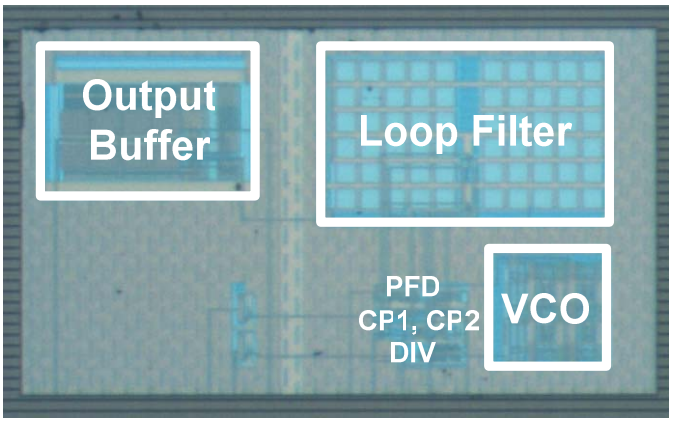


Fig. 3. Die photograph of the proposed PLL.

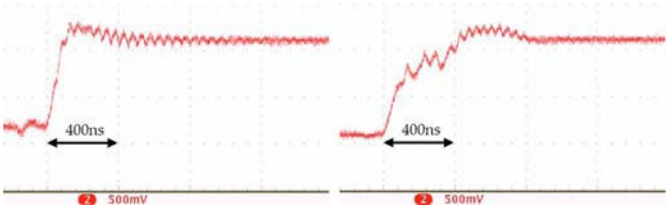


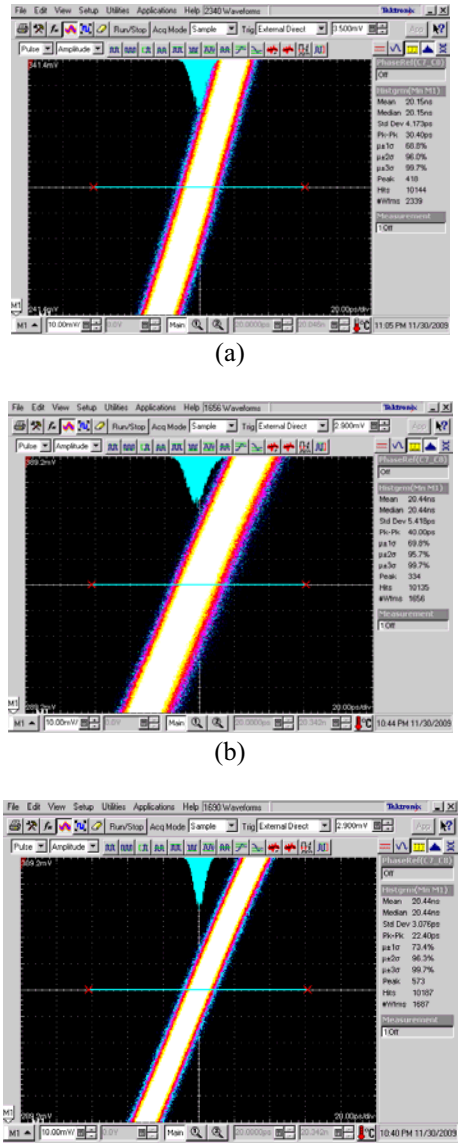
Fig. 4. Measured control voltage of PLL: a split half-duty sampled feedforward loop filter in (a) fast acquisition mode and (b) normal operation mode.

Figure 4 shows measured control voltage of PLL to check the acquisition time of the proposed PLL in both fast acquisition mode and normal operation mode. The reference frequency in normal operation is 20MHz, the output frequency is 1.6GHz. The measurement results suggest that the acquisition time in fast acquisition mode is about 40% less than in normal operation mode.

TABLE I
COMPARISON OF JITTER PERFORMANCE

Symbol	RMS Jitter (ps)	Peak-to-Peak Jitter (ps)
Conventional 2nd-order RC loop filter	4.173	30.40
Split half-duty sampled feedforward loop filter (fast acquisition mode)	5.418	40.00
Split half-duty sampled feedforward loop filter (normal operation mode)	3.076	22.40

Table 1 and Figure 5 show the measured jitter performance of the PLL. The RMS jitter of our PLL is 3.076ps, and the peak-to-peak jitter is 22.40ps. We see that our PLL in its normal operation mode has lower pattern jitter than a conventional 2nd-order RC loop filter, and almost the half amount of jitter as a PLL in the fast acquisition mode.



(a)

(b)

(c)

Fig. 5. Measured jitter histogram: (a) 2nd –order RC loop filter, (b) a split half-duty sampled feedforward loop filter in fast acquisition mode and (c) a split half-duty sampled feedforward loop filter in normal operation mode.

V. CONCLUSION

A PLL with our split half-duty sampled feedforward loop filter can achieve a fast acquisition time, by effectively reducing the capacitance of the loop filter as well as a low pattern jitter, by spreading the proportional gain during half of the reference cycle. The PLL is silicon-proven in a standard 0.18μm CMOS technology, and its performance was experimentally assessed by measuring the acquisition time as well as jitter characteristics. The IC has an active area of 0.068mm^2 and consumes 10.28mW at a 1.8V supply.

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BIOGRAPHIES

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