CMOS differential-capacitance-to-frequency converter utilising repetitive charge integration and charge conservation

H. Lee, J.-K. Woo and S. Kim

A low-complexity CMOS circuit is proposed for reading out monolithically integrated differential capacitive sensors. It directly converts the differential capacitance of a MEMS sensing device to a frequency by accumulating the charges produced by repeated charge integration and charge conservation. A prototype chip has been designed and fabricated in 0.35 μm CMOS technology. Experimental results show that differential capacitance is linearly converted to output frequency.

Introduction: Capacitive sensors are regularly employed in a wide variety of mechanical and chemical applications, including pressure sensing, fingerprint recognition, hazardous gas detection and the monitoring of biomolecular reactions. These sensors can be implemented within microelectromechanical systems (MEMS), so as to achieve a higher density of devices and better compatibility with the complementary metal-oxide-semiconductor (CMOS) process [1]. Several methods of reading out capacitive sensors [2] have already been published, in which capacitance-to-voltage conversion is followed by voltage-to-digital conversion using a delta–sigma oversampling analogue-to-digital (A/D) converter. But these circuits are relatively large and complicated. One of the alternative candidate circuits that offers the possibility of meeting this requirement is the capacitance-to-frequency converter (CFC) [3]. It produces a digitised output signal without requiring the complexity of an A/D converter, and thus reduces the hardware cost. We propose a further simplified CFC circuit in which the capacitance-to-voltage conversion (CVC) and voltage-to-frequency conversion (VFC) stages are merged into a single direct CFC that only requires a single opamp in its core. The operations needed for the proposed circuit can be implemented with concise components since the circuit only converts the difference between two capacitances into an output frequency, without measuring their full values. The circuit is able to detect small changes in this differential capacitance, and hence in the quantity being measured by the sensor. The sign of this differential capacitance, indicating which of the two capacitances being compared is the larger, is also reported.

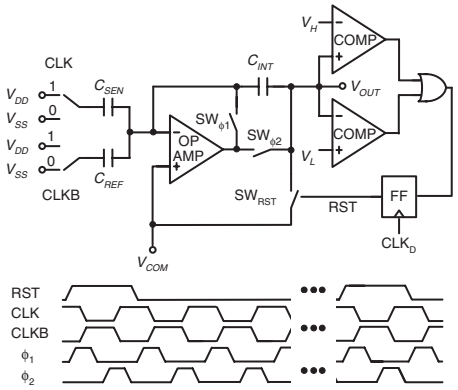

Fig. 1 *Schematic and timing diagram of proposed CFC*

Circuit design: A schematic drawing and timing diagram of the proposed CFC circuit core are shown in Fig. 1. The reference capacitor C_{REF} and the sensing capacitor C_{SEN} are connected to the negative input of the opamp, and driven by the differential charge-pumping clocks CLK and CLKB. The presence of $SW_{ø1}$ makes the circuit around the opamp unity gain, maintaining the bottom electrodes of C_{REF} and C_{SEN} at the common voltage level V_{COM}. $SW_{ø2}$ creates an integrator which transfers charge to the integrating capacitor C_{INT}. The circuit operates in three phases as follows:

(i) Reset phase: At the beginning of a new cycle, $SW_{ø1}$ and SW_{RST} are switched on to discharge C_{INT} completely. Now the output voltage V_{OUT} can go up or down depending on the sign of the differential capacitance.
(ii) Pump-in phase: $SW_{ø2}$ is turned on and CLK goes up while CLKB goes down. In this phase, charge corresponding to the difference between C_{REF} and C_{SEN} is transferred and then integrated by C_{INT}. The extent of the change in V_{OUT} during this phase can be expressed as follows:

$$\Delta V_{OUT} = \frac{(C_{SEN} - C_{REF})V_{DD}}{C_{INT}} = \frac{\Delta C V_{DD}}{C_{INT}} \quad (1)$$

(iii) Toggle phase: $SW_{ø1}$ is turned on and CLK goes down while CLKB goes up. C_{INT} is disconnected from the output, and thus the charge stored in C_{INT} is conserved.

Pump-in and toggle phases are repeated until V_{OUT} reaches a predefined upper threshold V_H or lower threshold V_L. At this point, the cycle is complete and a new cycle starts from the reset phase. This approach allows us to amplify the differential capacitance while averaging out noise.

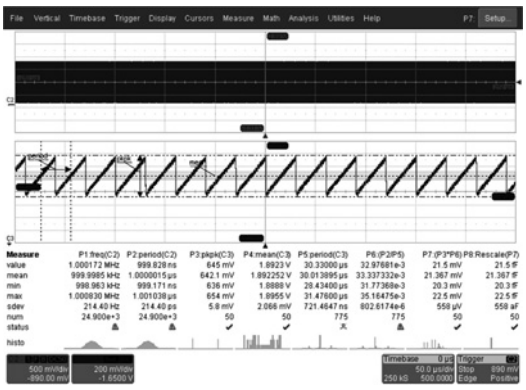

Fig. 2 *V_{OUT} measured at $\Delta C = +7.5$ fF*

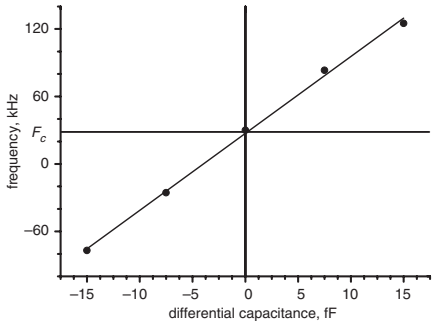

Fig. 3 *Measured output frequencies under varied differential capacitance ΔC, which ranges from −15 to +15 fF*

The differential capacitance is measured by comparing the frequency f_{OUT} of the triangular waveform generated by the CFC with the frequency of a reference clock as follows:

$$\Delta C = C_{INT} \times \frac{\sum_{k=1}^{n} \Delta V_{OUT}}{V_{DD}} \times n = C_{INT} \times \frac{V_{REF} - V_{COM}}{V_{DD}} \times \frac{f_{OUT}}{f_{CLK}} \quad (2)$$

where n is the number of clock cycles that pass during one cycle of the CFC. V_{REF} can be the upper threshold V_H or the lower threshold V_L, depending on the sign of the differential capacitance. The frequency of the RST pulse f_{RST} is the same as that of the triangular waveform produced by the CFC, allowing f_{RST} to be used as the 1-bit output pulse stream of the CFC.

Prototype design and experimental results: To demonstrate the feasibility of the proposed scheme, a prototype chip was designed and fabricated in 0.35 μm CMOS technology with a 3.3 V supply. A MEMS capacitive sensing device is monolithically integrated with our CMOS CFC circuit. The MEMS device was processed after the CMOS process was completed. Experimental results show that the integrated CFC circuit and MEMS capacitive sensing device operate at a clock frequency of 1 MHz and consume 660 μA at that speed. Fig. 2 shows the values of V_{OUT} produced by the converter circuit when measuring +7.5 fF of differential capacitance. Fig. 3 shows an excellent linearity, with a conversion gain of 6.8376 kHz/fF and a centre frequency of

27.148 kHz. Measurement outputs with negative signs are written as negative frequencies for convenience. Fig. 4 shows a microphotograph of our CFC circuit monolithically integrated with a differential MEMS capacitive sensing device on a single die.

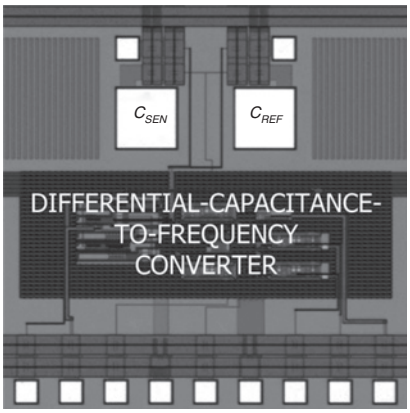

Fig. 4 *Die microphotograph of CFC monolithically integrated with differential capacitive sensing structure*

Conclusions: We propose a cost-effective CFC circuit that uses a small number of components. By accumulating the charges produced by repetitive charge integration, the difference between two capacitances can be converted to an output frequency with good linearity. Experimental results show that the circuit has a conversion gain of 6.8293 kHz/fF, which makes it possible to detect small changes in differential capacitance.

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