High-Speed 10-bit LCD Column Driver with a Split DAC and a Class-AB Output Buffer

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Abstract — *We propose a high-speed rail-to-rail 10-bit column driver with a reduced die area for LCD-TV applications. This column driver combines an 8-bit resistor-string digital-to-analog converter (R-DAC), constructed using a hybrid-type decoder to reduce the RC time delay and die area, with a 2-bit interpolation DAC. In the output buffer, error amplifiers drive a column line so as to realize a high-speed rail-to-rail drive. Gamma-corrected output voltages are generated by the resistor string of R-DAC, which contains resistors of unequal values that match the inverse of the liquid crystal transmittance-voltage characteristic. A prototype 10-bit LCD column driver was designed and fabricated using a 0.3μm CMOS technology, and has a settling time of within 2μs and a quiescent current of 5.4μA per channel.*[1]

Index Terms — LCD driver IC, DAC, gamma correction, class-AB.

I. Introduction

Liquid crystal displays (LCDs) have recently become the dominant type of flat-panel display, and have effectively replaced cathode-ray tubes. The wide range of applications for LCDs includes cellular phones, personal digital assistants, notebooks, monitors and digital TVs. Grayscale resolution required in an LCD depends on its application, and ranges from simple black and white to 6, 8 and 10 bits of color. While mobile devices such as cellular phones, personal digital assistants and notebooks only require 6 bits (yielding around 260k colors), high-end monitors require 8 bits (16.7 million colors); and the trend for TVs is towards 10 bits (a billion colors) [1]-[3]. Liquid crystal display television (LCD-TV) is evolving rapidly, leading to a large and growing demand for high-resolution, high-color-depth driver ICs [4], [5].

As well as a display panel, an LCD system requires a driver circuit which is able to support the required color depth and resolution. A display panel contains a number of switching devices, arranged in a matrix; these devices are driven by a driver circuit, which includes timing controller, reference source, column driver and scan driver. Column driver circuit is particularly important in a high-quality display. For LCD-TV applications, this circuit should be able to process 10-bit digital input codes and then convert them into analog voltages [6]. Column driver circuit generally includes shift registers, input registers, data latches, level shifters, digital-to-analog converters (DACs) and output buffers.

Transmittance of a liquid crystal exhibits a non-linear relationship to the applied voltage. To obtain a linear luminance output from an LCD in response to a digital input, the output of DAC is usually designed to be the inversion of the liquid crystal transmittance-voltage characteristic. That is, intervals between increments in voltage must be adjusted to compensate for non-linearity of the characteristic curve. This adjustment is called gamma correction. In order to implement a non-linear DAC, certain gamma voltages are applied to a resistor string which is made up of resistors of unequal values, selected to produce required curve. A single resistor string supplies reference voltages to all channels, but each channel needs its own decoder, to route the reference voltage supplied by resistor string to the corresponding output buffer. The die area of the routing lines used to connect resistor string and decoders is considerable and, together with decoders, will occupy a large percentage of the area of the column driver IC. This requirement is compounded when an R-DAC is uprated from 8 to 10 bits of color, which requires a fourfold increase in the size of decoder, leading to substantial growth in size of column driver die. This makes a high-resolution column driver costly and challenging to implement.

In order to drive column lines of an LCD panel, an output buffer is needed for each channel. These output buffers, which are usually made up of operational amplifiers, have to drive highly capacitive column lines. In general, hundreds of output buffer amplifiers need to be built into a single chip, so each buffer should occupy as small a die area as possible, and its static power consumption needs to be low. The output buffer also has to approach rail-to-rail voltage driving in order to accommodate the higher gray levels. In addition, settling time needs to be shorter than horizontal scanning time. Output buffers determine power consumption, voltage swing and settling time of the column drivers [7], and are therefore critical components.

In this paper, we show how die area can be reduced by replacing a conventional 10-bit R-DAC with a split architecture comprising an 8-bit R-DAC and a 2-bit interpolation DAC. We also propose the use of a hybrid-type decoder for 8-bit R-DAC, in order to reduce RC time delay, as well as in making a further saving in die area. Additionally, we present a high-speed output buffer circuit suitable for large

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LCD panels with a large input dynamic range and output swing, but a low quiescent power requirement.

The remainder of this paper has four sections. Section II provides an overview of the conventional architecture of a column driver. Section III describes our new column driver architecture. In Section IV, we present measured results from an experimental prototype column driver, designed and fabricated using a 0.3μm CMOS technology. Section V concludes the paper and summarizes the potential benefits of our approach.

II. CONVENTIONAL COLUMN DRIVERS

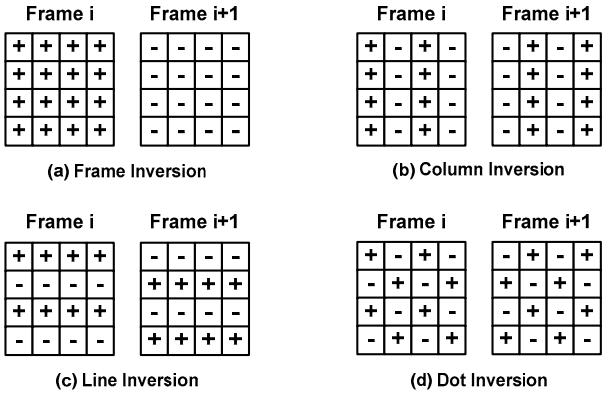

Fig. 1. Pixel inversion methods.

Column drivers consume a great deal of power because they drive thousands of highly capacitive column lines and use high driving voltages. Recent designs of LCD column drivers have therefore been focused on reducing their power consumption while maintaining high image quality [7]. The liquid crystal cells of LCD panels are driven by an AC voltage that alternates between positive and negative polarities with respect to the common backside electrode. This inversion technique, which has the advantage of increasing the lifetime of the liquid crystal material, has four variations: frame, line, column, and dot inversion. Figure 1 shows how these inversion methods are organized. In frame inversion method, the driving signals applied to the cells of the LCD cause all the pixels to have the same polarity during a frame period. At the next frame period, the polarity of all the pixels is inverted, as shown in Fig. 1 (a). Figs. 1 (b) and (c) show column and line inversion, in which the driving signals are applied to the cells in the LCD in such a manner that each pixel in the same column or row (i.e. a signal line or a scanning line) has the same polarity during each frame period, and each pixel in the adjacent column or row has the opposite polarity. During the next frame, the polarity of each pixel is inverted. Both frame and line inversions require the voltage swing of the column driver to be equal to the LC drive voltage. The arrangement for the fourth method, dot inversion, is shown in Fig. 1 (d). In this case, driving signals of opposite polarity are applied in a checker-board pattern, which is inverted at every frame period. This pattern effectively cancels both horizontal and vertical crosstalk, and therefore it is preferred in premium displays. The drawback of dot inversion method is that it dissipates more power because it requires twice the driving voltage required by the other methods [2], [4], [8].

A conventional column driver is composed of shift registers, input registers, data latches, level shifters, DACs, and output buffers. Its architecture is shown in Fig. 2. Basic function of the column driver is to transmit data signals from the external controller to each pixel. Shift registers generate an output from SET signal, which is synchronized by CLK signal. Incoming data signals are applied to the RGB input and sampled into the input registers. Then, the data saved in input registers are transmitted to data latches as EN signal. A wide data latch presents one row at a time of the serial input pixel data to the input of the level-shifters, which boost the digital signals. DAC converts these signals to the corresponding analog voltage levels. These voltages are fed to the output buffers, which are able to drive highly capacitive column lines.

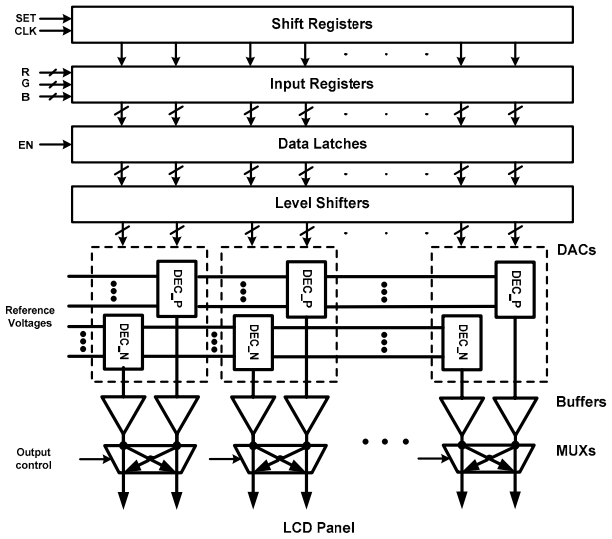

Fig. 2. Block diagram of a conventional column driver showing the data driving scheme in detail.

Figure 2 also shows the driving scheme. Operations of each polarity take different paths. Odd-numbered DACs and buffers form the path for negative-polarity operations, and even DACs and buffers form the path for operations of positive polarity. When odd column lines have negative polarity and even lines have positive polarity, input codes and output buffers are in their normal order. When polarities of the column lines are changed, the order of input codes and output buffers is reversed. However, PMOS input buffers and odd DACs continue to generate negative-polarity operations while NMOS input buffers and even DACs handle positive polarity operations. This achieves high-speed and rail-to-rail driving, while allowing the number of bits in each DAC to be reduced by one. It also means that two paths are required to drive column lines [2], [4].

Gamma correction of digital data is part of its conversion to the analog voltage that drives display. This is generally

performed by an R-DAC in column driver. Figure 3 shows a conventional R-DAC architecture in which an M-bit DAC is realized as a string of resistors and a matrix of MOS switches. Resistors are connected in series between high and low reference voltages, creating tap-points between successive resistors that can be selectively switched to one out of the many output lines, as specified by M-bit input word. Because the output is the voltage at a tap-point, analog representation of the digital input is inherently monotonic and accurate. However, for high-resolution applications, an R-DAC has several drawbacks. First, the number of the resistors and switches grows exponentially with the number of bits, causing a longer RC delay at the output. Second, the die area of the routing lines which are used to connect resistor string and decoders also increases rapidly. This makes an R-DAC impractical when the number of bits is too large.

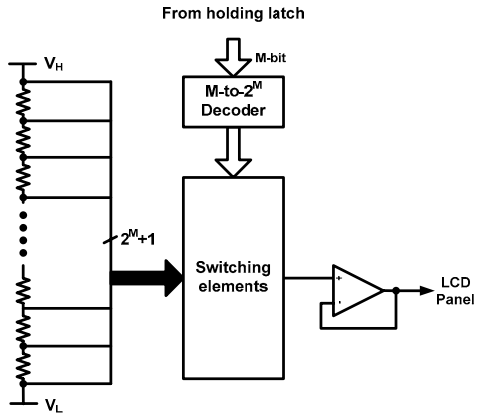

Fig. 3. Conventional resistor-string DAC.

The main purpose of output buffers is to deliver an adequate signal power to drive the highly capacitive column lines of display panel with an acceptably low level of distortion. In addition, efficient output buffers must combine a high maximum output current with a low quiescent current [9], [10]. A class-AB output buffer achieves a good compromise between signal distortion and quiescent current, and is usually used in column drivers. An adequately designed class-AB output buffer allows gate-to-source voltage of the output transistors to approach that of the supply rails [11], [12]. Due to hundreds of channels built into a single chip, it is very desirable to reduce die area and static power consumption of DACs and output buffers, especially in displays with a large color depth.

III. Proposed Column Driver

A. Architecture

Figure 4 is a block diagram of our column driver architecture. Its digital block consists of shift registers and sampling and holding latches, which sample incoming digital video signals. Exchange blocks perform the inversions. Split DACs are used to convert the digital video into analog voltage: this arrangement takes advantage of the inherent monotonicity of voltage-division DACs, while keeping the number of resistors manageable. An 8-bit resistor-string DAC is combined with a 2-bit interpolation DAC. The output of the interpolation DAC is buffered by a class-AB output buffer, which is made up of two error amplifiers and a pair of pull-up and pull-down transistors.

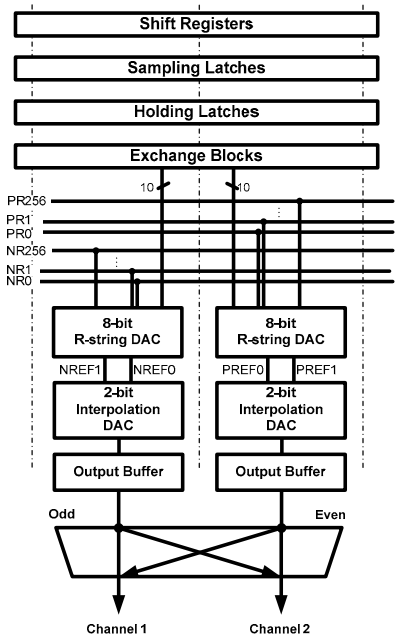

Fig. 4. Block diagram of a 10-bit column driver with a split architecture.

B. 10-bit digital-to-analog converter

The area of DAC is the most important issue in the implementation of high-resolution grayscale driver. As we have already pointed out, the number of resistors and switches in R-DAC grows exponentially with the word length, making a single-stage DAC impractical for a large number of bits. A two-stage R-DAC, consisting of two resistor-strings isolated by unity-gain buffers, seems to offer a way forward; but process variations in the unity-gain buffers can lead to random offset errors. This problem can be overcome by omitting unity-gain buffers, but this would require resistors in the second-stage resistor-string to have sufficiently large values to avoid affecting the voltage produced by the first-stage resistor-string when the two are connected in parallel. These large values are bound to increase the area of the DAC to some extent [3]. In our split architecture, the DAC is made up of an 8-bit R-DAC, which includes decoding logic, coupled to a 2-bit interpolation DAC. Decoding logic selects the two neighboring voltage levels specified by the sub-word containing eight most significant bits, and 2-bit interpolation DAC generates the final analog output signal by interpolating between these two voltages, as specified by the sub-word containing two least significant bits.

The concept underlying decoder-based DACs is illustrated in Fig. 5. In a tree-type decoder, switch matrix has the form of a tree structure, which eliminates the need for a digital decoder. This requires 2^{M+1}-2 switches for an M-bit converter. Figure 5 (a) shows how selected voltage propagates through M levels of switches before arriving at the buffer amplifier, which is necessary to provide a low-impedance output to the external load. Provided that DC offset voltage of the buffer does not affect common-mode voltage at the input, digital-to-analog conversion is sufficiently monotonic to support a resolution of 10 bits. However, as the number of bits increases, switch network imposes a serious delay. Resistor string may also cause delay; and its output impedance varies as a function of the number of closed switches in the network. For high-speed applications, tree-type decoder is therefore superseded by digital-type decoder shown in Fig. 5 (b). In this arrangement, common node of all the switches is directly connected to buffer amplifier. Even though the 2^M transistor junctions produce a large capacitive load, selected voltage only propagates through a single switch, so that DAC can operate more quickly. Nevertheless, logic circuit of an M-to-2^M decoder takes up a large area.

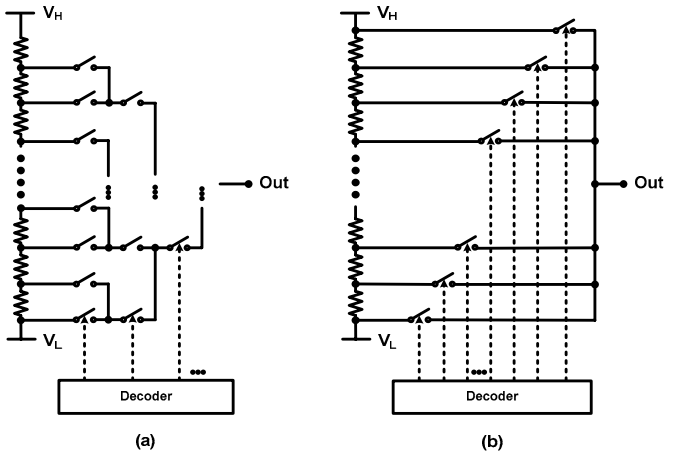

Fig. 5. Decoder-based DAC with (a) tree-type decoder and (b) digital-type decoder.

The number of switches in both of these decoder-based DACs still increases exponentially with the number of bits in the digital input, so that area constraints inevitably limit the number of bits of the digital input. In other words, an M-bit R-DAC with a digital-type decoder needs 2^M+1 switching elements or 2^{M+1} switching elements if it has a tree-type decoder. In terms of speed, RC time delay in the switch network is the dominant constraint on the R-DACs. This delay can be reduced by decreasing the number of transistors in the signal path or by making transistors wider. However, this requires additional logic circuits, and a trade-off between RC time delay and the number of these logic circuits is unavoidable. A compromise may be obtained by the use of a hybrid-type decoder such as the one shown in Fig. 6. This combines three types of decoders: a 3-bit digital-type decoder block, a 3-bit tree-type decoder block, and a 2-bit tree-type decoder block. This hybrid decoder requires 2^M+3•2^{N-J}+2^{K+1} switching elements are needed, where M is the number of bits of the digital input, J is the number of bits in the first decoder block, and K is the number of bits in the last decoder block. This arrangement requires fewer switching elements and logic circuits than conventional architecture.

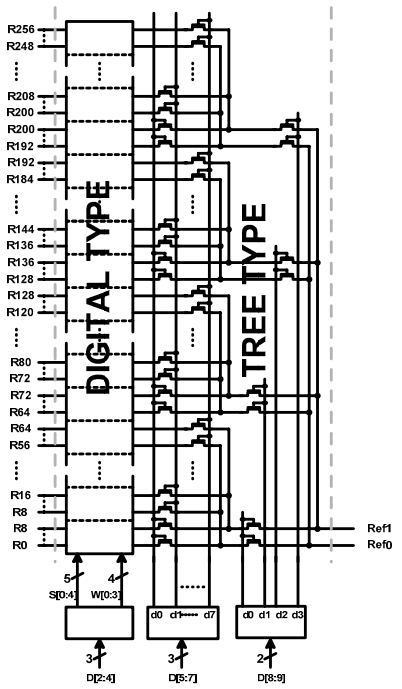

Fig. 6. 8-bit resistor-string DAC implemented using a hybrid-type decoder.

Figure 7 shows the split-DAC architecture. The 8-bit R-DAC, which is itself controlled by D<9:2>, produces two outputs, REF0 and REF1, and 2-bit interpolation DAC performs fine interpolation between them. Interpolation DAC consists of an XOR & Decoder block, four differential input stages and a differential trans-conductance stage. In the XOR & Decoder block, each bit of D<1:0> is XORed with D<2> and the resulting word is transformed into the thermometer code S<3:1>, which increases the value of S<3>. At this time, S<0> is equal to D<2>, and the value of S<3:0> represents the weight of REF1 for interpolation. When D<2> is low, REF0 is closer than REF1 to the output voltage for the all-zero input D<9:0>, and the weight of REF1 increases from 0 as the value of D<1:0> increases. Conversely, when D<2> is high, REF1 is closer to the all-zero output voltage, and the weight of REF1 decreases from 4, so that the weight of REF0 increases from 0. This scheme allows us to interpolate a selected interval between REF0 and REF1 monotonically, without missing any output levels. Each bit of S<3:0> and its inverse has its own differential stage, including a pair of switching transistors which is controlled by that bit. The differential stage has three input transistors of the same size with a common source terminal, which is also connected to a

separate tail current source for each differential trans-conductance stage, to improve the linearity. One of input transistors has its gate coupled to REF1 and its drain connected to the negative input terminal of the differential current summing stage via a switching transistor controlled by one bit of S<3:0>. Another input transistor has its gate coupled to REF0 and its drain connected to the negative input terminal of the differential trans-conductance stage via the other switching transistor.

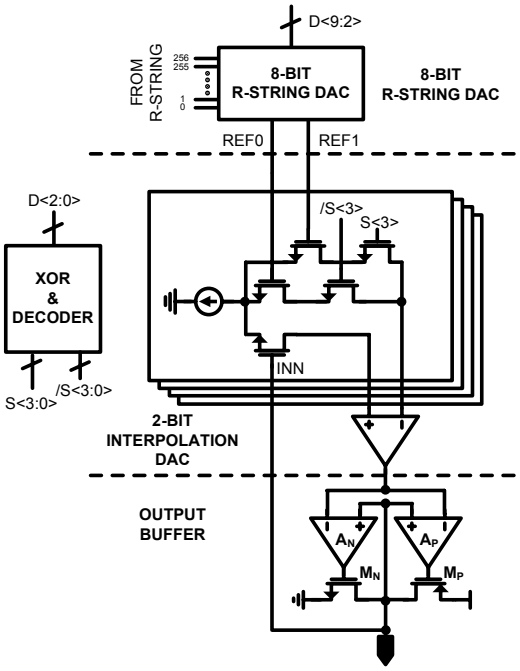

Fig. 7. Split-DAC architecture and output buffer.

C. Output buffer

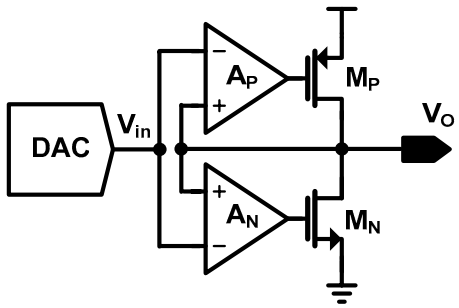

Fig. 8. Simplified diagram of the output buffer.

The driving capability of an output buffer can be improved by increasing the sizes of its output transistors. However, this will increase quiescent current and total power consumption. Another approach is to use a class-AB push-pull output stage as illustrated in Fig. 8. Two large common-source output transistors M_P and M_N are driven by two error amplifiers, A_P and A_N. Feedback loop around A_P (A_N) and M_P (M_N) ensures low output impedance. Error amplifiers must have a low open-loop gain, of the order of 10, because they have an input-referred DC offset voltage of several mVs. If this gain were not reduced, the referral of the offset from the input to the output would cause unacceptable variations of the quiescent currents in M_P and M_N. Additionally, broadband amplifiers are required to prevent crossover distortion [13]-[15]. The circuit diagram of a negative-half amplifier is shown in Fig. 9, and a positive-half amplifier is the complement of this. The output buffer contains a simple differential amplifier with an unbalanced current mirror (M_3, M_4) and a diode-connected transistor (M_5) that limits its gain. Assuming that output resistances of the transistors are high, gain of the amplifier can be found as follows:

$$A = \frac{g_{m,pmos}}{g_{m,nmos}} \cdot \left(\frac{1}{\alpha} - \frac{1}{2} \right), \tag{1}$$

where $g_{m,pmos}$ and $g_{m,nmos}$ are trans-conductance values of the transistors M_1 (or M_2) and M_3, respectively, and α is the split factor of the mirror and the diode-connected transistor. This equation shows clearly that the gain is limited and controlled by α.

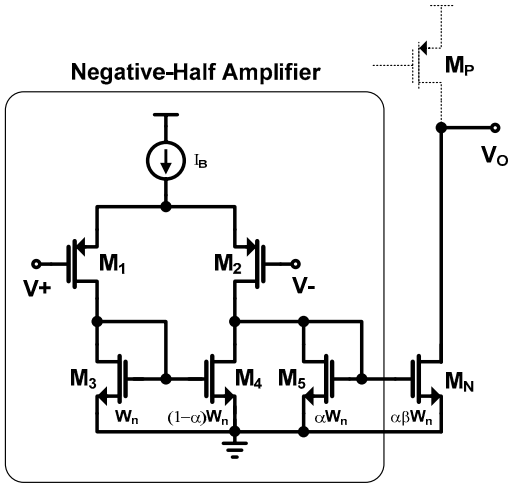

Fig. 9. Negative-half error amplifier of the output buffer.

In general, the distortion of output signal is reduced in proportion to quiescent current of the output buffer, but power consumption is inversely proportional to quiescent current, making a compromise necessary. The quiescent current is determined by the ratio between load transistor of error amplifier and output transistor. Assuming that drain currents through M_1 and M_2 are $\frac{I_B}{2}$, quiescent current can be expressed as follows:

$$I_q = \alpha \cdot \beta \cdot \left(\frac{I_B}{2} \right), \tag{2}$$

where I_B is bias current of the amplifier, and β is the ratio of M_N to M_5. Thus, quiescent current can be reduced to any desired value by adjusting transistor ratio of M_3~M_5 and M_N.

The stability of this buffer can be verified by calculating open-loop transfer function of a negative half-circuit, as the buffer operates symmetrically.

IV. Experimental Results

Fig. 10. Die photograph of the proposed column driver.

Proposed 10-bit column driver was fabricated using 0.3μm LV-HV CMOS technology. Its performance has been investigated by means of an HSPICE simulation, and subsequently proved in silicon. A larger value of the load capacitance increases the phase margin, which is 53° even when the load capacitance is as low as 30pF. Therefore, no additional capacitors are needed for frequency compensation, which reduces the die area.

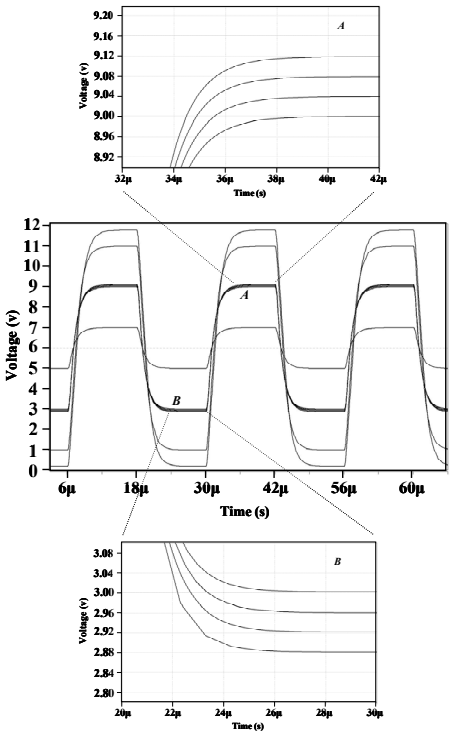

Fig. 11. Post-layout simulation results for the proposed 10-bit column driver including 2-bit interpolation DAC.

Due to the limited silicon area available, only eight channels of the column driver were built, and then tested on a printed circuit board. Figure 10 shows the microphotograph of one channel of our 10-bit column driver. Its active area, including digital control circuitry is 0.12mm^2. Column drivers use a low voltage of 3.3V for digital block and high voltage of 12V for DAC and output buffer block. Output voltages are determined by input data and 18 (= 9×2) external gamma-corrected power sources ($VGMA_1$ to $VGMA_{18}$). Input grayscale voltages of the same polarity with respect to common voltage are used for the nine gamma-corrected voltages $VGMA_1$ to $VGMA_9$, and the nine voltages from $VGMA_{10}$ to $VGMA_{18}$. Figure 11 shows the simulated channel output of a dot-inversion column driver with an RC load. The 2-bit interpolation DAC divides the applied voltage of 4mV into 4 levels. The results show the accuracy of 2-bit DAC output and an acceptably low RC delay in the current DAC. Figure 12 shows the measured output waveform of two neighboring channels. The applied load used a π3 model and consisted of a 10KΩ resistor and a 300pF capacitor. The output waveform was measured at the end-point of RC load. Voltage levels for negative polarities ranged from 1V to 5V, and while those for positive polarities were between 7V and 11V.

Fig. 12. Measured output waveform for the proposed column driver at the end node of RC load.

Figure 13 shows the measured gamma-corrected transfer curve of the DAC with its output buffer.

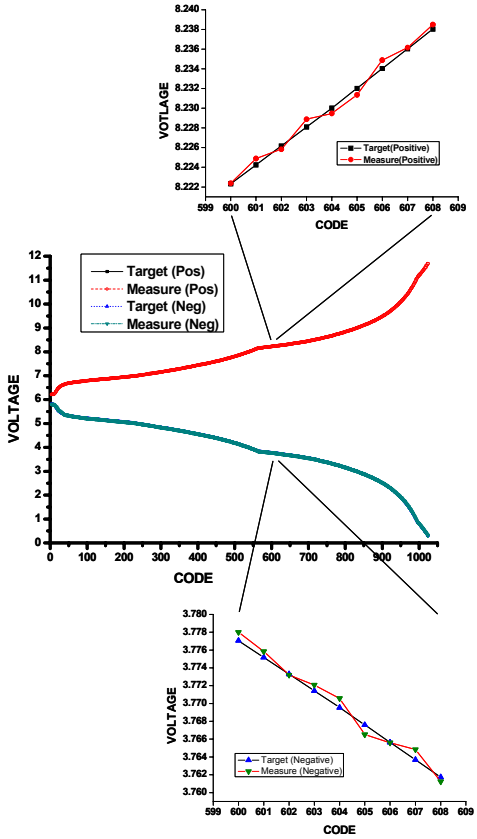

Fig. 13. Measured transfer curve for the proposed 10-bit column driver.

Voltages between 6V and 0.2V correspond to negative polarity, while those from 6V to 11.8V correspond to positive polarity. At the input node of RC load, the times for the output to settle within 0.2% (0.5 LSB) of the final voltage were 1.8 and 2μs, for rising and falling edges respectively. Differential nonlinearity and integral nonlinearity are measurements typically used to characterize a DAC. However, it is difficult to determine these two quantities for a nonlinear DAC. Instead, we used the differences between the calculated and measured output voltages, which were found to be within 4mV. The deviations are caused by the mismatch between the resistors in the DAC and the offset voltage of the amplifiers. The column driver for positive polarity consumes a quiescent current of 5.2μA, and the driver for negative polarity consumes 5.4μA. The measured performance of the prototype is summarized in Table I.

TABLE I

Process	**0.3μm LV-HV CMOS(1P3M)**
Resolution	**10 bit**
Supply Voltage	**3.3V(LV), 12V(HV)**
Output Dynamic Range	**0.2V to 11.8V**
Quiescent Current per channel	**5.2μA (Positive) 5.4μA (Negative)**
Settling Time	**2 μs for R_L=10kΩ, C_L=300pF**
Maximum deviation	**4mV**

V. Conclusion

We have presented a high-speed rail-to-rail column driver that is suitable for driving the large column line capacitance found in LCD TVs. An 8-bit resistor-string DAC was combined with a 2-bit LSB interpolation DAC to reduce the number of switching elements and the die area compared to a conventional 10-bit DAC. A further reduction in the die area was achieved by mixing digital and tree-type decoders within the 8-bit resistor-string DAC. Gamma correction voltages are applied to the resistor string of the R-DAC, and the unequal resistor values fit the inverse of the liquid crystal transmittance-voltage characteristic. The driving capabilities were improved by the use of error amplifiers with a particularly low quiescent current. Prototype column drivers were implemented in 0.3μm LV-HV CMOS technology. The combination of the reduced circuit loading and die area with an increased slew-rate confirms the suitability of the proposed column driver for large flat-panel displays.

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