Differential Capacitance-to-Digital Converter Utilizing Time-Domain Manipulation of Intermediate Signals

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***Abstract*—To achieve high-resolution in electrically noisy environments as well as low-power, we propose a differential capacitance-to-digital converter (CDC) that utilizes three-level time-domain manipulation of intermediate signals. The proposed CDC, designed in 0.35µm digital CMOS technology and simulated with HSPICE, achieves a 9-bit resolution at the power supply of 3.3V with the superimposition of 600mVpp 2.5 kHz square-wave noise disturbance, consuming the average power of 158.3µW/sample.**

I. INTRODUCTION

Significant attention has recently been paid to chemo-mechanical transduction of chemical and biomedical events, because these techniques can achieve high specificity and label-free assays. For instance, microcantilever techniques are widely used, and mostly involve optical detection. However, optical approaches are too bulky and costly to build into a compact device. In addition, optical detection is ineffective in opaque solutions. To solve these problems, thin-membrane transducer (TMT) [1], which is a type of differential capacitive sensors, has been recently introduced.

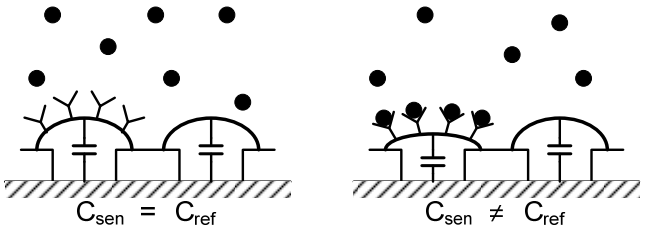

Figure 1. A pair of thin membrane transducers (TMTs).

The TMT provides highly sensitive capacitive detection and also avoids design constraints for metal-oxide semiconductor field effect transistor (MOSFET). As shown in Fig. 1, a bio-molecular reaction induces tensile and compressive stresses in a TMT, making its dome shape flatter or more rounded, which in turn alters its capacitance, C_{sen}. Fig. 1 also shows that there is a second TMT structure, C_{ref}, which is not sensitized to the target event, can be used to compensate for spurious deflection of the dome caused by environmental change.

In this paper, we propose a moderately high-resolution capacitance-to-digital converter (CDC) for the readout of differential capacitance in these kinds of applications. Our CDC is composed of two main parts. One is a differential capacitance-to-time converter (CTC) which converts differential capacitance to a time interval, and the other is a time-to-digital converter (TDC), which converts the CTC output to a digital code, using time splitter, chopper, and stretcher circuits.

Most conventional capacitance-to-digital converters (CDCs) generate a voltage as an intermediate signal that corresponds to the capacitance being measured, and then digitize it using an analog-to-digital converter (ADC); this type of IC has high signal-to-noise ratio and sensitivity [2]. However, as the supply voltage scales down in conventional CDC circuits, some critical shortcomings occur. One of these problems is that voltage references become easily unstable in the environment noise such as supply voltage fluctuations, so that quantization of voltage is less accurate [3]. But we use a time interval instead of a voltage as an intermediate signal of our CDC and manipulate it in three different manners. This can be measured more accurately and is less affected by the noise.

II. DIFFERENTIAL CAPACITANCE-TO-TIME CONVERTER

Our CDC circuit is composed of a differential capacitance-to-time converter (CTC) and a time-to-digital converter (TDC). As shown in Fig. 2 the difference in capacitance between the sensor capacitor and the reference capacitor generates sign, the start and stop signals. The sign indicates whether the sensor or the reference capacitor have larger capacitance. The time difference between the start and the stop signals is digitized by the TDC, generating digital code (D_{out}); in the content of the sign signal, this represent the difference in capacitance that we are trying to measure.

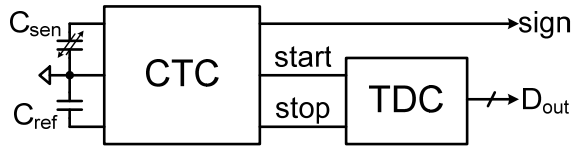

Figure 2. Block diagram of the capacitance-to-digital converter (CDC), which consists of differential capacitance-to-time converter (CTC) and a time-to-digital converter (TDC) [4].

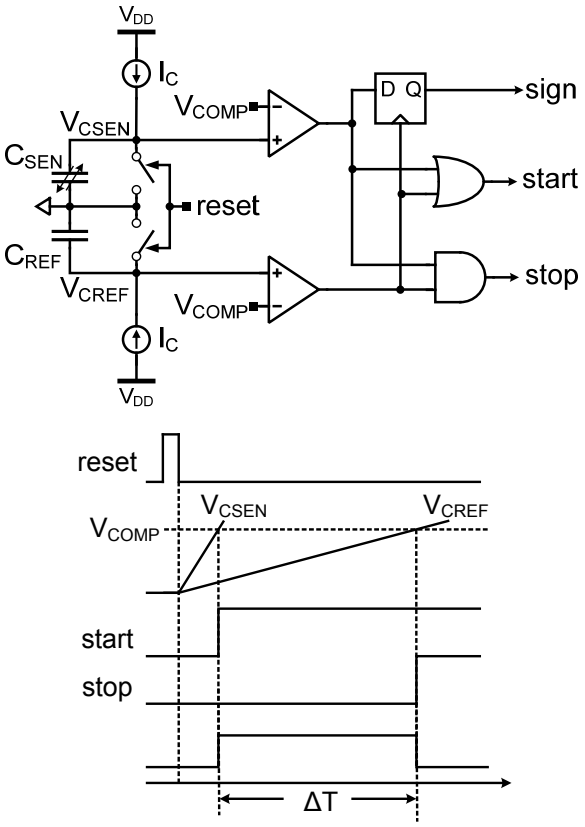

Figure 3. Architecture and timing of differential capacitance-to-time converter.

Our CTC as shown in Fig. 3, measures the difference between the capacitance of a reference and sensing capacitor, C_{REF} and C_{SEN}. The circuit converts differential capacitance into two signals which delineate a time interval.

Initially, the capacitances of both the reference and sensing capacitors are completely discharged by reset switches. Then, twin constant-current sources supply a current I_C to C_{REF} and C_{SEN}. The corresponding voltages V_{CSEN} and V_{CREF} then increase until they reach the comparator reference voltage V_{COMP}. The successive outputs of each comparator form start and stop signals, which delimit a time interval ΔT. This is proportional to the differential capacitance ΔC, as indicated in the equation below:

$$\Delta T = \left(\frac{V_{COMP}}{I_C} \right) \times \Delta C \,, \qquad (1)$$

$$\text{where } \Delta C = \left| C_{SEN} - C_{REF} \right| . \qquad (2)$$

The output of the D flip-flop provides a signal which indicates temporal order of the two comparator outputs.

III. Time-to-Digital Converter

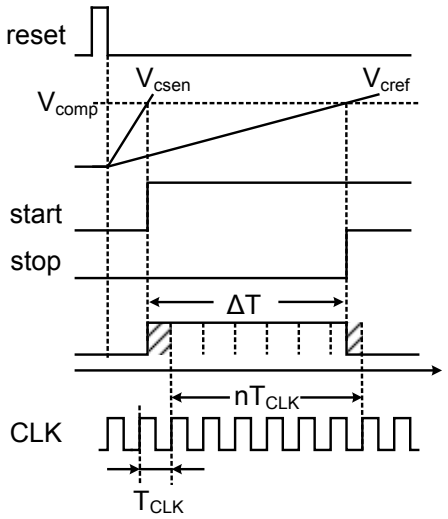

Figure 4. Quantization error of a single counter-based TDC ($\Delta T \neq nT_{CLK}$).

The time interval from the CTC circuit is needed to be converted to a digital code. This can be performed by a single counter [5], but this approach suffers from significant quantization error, as illustrated in Fig. 4 [6, 7]. One possible solution to this problem is to use a higher clock frequency for the counter. But this is far from entirely satisfactory. For one thing, there is an inherent bound on this frequency; and, for another, an increased clock frequency requires more power. Instead, we use an alternative TDC architecture which employs time splitter, chopper, and stretchers. This can achieve high resolution and low quantization error without increasing clock frequency.

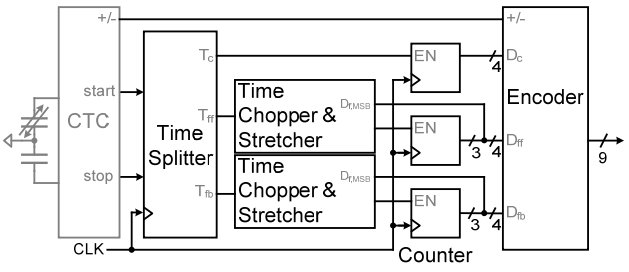

Figure 5. Proposed differential capacitance-to-digital converter.

The TDC is shown in Fig. 5. It consists of a time-splitter, a 4-bit coarse counter, two time-choppers, two time-stretchers, two 3-bit fine counters, and an encoder. The start and stop signals arrive at the inputs of the TDC, and the time-splitter use the rising clock edge to split the interval that they delimit

into three parts: a front fine time T_{ff}, a coarse time T_c, and a back fine time T_{fb}. The coarse 4-bit counter digitizes the synchronized coarse time T_c to D_c.

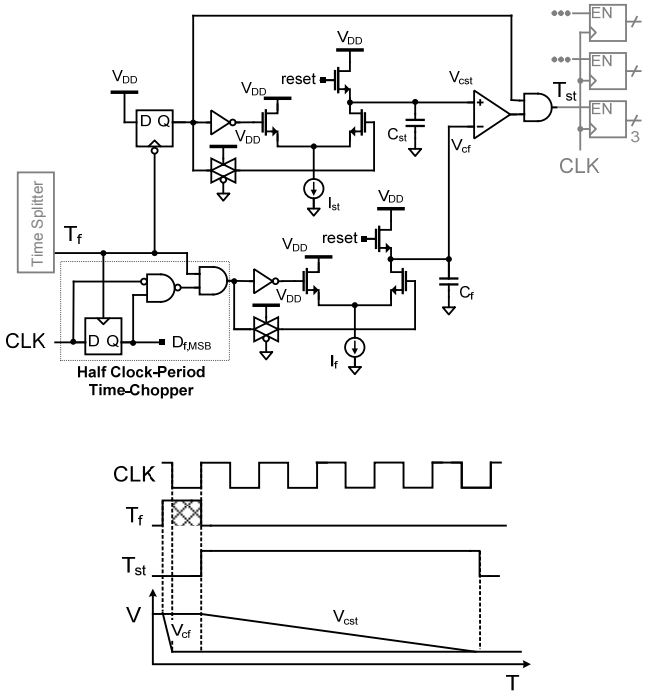

Figure 6. Architecture and timing diagram of proposed time-stretcher including half-clock-period time-chopper.

Each time-stretcher stretches a fine time interval, either T_{ff} or T_{fb}, by a stretching factor which is determined by the ratios between the current sources I_f and I_{st} and the capacitors C_f and C_{st} of the time-stretcher, as shown in Fig. 6. Both C_f and C_{st} are precharged during the initial stage of the stretching process. Then the half-clock-period time-chopper at the input of the time-stretcher determines the most significant bit of the fine data, $D_{f,MSB}$, before the fine time is stretched. Since the end of each period fine time T_f is synchronized with the rising clock edge by the time-splitter, it can be determined whether the most significant bit of the fine data $D_{f,MSB}$ is high or low with the help of the clock level. If $D_{f,MSB}$ is high, the half-clock-period time-chopper subtracts half a clock period from the fine time T_f; otherwise it leaves the fine time T_f unchanged. The processed fine time is then amplified by the final stage of the time-stretcher.

During the processing of fine time, the capacitor C_f discharges by the fine current source I_f. At the end of the process, I_f stops discharging the fine capacitor, C_f, at which point the voltage across the fine capacitor, V_f, is reduced by ΔV. At the end of the fine time T_f, the output of the negative-edge-triggered D flip-flop turns on the stretching current source I_{st}, in order to discharge the stretching capacitor C_{st}. The stretched time T_{st} is the period from the end of the processing fine time up to the time at which the voltage across the stretching capacitor V_{st} is reduced by ΔV, which is the same as the voltage drop across the fine capacitor C_f. Stretching factor can be determined as follows:

$$\Delta V = \frac{I_f T_f}{C_f} = \frac{I_{st} T_{st}}{C_{st}}, \tag{3}$$

$$T_{st} = \left(\frac{I_f C_{st}}{C_f I_{st}} \right) T_f . \tag{4}$$

The stretched time T_{st} is converted to a digital code by a fine counter. Then, the TDC assembles the predicted bit $D_{f,MSB}$ with the stretched bits $D_{f,LSB}$s and manipulates the fine data, either D_{ff} or D_{fb}. In the encoder, the three components of the digital data, D_c, D_{ff} and D_{fb}, are combined as follows:

$$D_{out} = 2^4 D_c + (D_{ff} - D_{fb}) . \tag{5}$$

IV. Simulation Results

We designed and simulated the CDC in 0.35μm CMOS technology with a supply voltage of 3.3V. The components in the time-stretcher are sized as follows: I_f = 125nA, I_{st} = 31.25nA, C_f = 1pF, and C_{st} = 4pF. It corresponds to the stretching factor of 16.

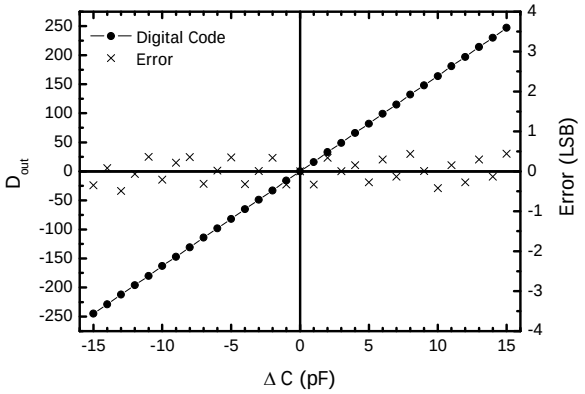

Figure 7. Linearity of the proposed CDC.

The time-chopper and stretcher can improve a resolution of 4 bits which is greater than that obtainable from a single counter running at the same frequency. In details, the half-clock-period time-chopper increases the resolution by 1 bit, and the time-stretcher itself adds a further 3 bits of resolution. If a conventional CDC without a time-chopper and stretcher operates at 1MHz clock frequency, which is 16 times higher, so as to achieve the same resolution as our CDC running at 62.5 kHz, it dissipates much more power. With a sensing capacitor C_{SEN} of 22pF, a conventional CDC using a single counter consumes 202.6μW per sample, whereas our circuit consumes 158.3μW per sample. Fig. 7 shows an excellent linearity when electrical noise in the form of a 600mV peak-to-peak 2.5 kHz square-wave is superimposed on the 3.3V power line voltage. The maximum error is -0.49/+0.44LSB. Our CDC is still able to digitize the value of a differential capacitance to 9 bits with a resolution of 61fF.

V. CONCLUSIONS

We have proposed the use of time-domain manipulation of intermediate signals, i.e. time-splitting/chopping/stretching techniques, to meet the power and resolution requirements of the capacitance-to-digital conversion in electrically noisy environments. HSPICE simulation results show that our circuit, operating at the clock frequency of 62.5 kHz with a 3.3V power supply, provides a 9-bit resolution with an average power consumption of 158.3μW.

ACKNOWLEDGMENT

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