Neural Recording System with Low-Noise Analog Front-End and Comparator-Based Cyclic ADC

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ABSTRACT

This paper describes a low-noise neural recording integrated circuit composed of a low-noise analog front-end (AFE) and a low-power analog-to-digital converter (ADC). The AFE amplifies biopotentials and the ADC converts input signal to digital output. The AFE exhibits 53.4dB of mid-band gain, 38.8Hz–10.6kHz of –3dB bandwidth. Total input referred noise (IRN) of AFE is 10.8μVrms and noise efficiency factor (NEF) is 8.1. The ADC achieves 10bit resolution and operates at 2.5MS/s. The chip is fabricated and successfully tested in a 0.18μm CMOS process.

I. INTRODUCTION

In the past decade, neuroscientists and clinicians have researched to observe the behavior of biopotentials, and the demand for low-noise low-power neural recording system has grown dramatically [1], [2]. An implantable neural recording system may provide an effective way for the development of practical brain-machine-interface (BMI) systems or epileptic seizure detection [3], [4]. Table 1 shows the biological sources and its applications of each biopotentials [5].

The neural recording system should be entirely implanted under the skin to avoid the risk of infection. This impalntability restricts the size and power consumption of the system [6]. A heat flux of only 80mW/cm² can cause necrosis in muscle tissue, so the power dissipation should not exceed a few hundred milliwatts [7], [8]. Besides, since the neural signals from extracellular recording are very weak, 50–500μV, the input referred noise (IRN) of the analog front end (AFE) should be kept below the background noise level, 5–10μVrms, of the recording site [9], [10].

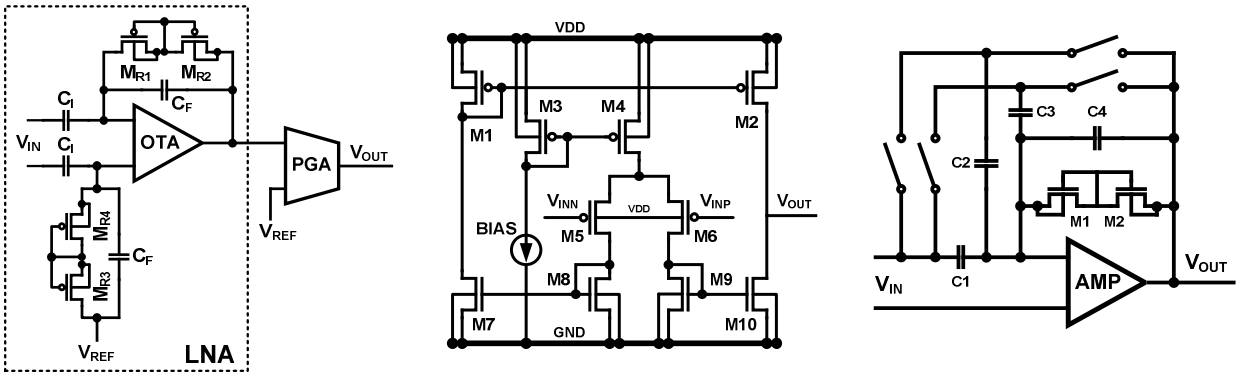
Table 1: Biological sources and applications of biopotentials

Biopotential	Biologic Source	Application
ECG	Heart	Cardiac monitoring
EEG	Brain	Sleep encephalography
EOG	Eye dipole field	Eye movement
EMG	Muscle	Diagnostic muscle activity

In this paper, we present a neural recording system for recording extracellular neural action potentials (ENAP) which consists of AFE and 10-bit cyclic analog-to-digital converter (ADC). This paper is organized as follows: In Section II, the architecture of the neural recording integrated circuit and the design of AFE and ADC are discussed in detail. In Section III, we present the measurement results of the system. In Section IV, we conclude the paper.

II. SYSTEM ARCHITECTURE

The neural recording integrated circuit consists of AFE and ADC. The neural signals are amplified by low-noise amplifier (LNA) with the mid-band gain of 46.4dB and the bandwidth of 45Hz–10kHz. Since the input range of the ADC is 500mV_{pp}, the programmable gain amplifier (PGA) is used to adjust the overall gain of the AFE in four steps: 7, 10, 15, 20dB. The ADC digitizes the amplified neural signal at a rate of 2.5MS/s with 10-bit resolution.



(a) (b) (c)

Figure 1: Schematic of the (a) AFE (b) current mirror OTA and (c) PGA

A. Analog Front-End

Fig. 1(a) shows the schematic of the AFE which consists of LNA and PGA. The LNA is designed as the capacitor feedback configuration similar to the topology in [4], [8], [11]. Capacitor feedback topology is easy to design and can get effective result in IRN compare with other LNA topologies. The mid-band gain of the LNA is set by C_I / C_F. To block the DC offset induced by the electrode-tissue interface, low high-pass cutoff frequency is required. The pMOS pseudo-resistors consisting of transistors $M_{R1} - M_{R2}$ and $M_{R3} - M_{R4}$ provide high resistance R_X, approximately $10^{12} - 10^{14}$ Ω. It creates low high-pass cutoff frequency with C_F. The high-pass cutoff frequency of the LNA is

$$f_H = \frac{1}{2\pi R_X C_F} \tag{1}$$

and it is inversely proportional to R_X. By using pMOS pseudo-resistors we can reduce the area. The low-pass cutoff frequency of the LNA is

$$f_L = \frac{1}{R_{out} C_L} \tag{2}$$

where C_L is the output load capacitance and R_{out} is the output load impedance. The loop gain $T(s)$ of the LNA can be approximated as

$$T(s) \cong \frac{\alpha G_m R_{out}}{1 + sR_{out} C_{L,tot}} \tag{3}$$

$$\left(\alpha = \frac{C_F}{C_F + C_I + C_P},\ C_{L,tot} = C_L + (1-\alpha) C_F \right)$$

by solving the KCL nodal equation, where C_p is the OTA input parasitic capacitance and G_m is the OTA transconductance. Assuming the DC loop gain is large enough, the transfer function of LNA can be approximated as

$$H(s) = -\frac{C_I}{C_F} \frac{1}{1 + s(C_{L,tot} / \alpha G_m)} \frac{sR_X C_F}{1 + sR_X C_F}. \tag{4}$$

The OTA of the LNA is designed using the current mirror OTA as shown in Fig. 1(b). The OTA is designed to achieve the mid-band gain of 46.4dB and the bandwidth of 45Hz–10kHz through simulation, considering that ENAP are typically in the range of 100Hz–10kHz [6].

As mentioned in Section I, low IRN of the LNA is essential to detect the neural signal. The IRN power spectral density (PSD) of the LNA can be derived as

$$\overline{v_{in}^2} = \frac{8kT}{3} \frac{1}{g_{m6}} \times \left[2 + \frac{4g_{m9}}{g_{m6}} + \frac{2g_{m4}}{g_{m6}} + \frac{2g_{m2}}{g_{m6}} \right] \times \Delta f \tag{5}$$

only considering thermal noise. As shown in (5), the IRN is inversely proportional to g_{m6}, where g_{m6} is the transconductance of the input pMOS transistor. Increasing the size of the input transistors decreases the IRN, but it also increases the area. The total IRN of the AFE is measured as

6.48 μVrms by integrating the IRN PSD from 1Hz to 10kHz through simulation.

The noise efficiency factor (NEF) in [12] indicates quantitative value of the tradeoff between power and noise. The NEF is derived as

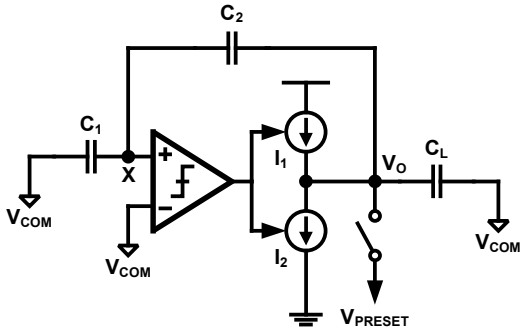
$$NEF = v_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \qquad (6)$$

where $V_{ni,rms}$ is the input referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier –3dB bandwidth. The bias current of the LNA is set to 4μA and the NEF of the AFE is 8.1.

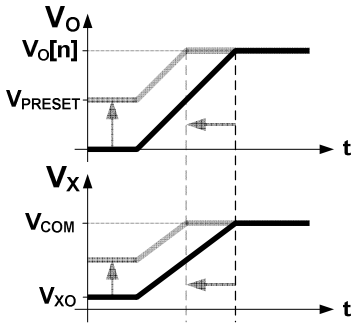
The PGA is designed using the band-pass configuration as shown in Fig. 1(c). The gain of the PGA is adjustable in four steps by using 2-bit control signals: 7, 10, 15, 20dB. The bandwidth of the PGA is 10Hz–30kHz. The AFE exhibits the mid-band gain of 54.1dB, when the PGA is set to the mid-band gain of 7dB, and the bandwidth of 45.4Hz–11.7kHz through simulation.

B. Analog-to-Digital Converter

An ADC is used to convert the amplified neural signals to digital signal that we can use it for further signal processing. Neural recording system requires high resolution, low power consumption and small area for ADC. In this paper a comparator-based cyclic ADC with boosted preset voltage is used as proposed in [13]. Since the cyclic ADC performs a conversion cyclically by repeated use of a single gain stage, it achieves high resolution with low power consumption and small area. As the CMOS technology scales down, the comparator-based switched-capacitor (CBSC) technique [14] achieves low power consumption compare with the opamp-based switched-capacitor technique by replacing the opamp with the combination of a comparator and a current source. Using CBSC technique is more energy efficient because while an opamp forces the virtual ground voltage during the entire charge transfer phase, the comparator detects the virtual ground voltage and triggers sampling. Fig. 2(a) shows the CBSC gain stage with boosted preset voltage scheme during the charge transfer phase. The charge transfer phase is divided into three sub-phases to achieve high accuracy and linearity. During the preset phase (P), conventional CBSC circuit shorts the output voltage (V_O) to ground during the preset phase to ensure that the V_X starts below V_{COM} . During the coarse charge transfer phase (E_1), fast and rough estimate of V_O and virtual ground condition is obtained. And during the fine coarse charge transfer phase, more accurate value of the V_O is obtained by using the fine phase current I_2 which has an opposite sign with the coarse phase current I_1 . Proposed CBSC circuit with boosted preset voltage scheme [13] operates different from conventional CBSC circuit during a preset phase. Fig. 2(b) shows the enhanced operation of the proposed circuit. To enhance the operation speed, the proposed circuit forces the proper voltage V_{PRESET} during a preset phase which ensures that the V_X starts slightly below V_{COM} . Boosting V_{PRESET} reduces the time required to obtain a rough estimate of V_O and virtual ground condition. Thus the proposed boosted preset voltage scheme [13] enhances the conversion rate without additional power. Fig. 2(c) shows the entire block diagram of the cyclic ADC.



(a)



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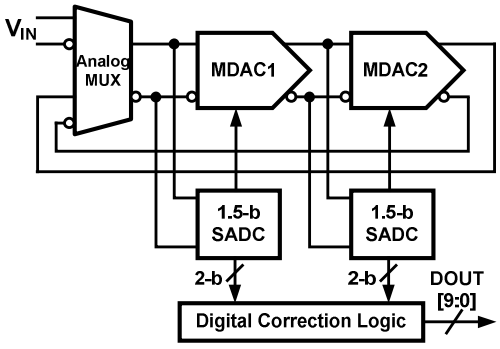


(c)

Figure 2: (a) CBSC with boosted preset voltage scheme (b) Enhanced transient response (c) Block diagram of the cyclic ADC

III. MESUREMENT RESULTS

The neural recording system is fabricated in 0.18µm CMOS process. The AFE and the ADC occupy area of 400µm x 350µm and 400µm x 880µm respectively. The layout of the system is shown in Fig. 3.

The AFE achieves the mid-band gain of 53.4dB, when the PGA is set to the lowest gain, and the bandwidth of 38.8Hz–10.6kHz. The output referred noise (ORN) spectrum is measured by Hewlett Packard 35670A, dynamic signal analyzer. The transfer function, the ORN spectrum and the IRN spectrum of the AFE are shown in Fig. 4(a), (b) and (c) respectively. The total IRN of 10.8µVrms is measured by integrating the area under the measured IRN spectrum from 1Hz to 10kHz. Fig. 5 shows the amplified neural signals recorded from the primary somatosensory cortex of a Sprague Dawley rat. Table 2 summarizes the performance of the overall system.

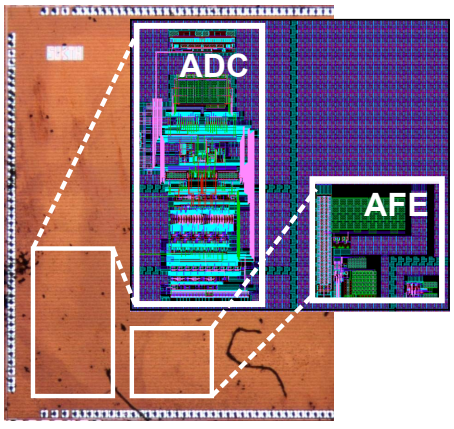
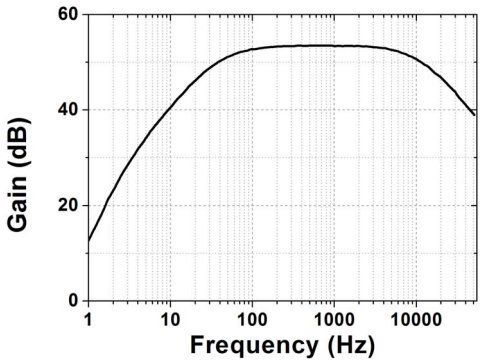
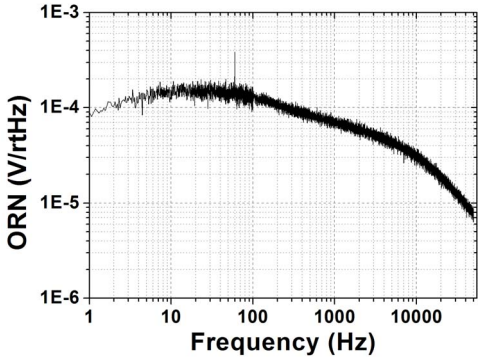


Figure 3: Die photo of the neural recording integrated circuit



(a)



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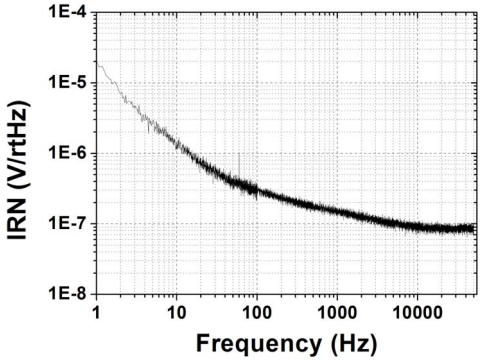

(c)

Figure 4: (a) Transfer function (b) ORN and (c) IRN of the AFE

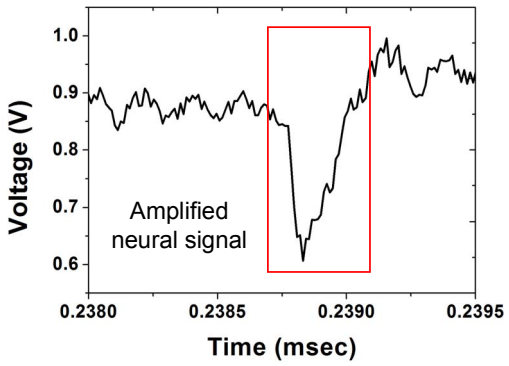

Figure 5: Measured neural signal from the primary somatosensory cortex of the Sprague Dawley rat.

Table 2: Performance summary

Parameter		Value
Supply voltage		1.8V
Technology		0.18um 1P6M CMOS
AFE	Mid-band gain	53.4dB
	Bandwidth	38.8Hz–10.6kHz
	IRN	10.8μVrms
	NEF	8.1
	Power consumption	22μW
	Area	0.101mm²
ADC	Sampling frequency	2.5MHz
	SNDR	55.99dB (fin=1.21MHz)
	SFDR	66.85dB (fin=1.21MHz)
	Power consumption	740μW
	Area	0.146mm²

IV. CONCLUSIONS

This paper presented the neural recording integrated circuit consists of AFE and 10-bit cyclic ADC. The capacitor feedback topology is utilized in the design of LNA. By adopting the CBSC technique to a cyclic ADC, we can achieve low power consumption. And the enhanced operation speed of the cyclic ADC by using boosted preset voltage scheme, the circuit can be used for multi channel neural recording system. The operation of the chip is successfully demonstrated by capturing neural signals from a Sprague Dawley rat's primary somatosensory cortex with proposed system.

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