A Low-Power Referenceless Clock and Data Recovery Circuit with Clock-Edge Modulation for Biomedical Sensor Applications

Sunkwon Kim, Jong-Kwan Woo, Woo-Yeol Shin, Gi-Moon Hong, Hyongmin Lee, Hyunjoong Lee, and Suhwan Kim
Electrical Engineering
Seoul National University
Seoul, Korea
{sunkwon.kim, jong-kwan.woo, woo-yeol.shin, gi-moon.hong, hyongmin.lee, Hyunjoong.lee, suhwan.kim}@amic.snu.ac.kr

Abstract—**This paper proposes a low-power referenceless clock and data recovery (CDR) circuit for biomedical devices or sensor applications. Its power consumption is reduced by adopting clock-edge modulation technique and using a voltage-controlled oscillator (VCO) based on a relaxation oscillator. Clock-edge modulation eliminates the need for an external reference clock without introducing the possibility of harmonic locking. Our CDR supports input data-rates between 200kbps and 10Mbps at 0.7V, and operate up to 24 MHz at 1.0V. The circuit is designed in a 0.18µm CMOS technology and consumes 8µW at an input data-rate of 10Mbps.**

Keywords - Clock and data recovery (CDR); relaxation oscillator; referenceless CDR; clock-edge modulation

I. INTRODUCTION

The design of high-performance biomedical devices such as sensors and implantable systems on a chip is continually improving, and play an important role in medical treatment [1]. Wireless biomedical devices must meet a number of requirements, affecting data rate, adequate power transfer, FCC compliance, size, minimal power consumption, and fabrication technology [2]. For example, 1000-site stimulating array requires 10-bit words for addressing at a 200Hz refresh-rate, this implies a minimum data-rate of 20Mbps [3]. The implanted unit requires small area to be minimally invasive, and a low power consumption to avoid tissue damage through heating effects. Fabrication costs should also be controlled by the use of a standard CMOS technology.

Inductive coupling is currently the most commonly used method of supplying power to those devices, and data is transmitted by RF telemetry. But an RF link has the disadvantage that its data-rate is effectively capped by interference from, and the need not to interfere excessively with, other devices. In a development designed to address this problem, a system receives both power and data by free-space optics. A prototype [4] includes an ultra-low-power CDR, which consumes 217nW at a 3b4b encoded input data-rate of 200kbps. However, a more flexible CDR that is able to lock over a wide range of data-rates (typically 45kbps – 200kbps) requires an external clock to be provided by the optical diode. The wavelength of this external clock must be different to the wavelength of the optical data to avoid crosstalk. But, in any case, a maximum input data-rate of 200kbps is barely adequate for high-performance biomedical devices.

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Fig.1 is a simplified block diagram of a sensor system which is controlled by optical signals. The system converts analog sensor signals to digital data, and transmits them. We propose a low-power, high data-rate referenceless CDR for optical transmission of data from this sort of biomedical device.

The rest of this paper is organized as follows: in Section II, we introduce the architecture of the CDR, the mechanism of data-edge modulation, and the design of each block. In Section III, we present experimental results obtained from the new CDR, and conclusions are drawn in Section IV.

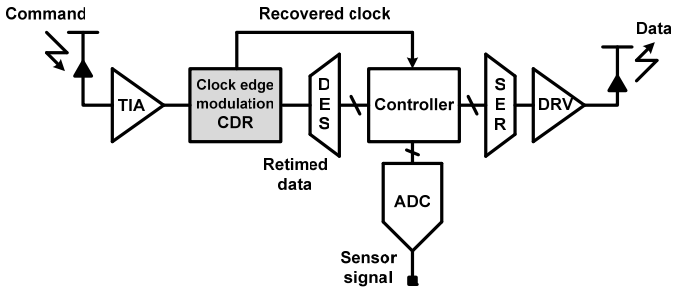

Figure 1. Simplified block diagram of the proposed sensor system

II. CDR DESIGN

A. CDR architecture

Research on CDRs for chip-to-chip transfer has mainly been focused on performance issues such as input data-rate, jitter and jitter tolerance [5]. However, a simpler CDR, with lower power consumption that supports lower data-rates cannot be obtained by scaling high-performance designs. In a wireless biomedical application, whether communication is RF or optical, the design of a synchronous CDR must take into account crosstalk between the data and the clock. A synchronous CDR is expensive for an optical system due to additional requirements such as optics for several wavelengths and band-pass filters. A referenceless CDR is more appropriate for this application [6-9].

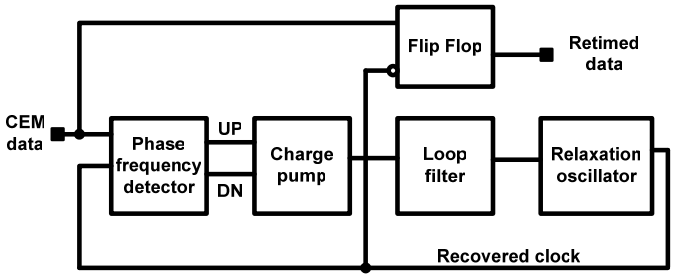

Figure 2. Block diagram of the proposed CDR

A general referenceless CDR has no reference clock, but it requires a complicated frequency detection circuit with a large area and consumes a lot of power. An alternative is the clock-embedded CDR which extracts the clock signal using information embedded in the data-stream; this approach simplifies clock recovery without introducing the possibility of harmonic locking, which suggests that it should be suitable for biomedical devices. However, the type of clock-embedded CDR which extracts clock information by the use of an additional voltage level [8] is not suitable for this application because of the limited dynamic range of a photo diode. The alternative clock-edge modulation (CEM) technique introduces information into the clock signal by repositioning the clock edge [9]. Bandwidth is preserved because multiple items of data are encoded in a single symbol period. However, this type of CDR generally requires a delay-locked loop (DLL) to create multiple-phases. We propose a low-power referenceless CDR architecture that achieves clock-edge modulation without the need for multi-phases, as shown in Fig. 2.

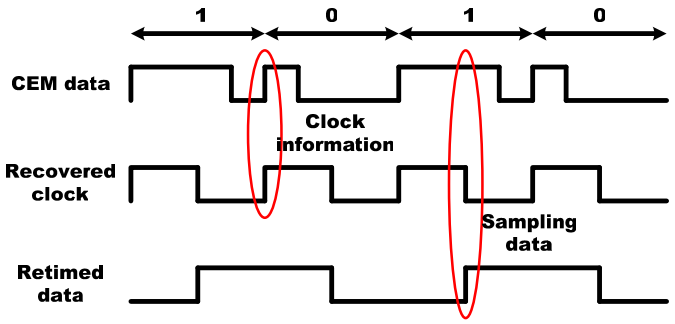

Figure 3. Clock-edge modulation

Our CDR is composed of a clock recovery loop and a negative edge-triggered sampling flip-flop for locating the clock data, as shown in Fig. 2. The clock recovery loop is based on a phase-locked loop (PLL) with a phase frequency detector (PFD), which is easily implemented due to the presence of CEM data. Fig. 3 shows the timing diagram of clock-edge modulation. The positive edges of the input data contain both period and phase information. The negative edges of the input data involve one bit of information. The PFD only extracts clock information for the positive edges of the input data, and compares the recovered clock with this CEM data.

UP / DN signals from PFD identify the leading and lagging phases of the recovered clock and are sent to the charge pump (CP). Then the voltage from the CP changes the period of the relaxation oscillator. Thus the lead or lag between the input data and the recovered clock determines the period and phase of the oscillator. This allows the recovered clock to be locked without placing any limit on the run-length of the clock information. When the input data is sampled at the falling edge of the internal clock in the locked state, accurate data values can be obtained quite simply. If the positions of a falling edge for 0 or 1 respectively are within 75% and 25% of the period, the CDR keeps the jitter of the recovered clock signal below 0.25UI.

B. Relaxation oscillator

Ring oscillators are commonly used in ultra-low power applications when operated in the subthreshold region [10]. However this type of ring oscillators may be unsuitable for the VCO of a CDR with a wide input range. On the other hand, the frequency of a crystal oscillator is much less affected by variations in supply voltage, temperature, and process; but crystals are bulky and add cost. Thus relaxation oscillators are often preferred for low-power applications because they do not require any external components and can be implemented cheaply in a CMOS technology. In addition, they draw less current than crystal oscillators at the cost of larger clock jitter [11]. However, we have already mentioned that jitter is not an issue in our application until 0.25UI.

Therefore our VCO uses a relaxation oscillator, as shown in Fig. 4. A relaxation oscillator produces a constant frequency by charging and discharging capacitors between two fixed voltages. In our CDR, The VCO has a constant charge voltage and a controllable discharge voltage. The VCO consists of a constant current source I_{ref} which is controlled by the recovered clock signal and two comparators that compare the voltage of capacitors V_{C1} and V_{C2} with the control voltage V_{ctrl}. An SR latch uses the output voltage from the two comparators and the output of the latch provides feedback that turns the constant current source on and off.

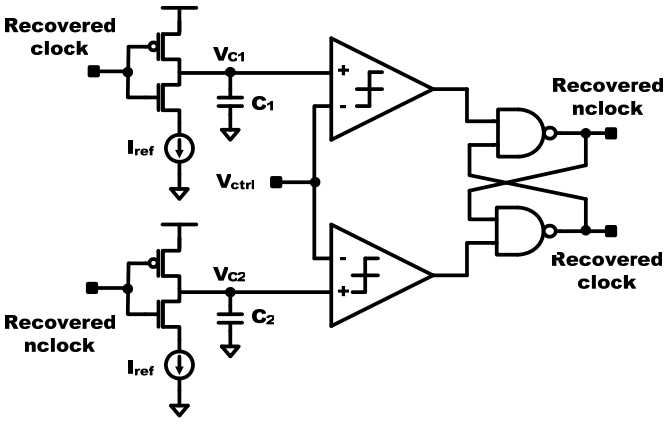

Figure 4. Schematic of the relaxation oscillator

As shown in Fig. 4, C_1 and C_2 are alternately charged to VDD, controlled by the state of the RS latch, and then discharged to V_{ctrl} by I_{ref}. The triangular waveforms of V_{C1} and V_{C2} form one period of the clock. The length T_{OSC} of this period is determined as follows:

$$T_{OSC} = \frac{2C(VDD - V_{ctrl})}{I_{ref}}, \quad (1)$$

where I_{ref} is a constant current, V_{ctrl} is the control voltage, and $C = C_1 = C_2$.

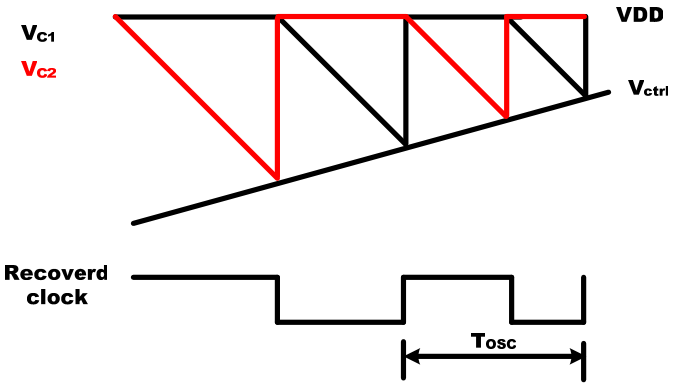

Figure 5. Timing diagrams of the recovered clock signal, V_{C1}, V_{C2} and V_{ctrl}, respectively

Thus the UP / DN signals are determined by the lead or lag of the phase at the output of the PFD. This adjusts V_{ctrl}, and the frequency of the relaxation oscillator is changed to align the phases as shown in Fig. 5.

III. Experimental Results

The proposed CDR was implemented in a 0.18μm process. Fig. 6 shows the die photograph. The loop filter, which occupies most of the die area, is a second-order RC filter for stability. The core area is 0.09mm^2, including some test circuitry.

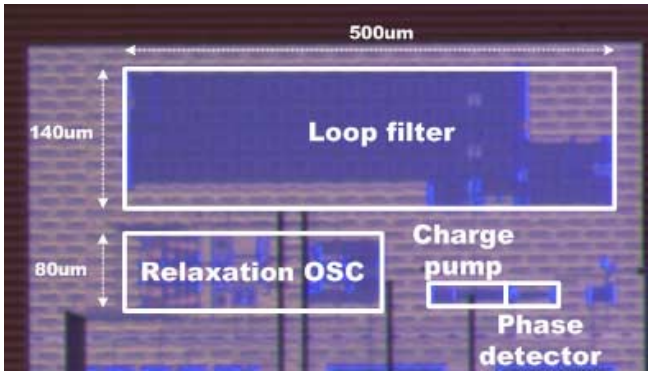

Figure 6. Die photo

Fig. 7 is a screenshot of the oscilloscope when the supply voltage is 0.7V and input data rate is 10MHz. The input pattern is '1001010' and is part of a 2^{15}-1 PRBS.

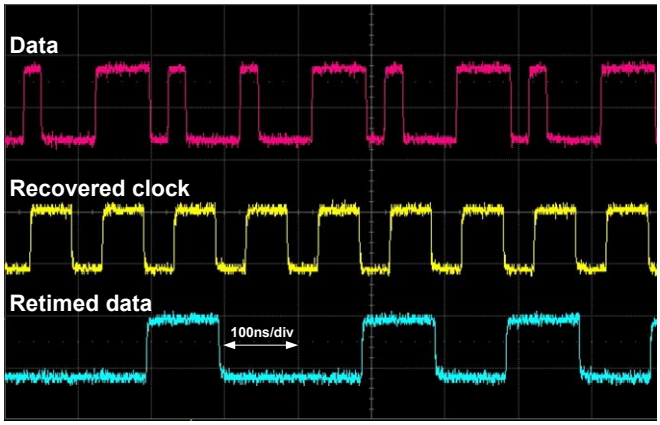

Figure 7. Measured waveforms of the input data, recovered clock and retimed data, respectively

Fig. 8 is a plot of power consumption versus data transfer rate. Our CDR supports input data-rates from 200kbps to 10Mbps at the supply voltage of 0.7V, and consumes 8μW at an input data-rate of 10Mbps. When the supply voltage is 1.0V, normal operation allows data-rates from 200Kbps to 24Mbps. In measuring the power consumption, an input pattern is used which produces the maximum number of transitions.

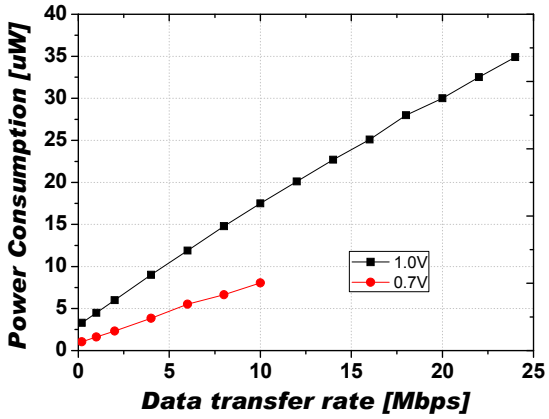

Figure 8. Measured data transfer rate vs. power consumption

Fig. 9 shows a histogram of measurements of the recovered clock period of 100ns. The minimum and maximum periods of the recovered clock are 97.3ns and 104.2ns respectively. The variation in recovered clock period is 6.9% over 1.5M samples. During a 32-hour test, no error bits were detected, suggesting that the bit error rate (BER) is lower than 10^{-13}. The data-rate was 10Mbps and the circuit was operating at the supply voltage of 0.7V with a 2^{15}-1 PRBS input pattern.

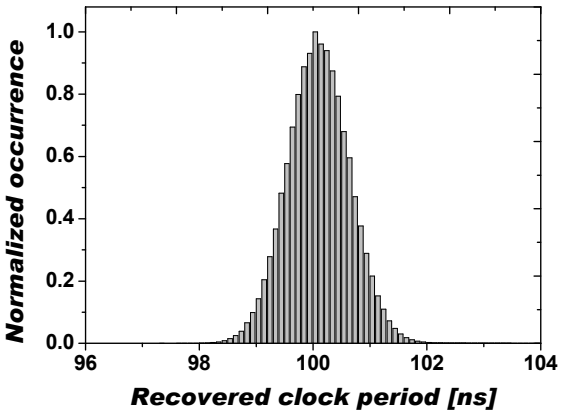

Figure 9. Measured histogram of recovered clock period

Measured parameters of this CDR are compared with previous devices in Table I. Our CDR uses the energy at 0.8pJ/bit, and achieves the highest data-rate, which is 10Mbps at a supply voltage of 0.7V.

TABLE I. COMPARISON WITH OTHER REPORTED CDRS

	09' VLSI [12]	10'ICSICT [13]*	10' ISSCC [4] **	This work
Process	0.18μm	0.18μm	90nm	0.18μm
Design	Demodulator (FSK)	CDR (ASK)	CDR	CDR
Data rate	250kbps	500kbps	200kbps	10Mbps
Supply voltage	0.7V	1.8V	0.3V	0.7V
Power	21μW	29.52μW	217nW	8.05μW
Energy/bit	84 pJ/bit	59 pJ/bit	1 pJ/bit	0.8 pJ/bit

*: simulation result

**: 3b4b coding, reference clock

IV. CONCLUSION

We have described an 8μW, 10Mbps referenceless CDR circuit with clock-edge modulation for biomedical devices and sensor applications, operating at the supply voltage of 0.7V. This design eliminates an external reference clock but is not subject to harmonic locking. A voltage-controlled oscillator based on a relaxation oscillator is used to reduce power consumption.

Our CDR has an input data-rate between 200kbps and 10Mbps at the supply voltage of 0.7V, and operates up to 24MHz at the supply voltage of 1.0V. The bit error-rate of our CDR is lower than 10^{-13}. The energy per bit is as low as 0.8pJ/bit, even though the circuit is implemented in a 0.18μm CMOS technology.

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