A CMOS Readout Integrated Circuit with Wide Dynamic Range for a CNT Bio-Sensor Array System

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***Abstract*—We present a sensor readout integrated circuit for the CNT bio-sensor array, the heart of which is our low-power current-input continuous-time ΔΣ modulator that is capable of dynamic range extension. Experimental results show that the prototype chip, designed and fabricated in 0.18μm CMOS process, achieves a dynamic range of 87.746dB and has a readout rate of 160kHz, which guarantees 1k sample/s per each sensor. It consumes 8.94μW/cell considering the 16x10 sensors and its core area is 0.085mm^2.**

Keywords—CMOS; readout integrated circuit; dynamic range; current-input; delta-sigma; carbon nanotube; bio-sensor

I. INTRODUCTION

Ever since carbon nanotubes (CNTs) are discovered by Iijima in 1991 [1], they have been treated as the most promising materials. Recently, CNTs demonstrate the sensitive modulation of its conductance to the charges adjacent to it [2]-[5]. This special property makes them to be used as chemical sensors for the voltage-mode detection of hazardous gasses such as NH_3 and NO_2. Several additional studies of CNT sensors show that there is a particular voltage across the CNT which is most suitable for each application. For instance, the detection of bio-molecules in an aqueous environment requires a voltage below 1V to prevent side-effects caused by the ionization of the buffer solution [4]. Meeting this requirement involves current-mode detection which depends on the conductance characteristics of a CNT.

An array structure is frequently adopted in sensor applications, since it is known to be relatively robust against undesirable effect such as process variation and environmental noise. In this case, the distribution of the initial conductance of CNT sensor elements is inherently spread widely. Therefore a readout circuit requires a wide dynamic range (DR) [5]. In general, a circuit with a high signal-to-noise ratio (SNR) which also has a wide DR is complicated and power hungry [6]-[8].

To cope with the problems described above, we propose a low-cost and low-power current-to-digital conversion scheme for CNT sensors with dynamic range extension. Fig. 1 shows the overall architecture of our readout integrated circuit (ROIC). The circuit consists of a voltage regulator and a current-input continuous-time ΔΣ modulator (CT-DSM), with a digital decimation filter. The voltage regulator sets voltage difference of $V_{DDCNT} - V_{REG}$ onto the CNT sensor, and the resulting current reflects the change in conductance. This current is then directly converted to a digital code by our current-input ΔΣ A/D converter.

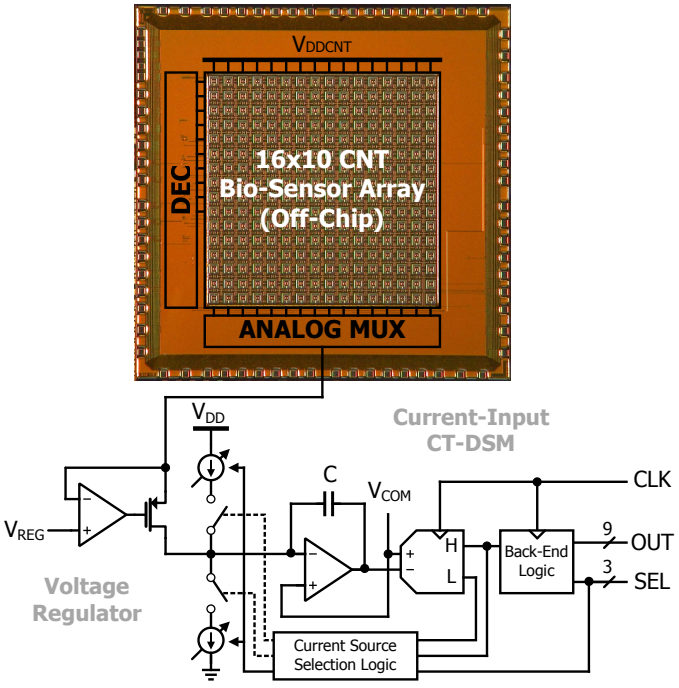

Figure 1. Overall architecture of the proposed CNT ROIC

II. CIRCUIT ARCHITECTURE

Fig. 2 shows a model of our current-input continuous-time ΔΣ modulator with a 1st-order loop. The resistance of the loop coefficient of its linear model can be moved to the front of the input path and to the middle of the feedback path. Then the resistance R of the input path can be eliminated by transforming the input voltage V_{IN} to an input current I_{IN} by Ohm's law. Finally the resistance of the feedback path can be merged with that of the voltage-mode DAC, producing a current-mode circuit with a current DAC. In this structure, the full-scale input current $I_{IN(FS)}$ is determined from the full-scale output voltage $V_{OUT(FS)}$ and the feedback resistance R.

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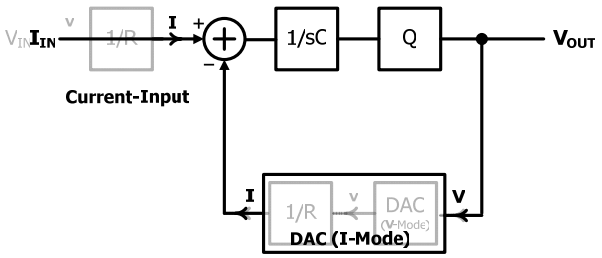

Figure 2. A model of the current-input continuous-time ΔΣ modulator with 1st-order loop.

In a real implementation the resistance in the feedback path is implicitly included in that of the current DAC, so we only need to determine the full-scale input current, which is equal to $I_{DAC(MAX)}$, the maximum output current from the DAC:

$$I_{IN(FS)} = \frac{V_{OUT(FS)}}{R} = I_{DAC(MAX)}. \quad (1)$$

This analysis can only be implemented as a circuit by eliminating the input resistance of the continuous-time ΔΣ loop and setting the maximum output current of the current DAC to the desired full-scale input current. Furthermore, if we adopt a 1-bit ΔΣ loop, a single current source supplying $I_{DAC(MAX)}$ may be sufficient. This makes the design both simple and effective because the full-scale input current is determined by the DAC alone. A similar analysis may be applied to a higher-order loop.

Fig. 3 shows the concept of the dynamic range extension scheme. In general, the DR is roughly proportional to the SNR. As we already mentioned, we could design an ADC of high SNR for sensor applications which require a wide DR, but a high-SNR circuit is an over-complicated way to achieve a high DR, and the high SNR would be wasted. Conversely, an ADC of moderate SNR will be less adaptive to variations in sensor characteristics because of its narrow dynamic range. In our scheme, only one core ADC is utilized, and its full-scale input level is adjusted to match the range of the current input. This allows an ADC of moderate SNR to provide an extended DR, as shown in the rightmost diagram of Fig. 3. As a result, the total dynamic range DR_{TOTAL} of the circuit is given as follows:

$$DR_{TOTAL} = DR_{ADC} + \left(FS_{MAX} - FS_{MIN}\right), \quad (2)$$

where DR_{ADC} is the dynamic range of the core ADC, FS_{MAX} is the maximum full-scale input, and FS_{MIN} is the minimum full-scale input, all expressed in decibels.

III. Circuit Implementation

The schematic of our 1st-order 1-bit current-input continuous-time ΔΣ ADC for the sensor array is shown in Fig. 4. It is implemented as a bidirectional single-ended circuit, which consists of a current DAC with the capability for full-scale current adjustment, an integrator consisting of an op amp and an integrating capacitor C, a comparator acting as a 1-bit quantizer, and back-end logic. This logic decimates the ΔΣ modulator outputs and determines the correct full-scale current of the DAC for the range of the input.

A. Current DAC

The current DAC sources current into, or sinks current from the integrating capacitor, depending on the outputs H and L of the modulator loop [9, 10]. In our design, three different full-scale currents of 50μA, 5μA and 0.5μA are available. Combinational logic circuitry is added to select the current source for each range, following instructions from the back-end logic.

B. Integrator and Comparator

The value of the integrating capacitor C is primarily determined from the loop characteristics, such as the oversampling ratio (OSR). However, a linear model does not reflect exact operation of a feedback loop containing a 1-bit quantizer. So we repeatedly analyze and simulate the loop, including the 1-bit quantizer and non-ideal op amp, until a proper condition is reached. The op amp in the integrator must have an appropriate DC gain and unity gain bandwidth (GBW). In a continuous-time implementation, a GBW frequency which is slightly higher than the sampling clock frequency is sufficient. The DC gain must be carefully chosen to correspond with the OSR.

To design the comparator as a 1-bit quantizer, we selected a non-return-to-zero (NRZ) output, which is easy to incorporate in this design. Attention must be paid to the clock jitter and the clock-to-output delay, caused by metastability; both of these can degrade the SNR.

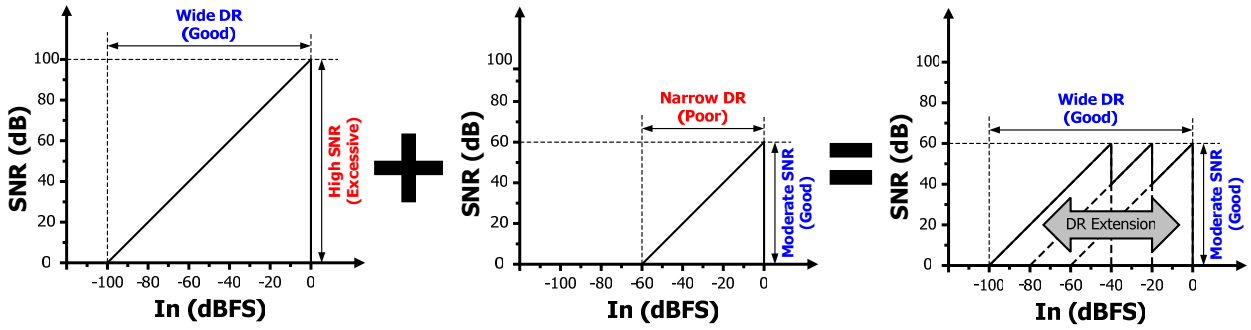

Figure 3. The concept of the dynamic range extension scheme

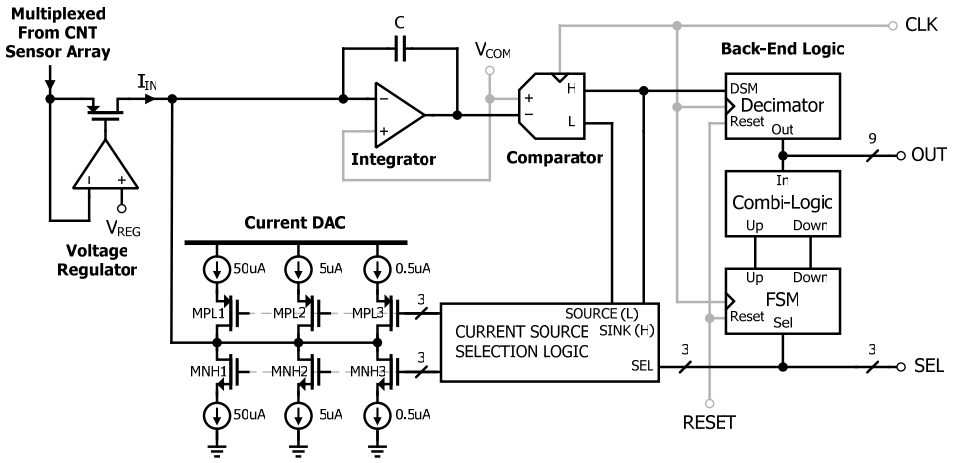

Figure 4. 1st-order 1-bit current-input continuous-time ΔΣ ADC with a voltage regulator for the ROIC

C. *Back-End Logic*

The back-end logic consists of the decimator, the combinational logic which determines whether the current input level is in the currently selected full-scale range, and the finite-state machine (FSM) that controls which range should be selected. This design is simplified by the use of a simple 1st-order sinc filter as the decimator [8]. The combinational logic observes the output of the decimator and generates an *UP* signal if the converted value exceeds an upper threshold or a *DOWN* signal if the converted value falls below a lower threshold. The FSM receives these *UP* and *DOWN* signals as inputs and changes the 3-bit control code *SEL* to select the appropriate current source for the current DAC which is then turned on. The transitive instant of the FSM output is synchronized to the rising edge of the clock and the output period of the decimator. In this design, upper thresholds are -26dBFS and -46dBFS, and lower thresholds are -28dBFS and -48dBFS, respectively. This allows a 2dB margin between the scale-up and scale-down thresholds, so as to prevent the circuit from falling into any metastable transition between two neighboring full-scale current ranges. If more reduced non-linearity in the transfer characteristic of the ROIC at each boundary crossing is preferred, the current DAC should be calibrated to guarantee more precision in the ratio among the currents of sources and sinks.

IV. Experimental Results

The proposed circuit has been fabricated in a 0.18μm CMOS bulk technology. Fig. 5 shows its microphotograph. The core area is 0.085mm^2. The ADC operates at 20.48MHz sampling clock frequency with 1.8V supply and it consumes 8.94μW/cell considering the 16x10 sensors. In-band frequency of 160kHz with the OSR of 64 enables the ADC to process maximum 16x10 cells at least 1kS/s conversion rate. Maximum full-scale input current for the readout circuit is 50μA. In an AC test with a 2.101kHz sinusoidal input, the measured SNRs were 49.113dB, 48.652dB and 45.316dB, for input currents of 25μA, 2.5μA and 250nA respectively. The output spectrum of the ΔΣ modulator at 25μA is shown in Fig. 6. A DC test demonstrated that the dynamic range extension scheme works properly.

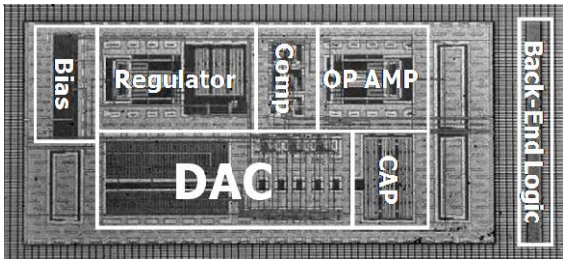

Figure 5. Microphotograph

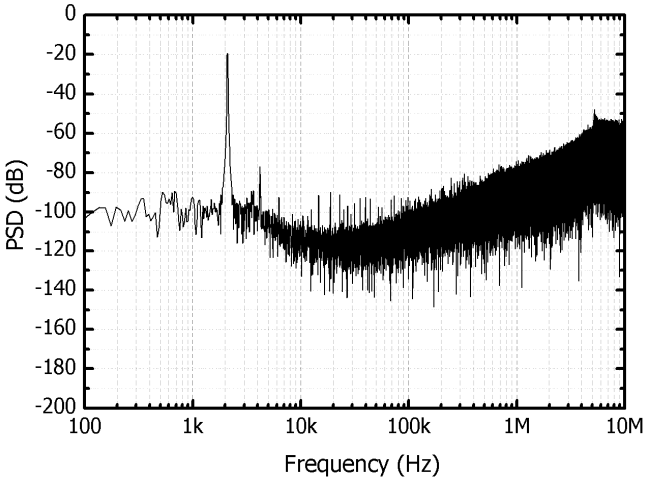

Figure 6. Output power spectrum of the ΔΣ modulator

The overall SNR characteristic with the extended dynamic range is shown in Fig. 7. Proposed circuit achieves a dynamic range of 87.746dB. Considering the allowed maximum full scale input current and the operating region of the regulator, the regulated voltage onto the CNT sensor can range from 50mV to 3.3V approximately. In this case, the measured dynamic range potentially corresponds to the resistance range from 1kΩ to 1.5MΩ. If extended upper bound of the measurable resistance is necessary, it is easily achievable since V_{DDCNT} is independent from the supply voltage of the ROIC, V_{DD}. Table I summarizes the design and performance parameter.

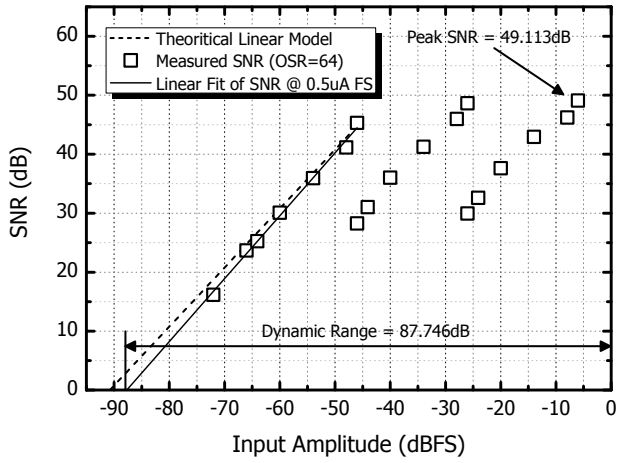

Figure 7. Measured overall SNR characteristic with the extended dynamic range

TABLE I. PERFORMANCE SUMMARY

Technology	0.18μm 1P6M CMOS
Supply Voltage	1.8V
Sampling Frequency	20.48MHz
In-Band Frequency	160kHz
Oversampling Ratio	64
Power Consumption/Cell	8.94μW/cell
Measured SNRs (2.101kHz sinusoidal input)	49.113dB (25uA Input)
	48.652dB (2.5uA Input)
	45.316dB (250nA Input)
Overall Dynamic Range	87.746dB

V. CONCLUSION

We have proposed a low-power CNT bio-sensor ROIC based on a current-input continuous-time ΔΣ ADC with wide dynamic range. This design incorporates a DR extension scheme into the current-mode circuit, allowing it to achieve extended DR using only a simple ADC with a moderate SNR. We expect this design to be effective in sensor applications where a wide dynamic range is required and in which the design complexity and power consumption must be low for compatibility with large-scale CNT bio-sensor arrays.

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