A HIGH-RESOLUTION AND FAST-CONVERSION READOUT CIRCUIT FOR DIFFERENTIAL CAPACITIVE SENSORS

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ABSTRACT

Our readout integrated circuit (ROIC) for differential capacitive sensors, such as thin-membrane transducer, uses current switching and time-domain based technique to measure the difference between the capacitance of the sensing and reference more rapidly, while maintaining accuracy. The 12-bit ROIC is designed and fabricated in a 0.35μm digital CMOS bulk technology.

I. INTRODUCTION

Piezoresistive devices are popular for sensor applications, but they dissipate a lot of power. Capacitive sensors have no intrinsic power consumption and can be interfaced with relatively low-power circuit techniques, giving them a wide variety of possible applications including pressure sensing, finger print recognition, hazardous gas detection, and the monitoring of bio-molecular reactions in micro-electro-mechanical systems (MEMS). The recently introduced thin-membrane transducer (TMT) is a sensitive capacitive device that also avoids the design constraints associated with metal-oxide semiconductor field-effect transistors (MOSFETs) [1].

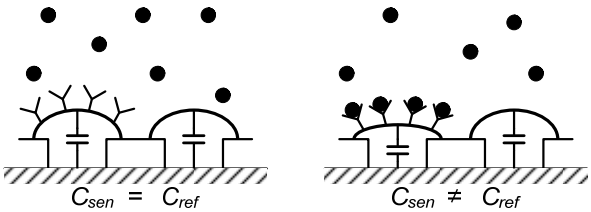

Figure 1: A thin membrane transducer (TMT) [4].

Figure 1 shows how a tensile or compressive stress is induced in the dome-shaped membrane of a TMT, typically by a bio-molecular reaction. This stress deforms the membrane and changes the capacitance of the device. The detailed operation of a TMT and its readout circuit depends on the application, but the capacitive sensor interface is usually an analog circuit.

Converting the sensed analog voltage to a digital code involves an analog-to-digital converter (ADC), which needs a lot of area and power [2]. The addition of an ADC makes a capacitive sensor liable to noise, crosstalk, and spurious coupling; and the dynamic range of the sensor is limited by the supply voltage, which is constantly decreasing as the technology is scaled down. These problems are getting worse if the sensor circuitry is integrated with complicated signal processing blocks on a single substrate implemented in a deep submicron CMOS technology. A particular problem is the relative instability of voltage reference sources [3]. Frequency references are more accurate, so that a capacitance-to-digital converter (CDC) that converts differential capacitance to a time difference and then quantizes it in the time domain is to be preferred [4].

Most time-to-digital converters (TDCs) measure time with a single counter; but the resolution of the CDC utilizing this type of the TDC approach is limited by both of the length of intermediate time signal and a reference clock frequency of TDC [5].

This observation motivates our use of a dynamic current switches and a coarse and fine TDC using a counter and a multi-phase delay-locked loop (DLL). The interpolators in the multi-phase DLL resolve the fractional parts of the clock cycle between the arrival times of the pulses. Measurement results are obtained by combining the number of full clock cycles given by the counter and the fractional parts resolved by the interpolators.

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II. CIRCUIT DESCRIPTION

A. Architecture

Our readout integrated circuit (ROIC) has two main parts; a capacitance-to-time converter (CTC) and a time-to-digital converter (TDC). The deviation of the capacitance of the sensor from that of the reference generates SIGN, START, and STOP signals which delineate a time interval. The SIGN signal indicates whether active or reference sensor has a larger capacitance; and the time difference between the START and STOP signals measures that difference. These signals are digitized by the TDC to produce the digital code D_{out}[0:11]. This combination of a counter and interpolation has been found to be practical when both a large linear dynamic range and high resolution are required.

B. Capacitance-to-Time Converter

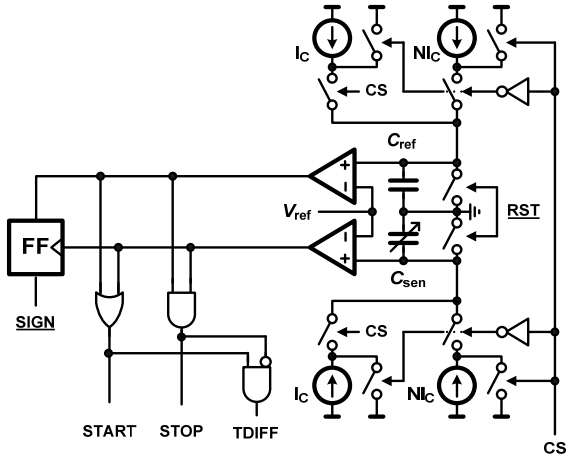

Figure 2: Block diagram of the differential capacitance-to-time converter with dynamic current switches.

The circuit of Fig. 2 converts the difference between the capacitance of the sensor (C_{sen}) and that of the reference (C_{ref}) to a time interval. This is achieved by connecting each capacitor to a constant current source and a comparator. If the C_{sen} is smaller than C_{ref}, then the SIGN signal is low; otherwise, it is high. The signals produced by the comparators are aligned by subsequent logic into START and STOP signals regardless of which capacitance is larger.

The CTC circuit operates in three phases: reset, charging, and comparison. During the reset phase, the reset signal level continues high and the reset switches discharge both sensor and reference capacitors to the same initial state. In the charging phase, each current source begins to charge its capacitor. When the output voltage from either comparator is asserted high, the START signal is also asserted, and the comparison phase begins. It lasts as long as the START signal stays high and the STOP signal stays low as shown in Fig. 3.

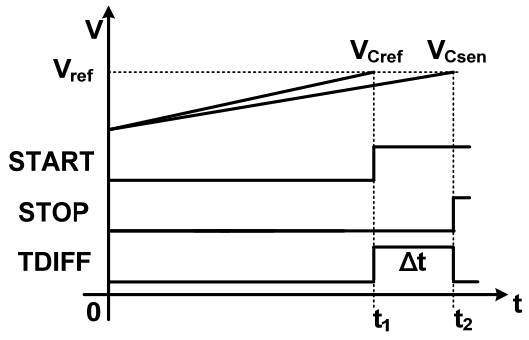

Figure 3: Timing diagram of a conventional differential capacitance-to-time conversion unit [4].

The interval between t_1 and t_2 is proportional to the difference between the two capacitances. Consider the case in which C_{sen} is greater than C_{ref}. Then the output of the comparator connected to C_{ref} becomes high sooner than that of the comparator connected to C_{sen}.

The time interval Δt is can be related to the difference between the charging time of the reference capacitor C_{ref}, which is t_1, and that of the sensing capacitor C_{sen}, which is t_2, by the following formulas:

$$t_1 = \frac{C_{ref} V_{ref}}{I_C},$$

$$t_2 = \frac{V_{ref}}{I_C}\left[\left(C_{sen} - C_{ref}\right) + C_{ref}\right], \text{ and}$$

$$\Delta t = t_2 - t_1 = \frac{V_{ref}}{I_C}\left(C_{sen} - C_{ref}\right)$$

The resolution of the circuit can be increased by reducing the source current I_C, which increases the length of the time signal Δt in inverse proportion. However, this also extends t_1 and t_2. The ratio between t_1 and Δt is the same as that

between C_{ref} and ΔC, which is about 1000 to 1, so that the conversion time soon become undesirably extended.

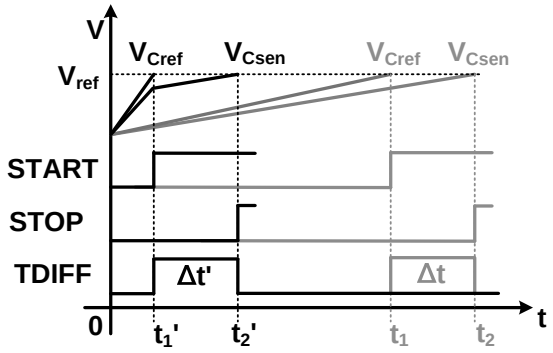

Figure 4: Timing diagram of a proposed differential capacitance-to-time converter utilizing a dynamic current switching technique.

In order to increase Δt without increasing the conversion time, we use a dynamic current switching technique. Two different current sources, I_C and NI_C, which is N times larger, are now used to charge the capacitors. The current source NI_C is used to charge the capacitors until the voltage at the comparator input reaches V_{ref} (t_1'). This reduces the charging time by a factor of almost N. After t_1', the current source I_C is used so that Δt is not reduced. Thus,

$$t_1' = \frac{C_{ref} V_{ref}}{NI_C},$$

$$t_2' = \frac{V_{ref}}{I_C}\left[(C_{sen} - C_{ref}) + \frac{C_{ref}}{N} \right], \text{ and}$$

$$\Delta t' = t_2' - t_1' = \frac{V_{ref}}{I_C}(C_{sen} - C_{ref}) = \Delta t$$

After the comparison phase, the CTC cycle begins again with the reset phase.

C. Time-to-Digital Converter

Time differences of microseconds or longer are best measured with a single counter that counts the pulses of an oscillator clock during the time interval. With a stable reference oscillator a counter can provide a moderate resolution, a large linear dynamic range, and good stability. Also, the conversion time is short, which enables a high measurement rate. However, the resolution of a TDC cannot be less than the time period of its clock.

To overcome this limitation, we propose the coarse and fine TDC circuit to calculate the residual times between clock ticks. Good stability can be achieved by locking the propagation delay of the delay-line to a cycle of a stable reference oscillator by using a DLL configuration with delay cells. Because, the arrival moment of the signals (START and STOP) is unknown and asynchronous with respect to the reference clock edges, synchronizing logic using multi-phase DLL is also adopted in the fine TDC circuit.

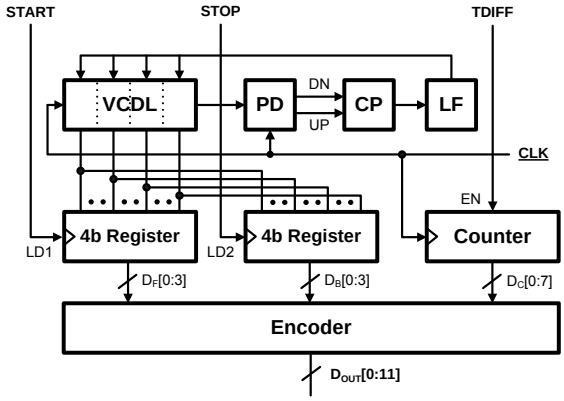

Figure 5: Block diagram of coarse and fine time-to-digital converter with a multi-phase delay-locked loop.

The presence of a clock signal makes it natural to lock the propagation delay of the delay-line to the clock cycle to achieve stable interpolation. The resolution of the basic delay-line is set by the propagation time of the delay cells. The delay-line generates a set of evenly spaced clock signals which propagate in the delay-line with a known phase difference, which is the resolution of the delay-line. The START and STOP signals take samples of the clock phases and store the state of the delay-line in registers. The state of these registers determines the moments of arrival of the START and STOP signals within the clock period. As the propagation delay of the delay-line is locked to the reference clock cycle, only a limited number of delay cells, defining the interpolation ratio, can be connected in series to form a delay-line.

As we mentioned above, a clock synchronous counter is used to obtain a larger dynamic range (coarse time). Delay-lines of DLL perform time

interpolation within a period of the reference clock CLK (fine time). The encoder receives three digital codes, one from the counter and two from the registers, and it calculates an n-bit digital code, D_{out}, as follows:

$$D_{out} = D_C \bullet 2^M + (D_F - D_B),$$

where M is the number of least significant bits determined by the DLL. In our implementation, M is 4.

III. EXPERIMENTAL RESULTS

To demonstrate the effectiveness of ours, we designed and fabricated the readout circuit in a 0.35μm CMOS technology.

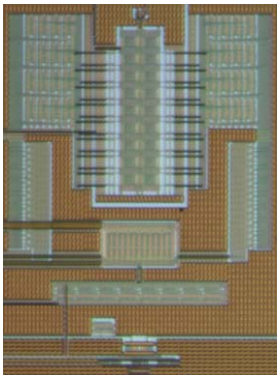

Figure 6: Chip microphotograph of the proposed ROIC circuit.

Figure 6 shows the chip microphotograph of our ROIC circuit. Characterizing its performance is carried out with 3.3V power supply. The current sources I_C and NI_C are 2μA and 16μA respectively. Dynamically switching two different current sources decreases the conversion time, compared with a circuit that only uses a 2μA source alone, while maintaining the same resolution. The counter is for the eight most significant bits and 16 delay cells in the DLL is for the four least significant bits. The potential inaccuracy of the time signal can be compensated for by digital control.

Figure 7 shows that our circuit experimentally achieves 12-bit resolution with clock frequency of 50MHz.

IV. CONCLUSIONS

A CMOS readout circuit for differential capacitive sensors such as thin-membrane transducer has been proposed and implemented in a low-cost digital CMOS technology. The current switching technique and TDC architecture based on a coarse and fine two-level conversion scheme are innovatively utilized to reduce the conversion time without sacrificing resolution. Experimental results confirm the suitability of the circuit for differential capacitive sensor applications.

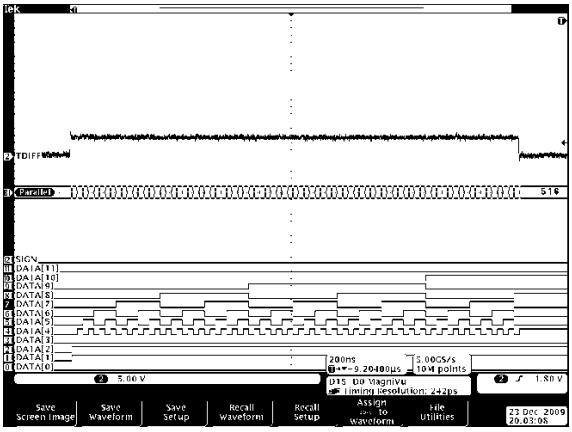

Figure 7: Measured digital output against difference in capacitance between the reference and sensing capacitors.

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