A Three-Step Power-Gating Turn-on Technique for Controlling Ground Bounce Noise

Rahul Singh[1] AhReum Kim[1] SoYoung Kim[2] Suhwan Kim[1]
[1]Electrical Engineering, Seoul National University, Seoul, Korea
[2]Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea
{rsingh,arkim}@ctcl.snu.ac.kr, ksyoung@skku.edu, and suhwan@snu.ac.kr

ABSTRACT
To suppress the ground bounce noise with a minimal wake-up time penalty, a three-step turn-on strategy and its corresponding power-gating structure are proposed. During the circuit's meta-stable region of operation, specifically, the amount of current flowing through the sleep transistors is precisely controlled while the virtual or circuit power supply is quickly boosted when the internal nodes of the circuit are stable. In 65 nm CMOS technology, simulation results demonstrate that our technique reduces the peak amplitude of the ground bouncing noise by up to 94% as compared to the conventional abrupt turn-on technique.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, VLSI (very large scale integration).*

General Terms
Design, Performance, Reliability

Keywords
Power-gating, ground bounce, inductive noise, mode transition, system-on-a-chip (SOC) design.

1. INTRODUCTION
In order to reduce the overall power consumption of modern high-performance integrated circuits, a well-known technique is to scale supply voltages. However, to maintain performance, devices threshold voltages must scale as well, which cause an exponential increase in sub-threshold leakage currents [1]. Reducing these leakage currents is crucial for burst-mode type circuits, where the system spends the majority of time in an idle standby and a failure to control the leakage currents can greatly reduce the battery life. The multi-threshold CMOS (MTCMOS) circuit [2] is an effective technique for reducing the leakage power in standby mode while still permitting high-speed operation in active mode. The power gating switch is typically positioned between the circuit power supply (or circuit ground) and the actual power supply rail (or the actual ground rail). During the active mode, the sleep transistor is switched 'on' ensuring normal operation. During the idle (or sleep) mode however, the sleep transistor is switched 'off' to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby.

Although the power-gating technique significantly reduces the leakage power consumption, it does suffer from certain disadvantages that necessitate a careful understanding of the impact of power gating on the behavior of circuits. For example, when a PMOS sleep transistor, stacked between the actual power supply rail and the circuit power supply, is turned off, all the internal nodes are discharged to a steady-state value near the logical ground. The sleep transistor, at the beginning of wake-up, is operating in the saturation region and consequently, large instantaneous current flows through it. Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these current surges manifest as voltage fluctuations in the power rails. If the magnitude of any such voltage droop is greater than the noise margin of the circuit (which is especially low for deep sub-micron designs), it may erroneously latch a wrong value or switch at the wrong time. This inductive noise can therefore cause unexpected logic behavior and signal integrity problems [3]. Decoupling capacitor can be added to reduce the noise on power supply rails, but this is at the expense of area, yield, and leakage power consumption. In this context, specific design techniques have been proposed that significantly reduce the wake-up penalty during mode transition [4]-[7].

In this paper, we observe the behavior of the internal nodes of the circuit as the virtual power supply rail is powered up to the supply value and divide the wake-up transition into three stages. We then propose a novel power-gating structure and its three-step turn-on control mechanism to adjust the magnitude of supply current to the logic block in each of the three stages to effectively suppress the ground bounce noise. The wake-up command initiates a finite state machine (FSM) which continuously monitors the circuit power supply to generate trigger signals to force the power gating circuit into a particular phase.

The remainder of this paper is organized as follows. Section 2 describes previously proposed techniques to suppress ground bounce. Our three step power gating structure and its controlling mechanism is then introduced and discussed in Section 3. In Section 4, the simulation results are presented and finally, conclusions are drawn in Section 5.

2. PREVIOUS WORKS
In Figure 1(a), a typical implementation of the power-gating technique is depicted. However, if the sleep transistor is turned on in an abrupt manner, significant ground bouncing can be observed. This is because at the start of the wake-up, the sleep transistor operates in the saturation region as the circuit power

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supply, called as the virtual VDD (VVDD) node, has been discharged to a steady state value near GND. Consequently, the large amount of instantaneous current that flows through the sleep transistor at the moment of wake-up initiation generates inductive noise and can disrupt the normal functioning of neighboring circuits.

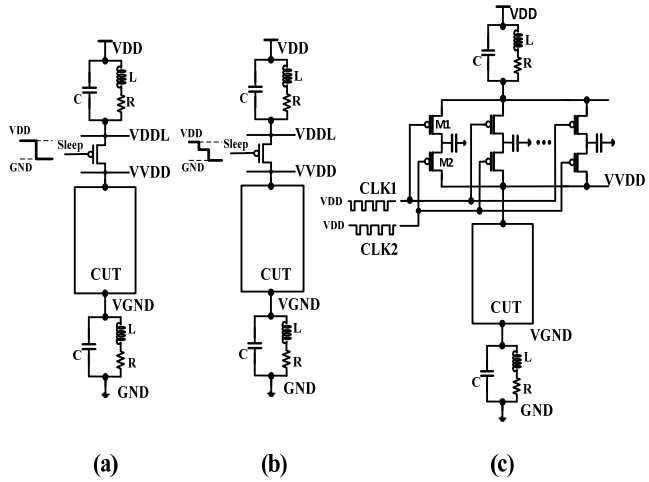
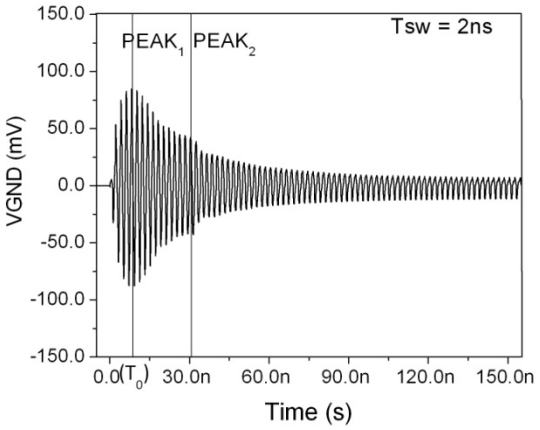


Figure 1: (a) Conventional power-gating switch. (b) Non-uniform stepwise powering-on of the sleep transistor (c) Sleep switch in a switched capacitor resistor configuration.

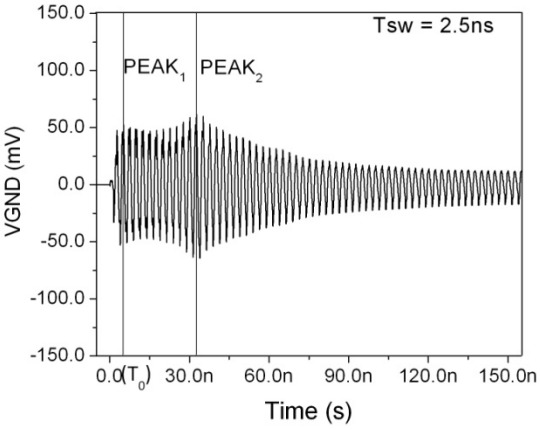
In [4], an approach to minimize ground bounce (the stepwise V_{GS} scheme) is presented where the sleep transistor is turned on in a non-uniform stepwise manner (Figure 1(b)). The idea is to control the V_{GS} of the sleep transistor dynamically and hence control the V_{DS} value and the current flowing through it. At the onset of wake-up, the instantaneous current value is very sensitive to variations in the V_{GS} of the sleep transistor. Therefore, the sleep transistor is first weakly turned on with a value between VDD and 0. This is the relaxation stage where the $|V_{DS}|$ of the sleep transistor is allowed to become small enough to make the instantaneous drain current a weak function of the change in V_{GS}. This relaxation stage is then followed by a complete turn-on of the sleep transistor. While the stepwise V_{GS} scheme can reduce the noise on VDDL node (power supply bounce) by limiting the current transient through the sleep transistor, ground bounce noise on the VGND node (the circuit ground) might still be observed.

In [6], the sleep transistor is implemented as a switched capacitor resistor. Two PMOS sleep transistors (M1 and M2 in Figure 1(c)) are stacked between the actual VDD and the VVDD node, with a metal-to-metal capacitor between them. Ground-bounce noise is reduced by controlling the PMOS sleep transistors through non-overlapping pulses generated by a control circuit. The presence of capacitor allows controlling the amount of charge supplied to logic during the change from the sleep to active mode and thus helps to reduce the ground bounce noise. First, a certain value of charge passes from VDD to the capacitor via M1 and then to the virtual VDD node through M2. As the process is repeated, VVDD eventually reaches the level of VDD and the circuit is ready for normal operation.

This configuration is applied to a circuit-under-test (CUT) designed and simulated in 65nm CMOS technology with a supply voltage of 1.2V. In our analysis, T_0 = 0ns represents the start of wake-up. It is observed that even though the charge is passed to the VVDD node in a gradual manner, two distinct peaks ($PEAK_1$ and $PEAK_2$ in Figure 2(a)) are observed on the VGND line. At a shorter period of the switched capacitor resistor, $PEAK_1$ being larger than $PEAK_2$ bounds the maximum noise observed and the presence of $PEAK_2$ can be disregarded as long as it remains smaller than $PEAK_1$. To obtain a better noise performance by limiting $PEAK_1$, the cycle period of input pulses to the switched capacitor resistor circuit can be increased at the cost of a longer wake-up time. An increase in switching period reduces the rate at which charge is transferred to the VVDD node and this may consequently further limit the maximum noise peak. However, at an increased switching period, even though $PEAK_1$ is reduced, which is what was expected, an interesting behavior with respect to $PEAK_2$ is observed. As is shown in Figure 2(b), $PEAK_2$ persists and is now larger than $PEAK_1$.



(a)



(b)

Figure 2: Transient plots of VGND during wake-up for a switched capacitor resistor at (a) switching period (T_{sw}) = 2ns (b) switching period = 2.5ns

The presence of two peaks and the emergence of $PEAK_2$ at a longer switching period leads us to make two important observations. First, the wake-up process has two critical transitions (corresponding to $PEAK_1$ and $PEAK_2$) where a sharp rise in voltage fluctuations on the VGND line is observed. Second, while increasing the equivalent resistance of the switched

capacitor resistor by increasing the switching period can limit the noise peak observed during the early stage of wake-up, the performance may still be limited by another noise peak following the first peak. Therefore, there is a need for a more efficient noise-aware power gating technique that accounts for and suppresses not just the power supply bounce but also the noise peaks observed on VGND during the wake-up power mode transition.

3. THREE-STEP POWER GATING TURN-ON TECHNIQUE

To better understand the origin of the noise peaks on VGND, we simulate the CUT comprising arithmetic and logic units by regulating the VVDD line with a constant current source (I=5mA). The constant current source acts as an ideal switched capacitor resistor providing a constant current irrespective of the voltage level on the VVDD node. Figure 3 shows the variations in some of the internal nodes as VVDD is charged by the constant current source.

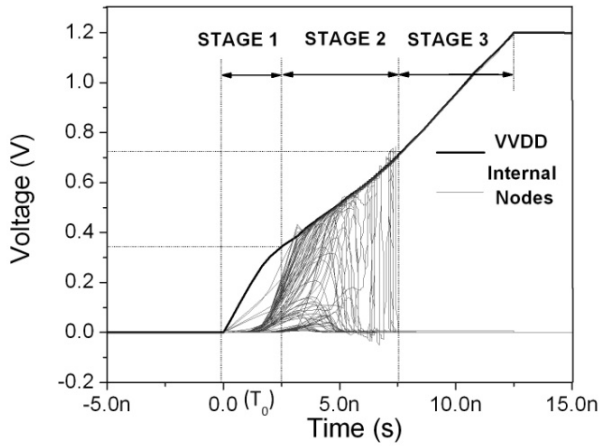


Figure 3: Transient behavior of internal circuit nodes with constant current source connected to VVDD.

We observed that the wake-up phase can be divided into three distinct stages, as explained below:

STAGE 1: At the start of simulation when VVDD has not yet reached $|V_{th,p}|$, the PMOS threshold voltage, the internal nodes see very little variation from their pre-wake up steady state values acquired during the sleep period. This is because the PMOS transistors connecting the VVDD line to the internal nodes are 'off', as their $|V_{GS}|$ values are below the PMOS threshold voltage. Thus, the current supplied to the circuit block is used exclusively to charge up the VVDD node. This is evidenced by a quick rise in the level of the VVDD node, as can be seen in Figure 3, and an almost zero current is observed flowing through VGND.

STAGE 2: As VVDD crosses the PMOS threshold, the PMOS transistors connected to the VVDD node are turned 'on' and consequently, the internal nodes start getting charged up. VVDD now charges up less rapidly than in STAGE 1 which is reflected in the different slopes of the rise in voltage at VVDD during STAGE 1 and STAGE 2 (see Figure 3). The charging of the internal nodes to intermediate voltage levels in turn creates a situation where some PMOS and NMOS transistors are simultaneously activated leading to short-circuit paths [7]. The transient current spurts due to these short-circuit paths in the logic can cause voltage fluctuations on the ground distribution network. Furthermore, the internal nodes in the immediate fan-out of the simultaneously 'on' PMOS and NMOS transistors become meta-stable and they build up charge as a result of contention between the NMOS and PMOS transistors connected to them. This stage is therefore characterized by the internal nodes fighting to align themselves either with VVDD or VGND.

Soon after the onset of STAGE 2, internal nodes begin to settle down. Accumulated charges on nodes stabilizing to the VGND value are dumped leading to a sudden surge in the current passing through VGND. Since an instantaneous change in the current is reflected as voltage fluctuations on the VGND line because of the parasitic impedances, this surge may correspond to $PEAK_1$ of Figure 2. During this period of metastability, large currents flow through the VGND node as the internal nodes fight to become consistent with either VVDD or VGND.

STAGE 3: It is then observed that after a period of metastability (VVDD ~ $|V_{th,p}|+V_{th,n}$), during which all circuit nodes either start following VVDD or become stable at the VGND value, no further activity is seen on the internal nodes. This is the final stage of the wake-up transition. It must be noted that the sum of PMOS and NMOS transistor thresholds is also the minimum difference between the circuit power supply and ground rails required for a circuit to perform its logic function correctly [8].

At the beginning of STAGE 3, the current supplied to the circuit block is used only to charge up those nodes that have started following the VVDD node. Therefore, only a very small current is observed at the VGND node. Again, since an instantaneous change in current manifests itself as ground bounce noise, this sudden drop in current at the transition boundary between STAGE 2 and STAGE 3 may correspond to $PEAK_2$ of Figure 2.

Based on this understanding of the three stages in the wake-up phase, we suggest the idea of adjusting the magnitude of the supply current at each stage to effectively reduce ground bounce. During STAGE 1, the VVDD node can be rapidly ramped up to a value just below $|V_{th,p}|$ as all the current through the PMOS sleep transistor would be used only to charge the VVDD node. Thus, if the current supply at STAGE 1 is increased, the wake-up time can be reduced without disrupting the VGND node. As the circuit's meta-stable region of operation extends through STAGE 2, there exist many potential paths between the VVDD and VGND line. Thus, if a large amount of current is supplied to VVDD, sharp instantaneous currents passing through to the VGND node can exacerbate the ground bounce behavior of the circuit. An effective approach to suppress noise peaks ($PEAK_1$ and $PEAK_2$) is to limit the amount of current in STAGE 2 to a small value and wait for the circuit nodes to settle down. The charge accumulation on the internal nodes during the meta-stable region of operation can be minimized by having a small amount of current available, and consequently the current surges due to the transition from metastability to steady values should be reduced. In STAGE 3, once the internal nodes have settled, VVDD can again be ramped up. All current supplied to the VVDD node in this stage is used only to charge up those internal nodes that have started following VVDD, while the nodes that have settled to the VGND value will remain unaffected. Thus, even though the power-gating circuit is relaxed during the circuit block's meta-stable region of operation

(STAGE 2), the total wake-up time can be maintained by boosting the power-gating circuit before and after STAGE 2.

The effect of using current sources with different values for three wake-up stages is corroborated by our simulations. Figure 4(a) shows the maximum peak-to-peak variation on the VGND line ($VGND_{PP}$) observed in STAGE 2 increases as the current value is increased. However, little or no ground bouncing is observed in STAGE 1 and STAGE 3 even for higher current levels. In Figure 4(b), it can be observed that for a very low current value of 0.3mA, a dip is seen on the VVDD node. This might happen when the logic block connected to the VVDD node pulls it down at a rate faster than it is charged up by the sleep transistor. As a result, the VVDD node does not rise monotonically and this elongates STAGE 2 and the entire wake-up process. Thus, the current level during STAGE 2 should be kept above a minimum level to ensure a monotonic charging up of the VVDD node.

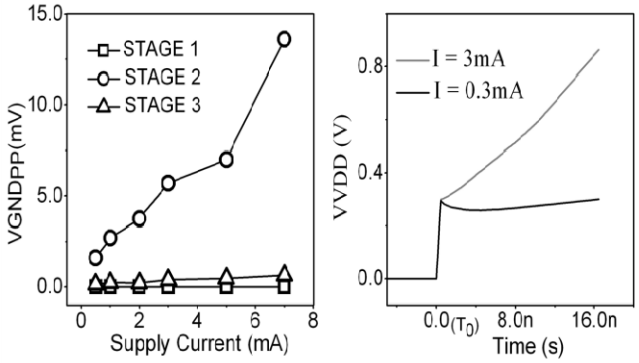


Figure 4: (a) Maximum Peak-to-peak variation on the VGND line with different current levels for the three wake-up stages (b) Dip in VVDD line for low- current levels during STAGE 2.

Based on these observations, we propose a three-stage power-gating scheme where, during STAGE 2, the current supplied by the power-gating circuit to the logic block is limited to a small value (VVDD charged up slowly) and in STAGE 1 and STAGE 3, is maintained at a higher value (VVDD charged up rapidly). This scheme of operation ensures that the noise on the VGND line is minimized during the entire wake-up transition of the logic block while maintaining the wake-up time. However, it is also observed that the current value during STAGE 2 cannot be too small.

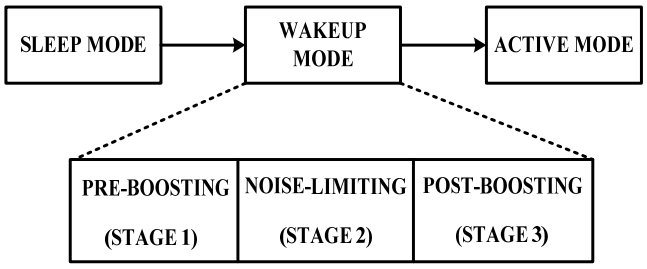


Figure 5: Three-stage wake-up mode

To implement the three-stage approach (Figure 5), we use a signal-control FSM described in Figure 6(a), (b). Depending on the state of the VVDD line, the FSM works in four stages: Sleep, Pre-boosting, Noise-limiting and Post-boosting. Pre-boosting stage corresponds to STAGE 1 while Noise-limiting and Post-boosting stages correspond to STAGE 2 and STAGE 3 respectively.

To generate input signals for the FSM, two analog comparators are used. They continuously monitor the VVDD line to generate two signals, MS_{START} and MS_{END}. The signals correspond to the start and end of STAGE 2 in the ALU logic. The value of REF1 (reference voltage level for the first comparator) is fixed at a value just less than the PMOS threshold voltage ($|V_{th,p}|-\Delta$) while the value of REF2 (reference voltage level for the second comparator) is kept at a value between VDD/2 and VDD ($\sim |V_{th,p}|+V_{th,n}$). Therefore, when VVDD reaches the value of REF1, MS_{START} goes high and when VVDD reaches the value of REF2, MS_{END} goes high. The low-to-high transitions of MS_{START} and MS_{END} signals push the FSM into 'Noise-limiting' and 'Post-boosting' stages respectively (Figure 6(a)).

The power gating circuit, shown in Figure 6(b) is implemented through three transistors M1, M2 and M3 connected in parallel between the supply and VVDD nodes. At the onset of wake-up, the FSM can transition into any of the three stages depending on the VVDD value at the end of the sleep period and feedback from the analog comparators. Assuming VVDD has discharged to a value close to GND, the power-gating circuit will first move into the 'Pre-boosting' stage. Since the idea is to rapidly increase the VVDD voltage to a value close to $|V_{th,p}|$, transistor M1 is used to provide a large current to the ALU logic block. It must be noted that the size of M1 is smaller than the size of the sleep transistor used in a conventional power gating structure. This is because of two reasons. First, a very large size for M1 will make it difficult to detect the start of metastability by the FSM as VVDD would reach $|V_{th,p}|$ very rapidly. Second, allowing very large currents through M1 initially will cause power supply bounce (noise on the VDDL node – the node VDDL is shown in Figure 6(a)) due to the large current transient at the start of wake-up. Thus, M1 is sized adequately to facilitate a rapid rise of VVDD while ensuring the noise on the power supply rail is not significant. It is controlled by the signal *Pre-boosting* which is first transitioned low at the start of wakeup by the FSM if both MS_{START} and MS_{END} signals are low and then transitioned high (and hence turning off M1) when VVDD reaches the value of REF1. At this instant, the FSM moves to the 'Noise-limiting' stage. The signal *Noise-limiting* transitions low and M2 starts conducting a small current through it. The power-gating circuit is now in a relaxation stage. M2 provides a small value of current to limit ground bouncing during the meta-stable region of operation. Finally, when the end of metastability is detected by the FSM (MS_{END} goes high), it moves into the 'Post-boosting' stage. The signal *Post-boosting* is transitioned low which powers on transistor M3. Transistor M3 is sized large to rapidly ramp the VDD voltage to the final supply value. When VVDD reaches the VDD value, the circuit is ready for operation (active mode).

Finally, when the sleep mode of operation (Wakeup = '0') is initiated, the FSM switches off all the transistors (M1-3) gating the supply line from the logic and the circuit enters the low-leakage sleep mode.

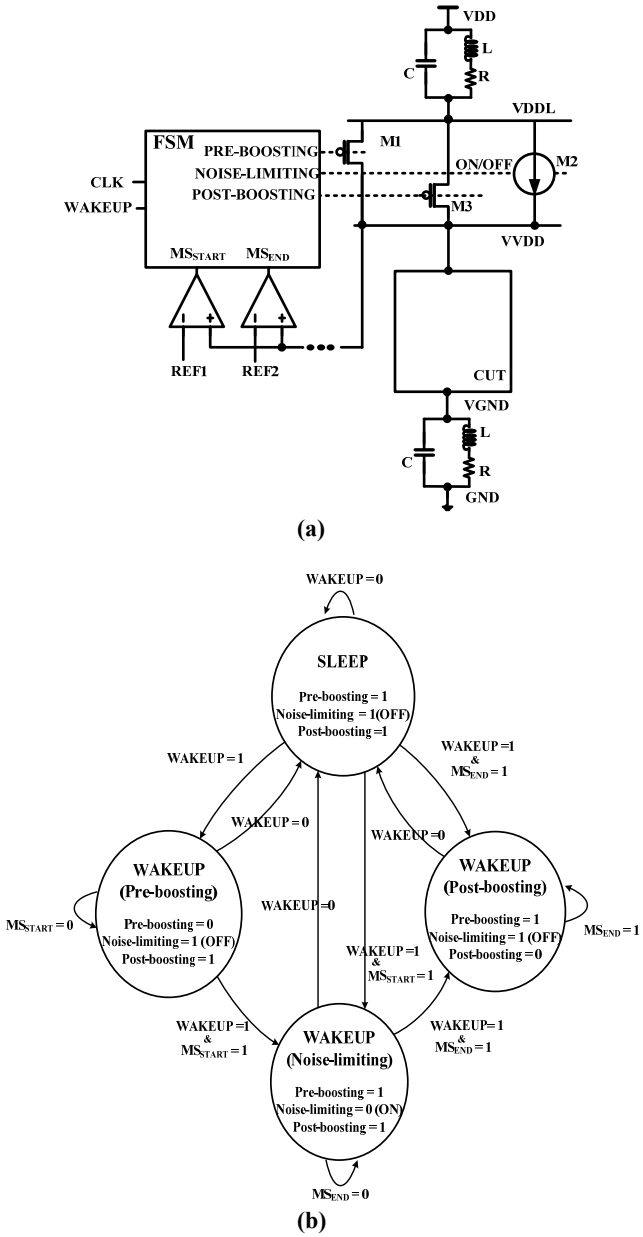


Figure 6: (a) Three-step turn-on power gating structure (b) Stages of the finite state machine.

4. SIMULATION RESULTS

The proposed three-step power gating scheme is used with two 16-bit ALU units designed and simulated in 65nm-1.2V CMOS process with package parasitics R=0.217Ω, C=5.32pF and L=8.18nH [6]. The simulation results are summarized in Table 1. The impact of inductive noise is compared in terms of eight parameters defined to characterize the ground bounce behavior [6]. V_{max}/VGND, V_{min}/VGND represent the highest and lowest levels of bounce on the VGND node while V_{pp}/VGND represents their difference - the maximum peak-to-peak variation. Similarly, V_{max}/VDDL, V_{min}/VDDL represents the highest and lowest values of deviation from the nominal value on the VDDL node while V_{pp}/VDDL represents the peak-to-peak difference. $I1_{max}$/R and $I2_{max}$/R are, respectively, the maximum current observed flowing through the parasitic resistance connected to VGND and VDDL nodes during wake-up.

The maximum magnitude of voltage glitches on the VGND rail of the ALUs with the three-step turn-on power gating structure is reduced by up to 92% and 94% respectively, compared to the ALUs with a conventional gating scheme. The corresponding reduction for the VDDL node is 60% and 82%. The peak current flowing through the parasitics is also reduced by up to 91% ($I1_{max}$/R) and 83% ($I2_{max}$/R). Thus, the proposed scheme achieves a significant reduction of the inductive bounce noise at both the VGND and VDDL nodes. The corresponding figures for the reduction of the bounce noise are between 30-to-74% for the stepwise VGS scheme and between 20-to-79% for the switched capacitor scheme. Clearly, the three-step turn-on scheme achieves superior noise reduction compared to previously proposed power gating structures. It must also be noted that the three-step turn-on scheme effectively suppresses any noise peaks during the entire wake-up transition as the disruption seen on the VGND and VDDL rails is always within ±5% of the full rail-to-rail swing. Thus, neighboring circuits can remain running and the wake-up of the circuit block coming out of the sleep mode will not disrupt their correct functioning.

In addition to the inductive noise minimization, the three-step turn-on scheme can also be advantageous in terms of the time taken for the VVDD node to reach the final supply value. While the switched capacitor scheme charges up the VVDD node slowly, the stepwise VGS scheme may require a long relaxation stage to limit the noise. In contrast, the boosting stages before and after the relaxation stage (the Noise-limiting stage) in the proposed scheme can help to reduce the time penalty.

Table 1: Comparison of metrics of three-step turn-on scheme with other power gating structures. Figures in brackets represent the percentage reduction when compared with the conventional abrupt turn-on technique.

	V_{max}/VGND (mV)	V_{min}/VGND (mV)	V_{PP}/VGND (mV)	V_{max}/VDDL (mV)	V_{min}/VDDL (mV)	V_{PP}/VDDL (mV)	$I1_{max}$/R (mA)	$I2_{max}$/R (mA)
Stepwise V_{GS} scheme	60.7 (-60%)	-56.4 (-74%)	117.1 (-69%)	69.9 (-30%)	217 (-33%)	286.7 (-32%)	6.14 (-65%)	10.5 (-40%)
Switched Capacitor Resistor	51.7 (-66%)	-45.4 (-79%)	97.1 (-74%)	82 (-20%)	100.5 (-68.8%)	182.5 (-58%)	2.36 (-88%)	3.05 (-83%)
Three-step Turn-On	12.13 (**-92%**)	-12.88 (**-94%**)	25.01 (**-93%**)	39.7 (**-60%**)	60 (**-82%**)	99.7 (**-77%**)	1.58 (**-91%**)	3.1 (**-83%**)

5. CONCLUSION

This paper introduces a novel scheme for implementing the wake-up transition of a power-gating circuit in a controlled three-step manner. Based on the state of the internal nodes, the wake-up mode is divided into three stages: Pre-boosting, Noise-limiting and Post-boosting. A large current is provided to the logic block during the Pre-boosting and the Post-boosting stages while a limited current is supplied in the Noise-limiting stage. Transition between the stages is controlled by a signal-control FSM which utilizes feedback from the virtual VDD node to force the power-gating circuit into one of the three stages. Simulation results on two ALU units built with 65nm-1.2V CMOS process demonstrates that all inductive noise peaks are limited to less than 5% of the full rail-to-rail swing during the entire period of wake-up transition.

6. ACKNOWLEDGEMENT

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