A HIGH RESOLUTION CAPACITANCE DEVIATION-TO-DIGITAL CONVERTER UTILIZING TIME STRETCHING

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ABSTRACT

We present a capacitance deviation-to-digital converter (CDC) for the thin membrane transducers (TMT) used for bio-molecular detection. Our CDC consists of a capacitance deviation-to-time converter (CTC), time-stretchers, and a time-to-digital converter (TDC). The time-stretchers are innovatively adopted to achieve higher resolution of the CDC with expanse of moderate power consumption. Designed and simulated in 0.35um CMOS bulk technology, the CDC has a resolution of 370aF with a maximum error of 0.027‰, at a rate of 700 samples per second.

I. INTRODUCTION

The chemo-mechanical transduction of bio-chemical events has recently attracted significant interests due to advantages such as high specificity and label-free assay. Micro-cantilever techniques, mainly employing optical detection, have become especially popular. However, it is difficult to realize such techniques as compact devices due to the bulk of the optical setup that is required.

The recently introduced thin-membrane transducer (TMT) [1] provides highly sensitive capacitive detection and also avoids design constraints for metal-oxide semiconductor field effect transistor (MOSFET). As shown in Fig.1, a bio-molecular reaction induces tensile and compressive stresses in a TMT, making it dome shape flatter or more rounded, which in turn alters its capacitance. Fig. 1 also shows has a second TMT structure, which is sensitized to the target event, can be used to compensate for spurious deflection of the dome caused by environmental change.

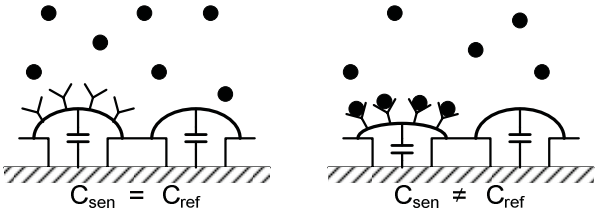

Figure 1: A thin membrane transducer (TMT).

A readout integrated circuit based on capacitance-to-voltage followed by voltage-to-digital conversion, is widely used in conjunction with capacitive sensors, such as the TMT; this type of IC has high signal-to-noise ratio and sensitivity [2]. However, as the supply voltage scales down in conventional capacitance deviation-to-digital (CDC) circuits some shortcomings occur. One of these problems is that voltage references are less stable than frequency references, so that quantization of voltage is less accurate than that of time [3]. Therefore, conventional CDCs, which quantize time, usually use a single counter for digitization [4].

The CDCs with a single counter have the further shortcoming that the operating clock frequency limits their resolution. Of course, increasing the clock frequency can improve the resolution, but that results in a proportional increase in the power consumption of the circuit.

To cope with the problems described above, we propose a novel CDC architecture, which is the first to use a time stretching scheme. This design achieves higher resolution without excessive power consumption.

II. CAPACITANCE DEVIATION-TO-DIGITAL CONVERTER BASED ON TIME-STRECHING

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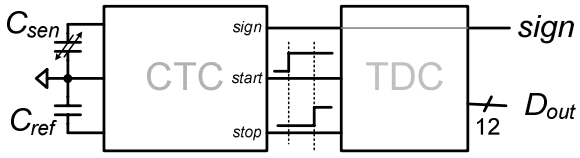
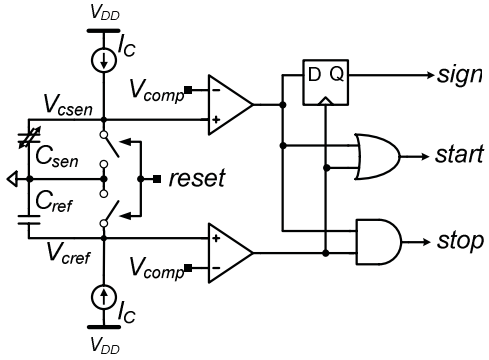


Figure 2: Block diagram of the proposed capacitance deviation-to-digital converter, which consists of a capacitance deviation-to-time converter (CTC) and a time-to-digital converter (TDC).

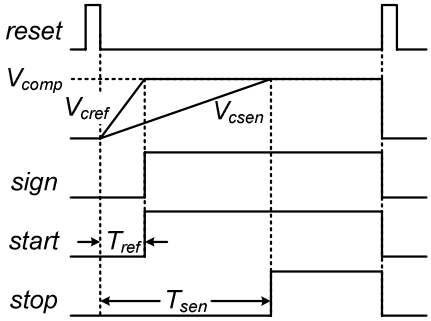
Our CDC circuit is composed of a capacitance deviation-to-time converter (CTC) and a time-to-digital converter (TDC). As shown in Fig. 2 the difference in capacitance between the sensor capacitor and the reference capacitor generates *sign*, the *start* and *stop* signals. The *sign* indicates whether the sensor or the reference capacitor have the higher capacitance. The time difference between the *start* and the *stop* signals is digitized by the TDC, generating digital code (D_{out}); in the content of the sign signal, this represent the difference in capacitance that we are trying to measure.

A. Capacitance Deviation-to-Time Converter

The CTC requires an independent constant current source and comparator for each capacitor. If the sensor capacitor is smaller than the reference capacitor, the sign signal voltage becomes low; if the sensor capacitor is larger, the voltage is high. The *start* and *stop* signals are inserted in the correct order regardless of the order in which comparator outputs become high. This is achieved by the logic shown in Fig. 3(a).



(a)



(b)

Figure 3: (a) The capacitance deviation-to-time converter and (b) its timing diagram.

The TDC repeatedly cycles through four phases: reset, charging, comparison, and wait. During the reset phase, the *reset* signal is high and the reset switches discharge both the sensor and reference capacitors to the same initial state. At the start of the charging, both current sources begin to charge each capacitor. When the output voltage of either comparator goes high, so does the *start* signal. The comparison phase new begins; it measures the length of time during which the *start* signal stays high and the *stop* signal stays low. When both the *start* and *stop* signals are high, the wait phase begins, during which the CTC circuit is merely waiting for another reset, at which point the cycle begins again.

If the charging current is I_C, the voltage level detected by the comparators is V_{comp}, and capacitance of the sensor and reference capacitors are C_{sen} and C_{ref} respectively, as shown in Fig. 3 (a), then the charging times are given as follows:

$$T_{sen} = \frac{C_{sen} \cdot V_{comp}}{I_C} \quad . \tag{1}$$

$$T_{ref} = \frac{C_{ref} \cdot V_{comp}}{I_C} \quad . \tag{2}$$

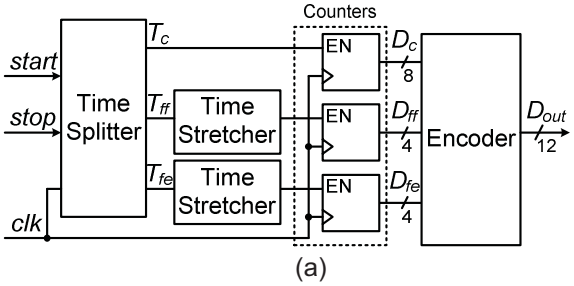
The difference in charging time is proportional to the difference in capacitance:

$$\left|T_{sen} - T_{ref}\right| = \frac{V_{comp}}{I_C} \cdot \left|C_{sen} - C_{ref}\right| = k \cdot \Delta C \quad ,$$

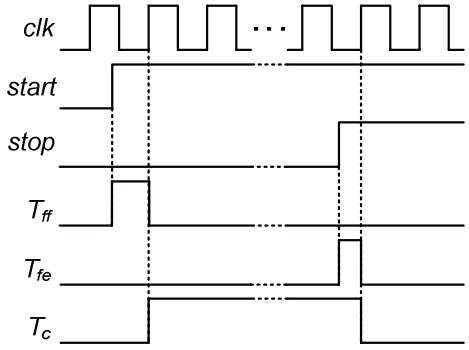
where $k = \frac{V_{comp}}{I_C}$ and $\Delta C = \left|C_{sen} - C_{ref}\right|$. (3)

B. Time-to-Digital Converter

Conventional time-to-digital conversion uses a single counter that digitizes time by counting clock cycles. Therefore, the resolution of such a CDC cannot be smaller than the time period of the operating clock [5]. To overcome this limitation, the proposed circuit measures fraction of clock cycles, as shown in Fig. 4(a).



(a)



(b)

Figure 4: (a) The time-to-digital converter (TDC) and (b) the timing diagram of the time-splitter input and output signals. The time-splitter in the TDC generates the coarse time signal T_c and the fine time signals T_{ff} and T_{fe}.

The time-splitter in the TDC divides the time between the *start* and *stop* signals into three parts, T_c, T_{ff} and T_{fe}. The coarse time T_c is synchronized with the rising edge of the operating clock *clk*, and measured by an 8-bit counter. The periods T_{ff} and T_{fe} represent the fractions of a tick before and after the interval measured by T_c. Each of these fractional intervals is assigned to its own time-stretcher.

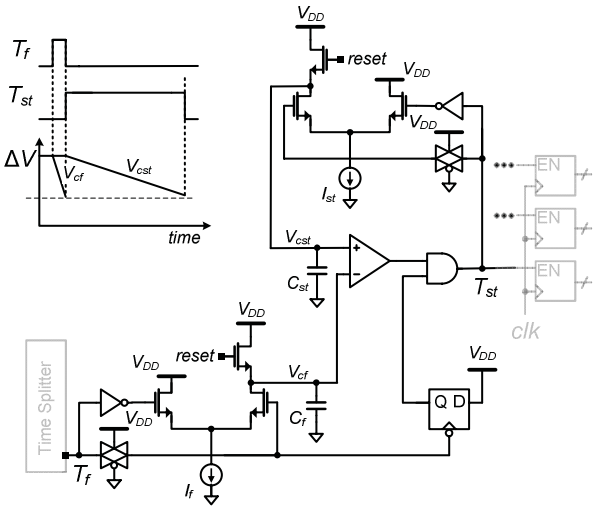


Figure 5: A time stretcher.

When the fine time-signal T_f, which may be either T_{ff} or T_{fe}, arrives at the input of the time-stretcher illustrated in Fig. 5, the input differential NMOS pair discharges the capacitor C_f for the duration of T_f, with a current of I_f, which reduces the voltage node across C_f by ΔV. As soon as T_f ends, the other NMOS pair will discharge the capacitor C_{st}. Since the current across each pair and the capacitance to which it is connected to, are different, the stretched time T_{st} can be computed as follows:

$$\Delta V = \frac{I_f}{C_f} \cdot T_f \quad . \tag{4}$$

$$T_{st} = \frac{C_{st}}{I_{st}} \cdot \Delta V = \frac{C_{st}}{C_f} \cdot \frac{I_f}{I_{st}} \cdot T_f = M \cdot N \cdot T_f \quad ,$$

$$\text{where } C_{st} = M \cdot C_f \text{ and } I_{st} = I_f / N \quad . \tag{5}$$

The outputs of the time-stretchers digitized to digital codes D_{ff} and D_{fe} by 4-bit counters. The encoder receives all three kinds of digital codes, D_c, D_{ff} and D_{fe}, from which it calculates a 12-bit digital code, D_{out} as follows:

$$D_{out} = D_C \cdot 2^4 + \left(D_{ff} - D_{fe} \right) \quad . \tag{6}$$

III. SIMULATION RESULTS

We designed and simulated the CDC circuit in 0.35μm CMOS bulk technology with a supply voltage of 3.3V, and nominal initial values of the

reference and sensor capacitors of 20pF. The components in the time-stretcher were sized as follows: C_f =1.1pF, C_{st} =4.4pF, I_f = 1μA, and I_{st} = 0.25μA. As results, the time-stretchers have the stretching factor of 16.

The proposed architecture with 12-bit digital output achieves a resolution of 370aF at a conversion rate of over 700 samples per second, with a clock frequency of 1MHz. The error characteristics shown in Fig. 6 demonstrate that the proposed circuit achieves an error of less than 0.027‰.

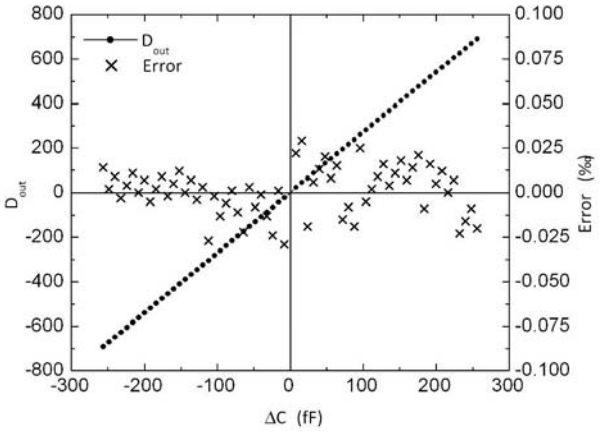


Figure 6: Digital output and error characteristics of the proposed CDC as a function of sensor capacitance deviation.

We can attribute the error to reveal causes: (a) an inaccurate time-signal from the CTC circuit, due to comparator offset, parasitic capacitance, and channel length modulation of the current source; (b) a nonlinear response by the comparators in the time-stretchers, because integral non-linearity (INL) and differential non-linearity (DNL) of the time-stretcher are approximately 0.408 LSB and 0.556 LSB respectively; and (c) quantization errors caused by asynchronous issues of the *start* and *stop* signals to the TDC.

IV. CONCLUSION

We have proposed low-power and high-resolution capacitance deviation-to-time converter for TMT-based bio-sensor, which makes innovative use time stretching. Designed and simulated in 0.35um CMOS bulk technology with a 3.3V supply, the circuit was able to measure difference in capacitance of 370aF, with an accuracy of 0.027‰, at a rate of 700 samples per second conversion rate.

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