A PVT-INSENSITIVE TIME-TO-DIGITAL CONVERTER USING FRACTIONAL DIFFERENCE VERNIER DELAY LINES

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ABSTRACT

We propose a high-resolution 8-bit time-to-digital converter that uses two-level fractional difference conversion to reduce area and power consumption. Two delay-locked loops stabilize the propagation delay in the upper and lower buffer chains of the Vernier delay line that is used to make the measurement. In a transistor-level simulation using 0.35um technology, this architecture achieves a resolution of 24ps with a 22ps single-shot accuracy. The maximum sampling rate exceeds 5MS/s and the total power consumption is 8.81mW.

I. INTRODUCTION

High-resolution time-to-digital converters (TDC) have found applications in many areas, including capacitive sensor readouts [1], all-digital phase-locked loops [2], and built-in self-test jitter measurement [3]. A number of different TDC schemes have been proposed, and those capable of high resolution can be classified into two different types: indirect and direct conversion scheme.

Indirect conversion TDCs usually have a time-to-analog (TAC) stage and an analog-to-digital (ADC) stage. Ramp TDCs [4] and dual-slope TDCs [5] are of this type. In a dual-slope TDC circuit, one capacitor is discharged to a reference level by a rundown current which is relatively large in the content of the time interval to be measured. The time to discharge the other capacitors to the same reference level is sampled by an external clock. A state-of-the-art dual-slope TDC can achieve a resolution as high as 50ps with a power consumption of 0.75mW [5]. One disadvantage of indirect conversion schemes is the extra error caused by the TAC stage. During time-to-voltage conversion, the signal is distorted due to the nonlinearity of the capacitors and the leakage current. Another disadvantage of this type of circuit is the low sampling-rate, which focus a trade-off between resolution and conversion time.

In direct TDC circuits, delay lines are usually used to measure the fine interval between the rising edges of the start and stop signals. The simplest arrangement is a tapped delay line with one D flip-flop (DFF) connected to each tap. In this case the resolution is the propagation delay of a single delay buffer.

Higher resolutions can be achieved using a Vernier delay line (VDL), as shown in Figure 1. The propagation delay t_{d1} in the upper buffer chain is slightly larger than the propagation delay t_{d2} in the lower chain, and the resolution is the difference between these two delays.

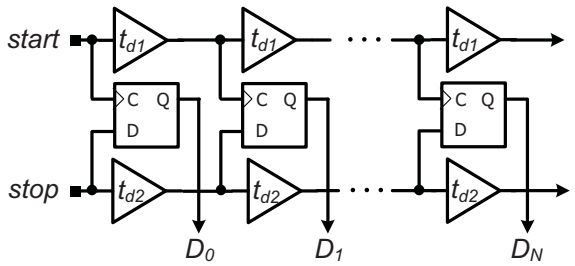

Figure 1: A Vernier delay line.

One of the main problems with the use of VDL in a TDC is the effect of variations in process, voltage and temperature (PVT). Delay-locked-loops (DLLs) can be used to provide negative

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feedback [6] that compensates for PVT variation; however, this incurs the cost of a significant increase in power consumption.

In this paper, we propose a novel TDC architecture, based on Vernier delay line, which employs a two-level fractional-difference conversion scheme to economize in both area and power.

II. CIRCUIT DESCRIPTION

The conventional configuration of a DLL-stabilized VDL circuit [6] is shown in Figure 1 and the resolution of the resulting TDC with Mf_0 reference clock can be formulated as follows:

$$t_R = \frac{T_{clk0}}{MN}, \tag{1}$$

where N is the number of stages in the VDL and T_{clk0} is $1/f_0$. This equation expresses the trade-off among resolution, power and the number of VDL stages. Resolution can be improved using higher reference clock frequency or more VDL stages, at the cost of increased power consumption or area.

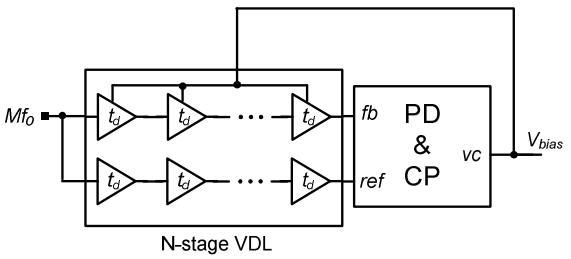

Figure 2: Conventional configuration of a DLL-stabilized Vernier delay- line TDC.

Hwang et al. [7] proposed a TDC utilizing dual-DLL architecture, in which each DLL contains N- or (N+1)-stage delay buffers respectively. A particular resolution can be achieved by lowering the clock frequency or reducing the number of VDL stages, compared to a DLL-stabilized VDL TDC [6]. For the same reference clock Mf_0, the enhanced resolution achieved in this way can be expressed as follows:

$$t_R' = \frac{T_{clk0}}{MN^2}. \tag{2}$$

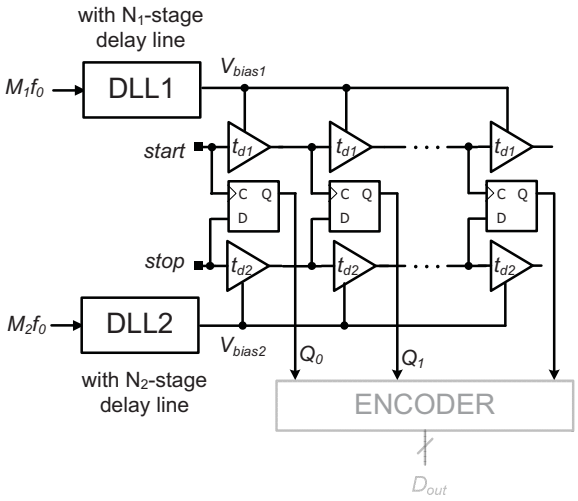

Figure 3: A time-to-digital converter with two-level fractional difference conversion scheme.

The time resolution can be further enhanced by the two-level fractional difference conversion scheme that we propose, which is shown in Figure 3. The circuit is mainly composed of two DLLs (DLL1 and DLL2) and VDL. DLL1 generates the bias voltage V_{bias1} for the upper chain of the VDL, and DLL2 generates the bias voltage V_{bias2} for the lower chain. DLL1 and DLL2 have with different numbers of delay line stages, and operate at fractional frequencies. The resolution of DLL1 and DLL2 can be expressed as follows:

$$t_{R1} = \frac{T_{clk0}}{N_1 M_1}, \tag{3}$$

$$t_{R2} = \frac{T_{clk0}}{N_2 M_2}, \tag{4}$$

And the overall TDC resolution can then be obtained as:

$$t_R'' = \left| t_{R2} - t_{R1} \right| = \frac{\left| N_2 M_2 - N_1 M_1 \right|}{N_2 M_2 N_1 M_1} T_{clk0}. \tag{5}$$

By an appreciate choice of N_1, N_2, M_2, M_1, we can make the numerator in this equation equal to 1 and the expression then reduces

$$t_R'' = \frac{T_{clk0}}{N_2 M_2 N_1 M_1}. \tag{6}$$

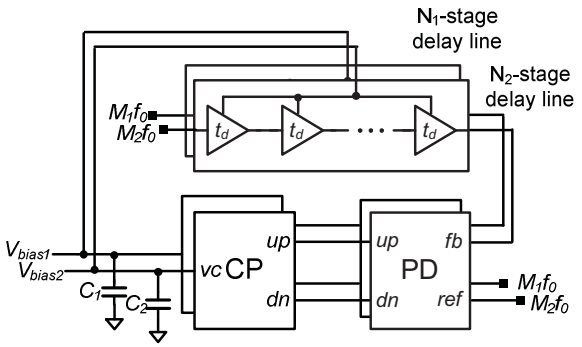

Figure 4: The two DLLs in the proposed two-level fractional difference converter. Each DLL consists of a phase detector (PD), a charge pump (CP), a capacitor, and a delay line.

To compare the performance of our scheme with that of the previously published dual-DLL scheme [7], we assume that both schemes have the same number of delay states, so that

$$2N+1 = N_1 + N_2 . \tag{7}$$

We assume that the dual-DLL scheme is operating at the higher frequencies of our two DLLs, so that

$$M = \max(M_1, M_2) . \tag{8}$$

Thus,

$$\begin{aligned} \frac{t_R^{'}}{t_R^{''}} &= \frac{N_1 N_2 M_1 M_2}{\left(\frac{N_1+N_2-1}{2}\right)^2 \max(M_1, M_2)} \\ &= \min(M_1, M_2)\frac{\left(N_1+N_2\right)^2-\left(N_1-N_2\right)^2}{\left(N_1+N_2-1\right)^2} \\ &> \min(M_1, M_2)\left(1-\alpha^2\right) \end{aligned} \tag{9}$$

where

$$\alpha = \frac{\left|N_1-N_2\right|}{N_1+N_2} . \tag{10}$$

By carefully choosing, N_1, N_2, M_2, M_1, we can make α < 0.2. Thus, the resolution of this circuit is better than that of dual-DLL circuit by a factor of at least 0.96·min(M_2, M_1), even though one DLL is operating at a lower frequency.

The Load capacitances in the upper and lower chains of the VDL should be carefully matched with those of DLL1 and DLL2 respectively, to ensure that they produce the same delay. The inequality $N_2M_2 > N_1M_1$ must also be satisfied in order to ensure that the propagation delay in the upper chain is slightly larger than that in the lower chain.

III. SIMULATION RESULTS

The proposed scheme was simulated in 0.35μm CMOS technology with a supply voltage of 3.3V. Clock frequencies of 125MHz and 83.3MHz were selected for DLL1 and DLL2 respectively. There were 19 delay buffers in DLL1 and 13 in DLL2. The simulated TDC output and error characteristic are shown in Figure 5.

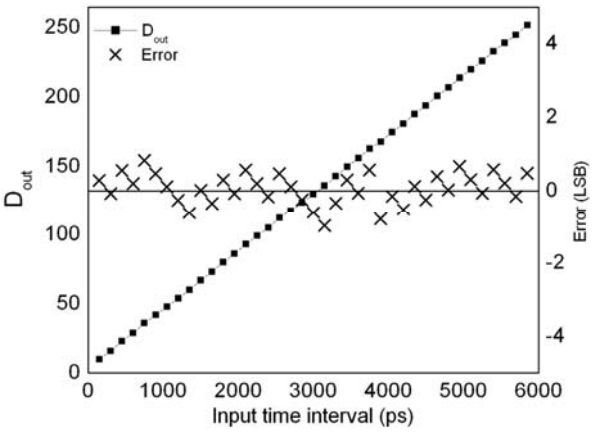

Figure 5: Output and error of the proposed TDC as a function of the input time interval.

The TDC achieves a resolution of 24ps with a single-shot accuracy of 22ps. The maximum error is 0.91 of the least significant bit (LSB).

We found that there is deviation between the simulated and calculated resolution, which can be mainly attributed to two factors: 1) Imperfect phase match in the DLLs caused by dynamic phase detector (PD). 2) Imperfect matching of the load between the delay line of the VDL and the DLLs. Although the load elements in the VDL and the DLLs are identical, transistors in the FFs may have different gate voltages, resulting mismatch in self-capacitance between the delay lines in the VDL and DLL.

Simulation results show the power consumption to be 8.81mW. Sampling rate exceeds 5MS/s. Table 1 summarizes the performance of our TDC circuit and compares it with other delay-stabilized Vernier TDCs of comparable resolution. It is apparent that the two-level fractional-difference conversion scheme is highly competitive in terms of power consumption.

Table 1: Summary and comparison of the proposed TDC performance

Parameter	[7]	[8]	[9]	This work
Technology	0.35um	0.7um	0.35um	0.35um
LSB	24~30ps	48.8ps	37.5ps	24ps
Input range	>6100ps	-	>50ns	>5900ps
Clock frequency	130~ 160MHz	-	-	83.3MHz and 125MHz
Sampling rate	-	-	168kS/	>5MS/s
Supply voltage	3.0~3.6V	5V	3.0~3.9V	3.3V
Power	<50mW	110mW	150mW	8.81mW
Error	1.5LSB	0.37LSB	0.35LSB	<0.91LSB

IV. CONCLUSION

We propose the use of two-level fractional-difference conversion technique to reduce the area and power consumption in the implementation of a high-resolution time-to-digital conversion. Simulation results show that the circuit has a resolution as high as 24ps with a 22ps single-shot accuracy. The low power consumption of our TDC makes it a serious competitor with otherwise comparable PVT- insensitive TDC circuits.

ACKNOWLEDEGMENTS

The authors would like to thank for the financial support from System IC 2010 Program of the Ministry of Knowledge Economy, Nano IP/SoC Promotion Group of Seoul R&BD Program, and Agency for Defense Development.

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