A Fast-Locking CDR Circuit with an Autonomously Reconfigurable Charge Pump and Loop Filter

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Abstract— **This paper presents the design of a phase-locked loop (PLL) based clock and data recovery (CDR) circuit that meets fast locking and low jitter. We reduce the locking time of a CDR circuit using a new autonomously reconfigurable charge pump and loop filter in a 1.25Gb/s CDR circuit. An experimental prototype was implemented in a 0.18 μm standard CMOS technology. A receiver that incorporates our CDR circuit has an active area of 380 μm×350 μm.**

I. Introduction

Successive improvements in CMOS fabrication technology have led to a continuing exponential increase in the internal operating speed of a chip, which may now consist of tens of millions of transistors. However, I/O bandwidth is constrained by pins, packages, and channel environments, which are becoming the primary bottleneck in a system.

CDR circuits are commonly used in high-speed data transmission systems such as Ethernet receivers, disk drive read and write channels, digital mobile receivers, and high-speed memory interfaces. The phase-locked loop (PLL) is a popular basis for clock and data recovery (CDR) architectures. For networks with fast switching between nodes, short locking time reduces the number of preamble bits required and results in higher efficiency. Low jitter is important in achieving low bit-error rate (BER) in data transfer. Therefore, the CDR circuits not only require clock signals with low noise, or jitter, but should also achieve fast locking. Adaptive bandwidth and gear-shifting algorithms have been proposed [1]-[5] to achieve this combination, but these schemes consume a lot of power, require a large die size.

In this paper, we present a 1.25Gb/s CDR circuit whose locking time is reduced by the introduction of a new autonomously reconfigurable charge pump and loop filter into phase-locked loop (PLL) based clock and data recovery (CDR) architecture. This scheme makes it possible to change the bandwidth of the circuit's response thereby reducing the locking time without loss of stability. Additionally, it can also be used for PLL as well as CDR circuit. A prototype has been fabricated in 0.18 μm standard CMOS technology, using a 1.8V supply.

II. Architecture of Clock and Data Recovery (CDR) Circuits

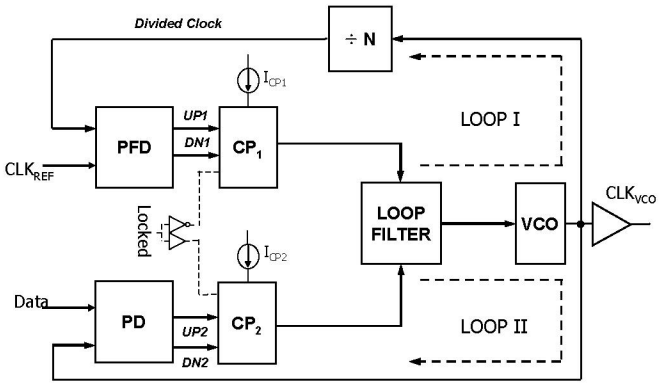

Fig. 1 Clock and data recovery circuit architecture

A clock and data recovery (CDR) circuit must be designed to perform frequency and phase acquisition in a way that achieves robust locking. Most CDRs include a frequency detector (FD) from their implementation, because many serial-link applications specify that the CDR must operate in a plesiochronous condition. In a plesiochronous system, the receiver is already aware of the data rate, subject

to only a small uncertainty. Therefore, the majority of CDRs use an external clock source as a frequency reference.

Fig. 1 shows a general architecture that acquires frequency and phase lock in two steps [6]. The architecture of CDR has been realized as a two-loop structure consisting of LOOP I and LOOP II, each of which is capable of processing the incoming local reference clock and high-speed random data. At start up, using a single VCO, the LOOP I provides locking to the system frequency with the help of the reference clock. The lock detector monitors the frequency error, which is the difference between the reference frequency and the dividend frequency. After the VCO clock reaches a system frequency, the LOCK signal is generated and the LOOP I is turned off while the LOOP II is turned on. In other words, it disables the LOOP I and enables the LOOP II when the error drops to the sufficiently small value. LOOP II tracks the phase of the generated clock with respect to the data and aligns the VCO clock such that its rising edge is in the middle of data eye. The lock detector continues to operate so that LOOP I can be re-activated if the lock is lost as a result of unexpected noise.

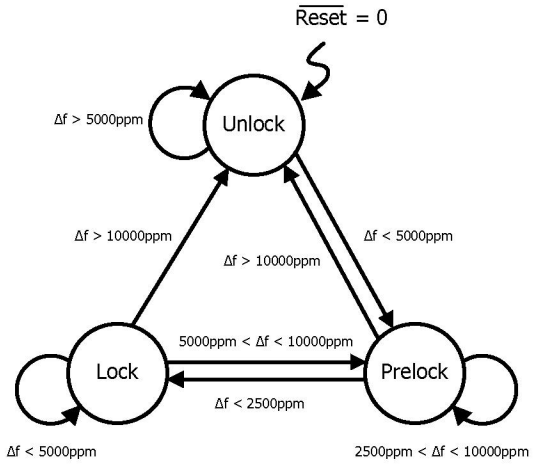

Fig. 2 The state diagram of lock detector

The lock detector is generally used in order to monitor the status of the phase locking operation. In two-loop clock and data recovery circuits, lock detector has two main responsibilities. One is to monitor the status of the locking process and to enable or disable LOOP I, when the clock frequency is close to its target, the other the lock detector determines whether a divided version of the recovered clock is within a predetermined frequency window about the reference clock. If the recovered clock falls outside the window, the lock detector activates the Loop I. The frequency lock detector has hysteresis for a clean transition of loop control from LOOP I to LOOP II. In addition to these functionality, in this work, we introduce additional *PRELOCK* signal which indicates that the CDR is about to be locked. The *PRELOCK* signal is activated within a wider error margin than the lock signal, and changes the CDR's charge pump current and the loop filter's capacitances. By switching these, it is possible to change the bandwidth without a loss of stability thereby decreasing lock time. The state diagram of the lock detector in this work is given in Fig. 2.

II. Autonomously Reconfigurable Charge Pump and Loop Filter

It is difficult to design a clock and data recovery (CDR) circuit to achieve fast locking as well as low jitter. Our CDR meets these simultaneous requirements through dynamic reconfiguration of the charge pump current and loop filter parameters.

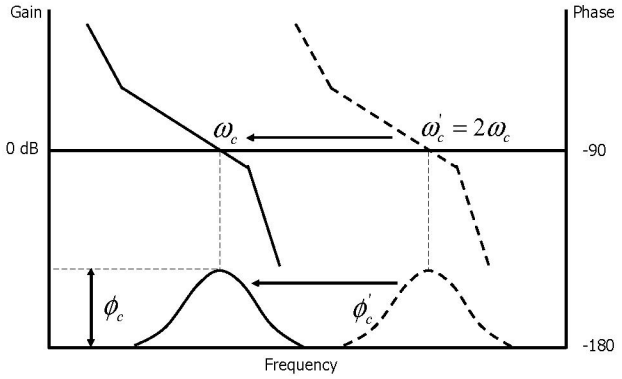

Fig. 3 Bode plot of the open loop response [8], [9]

The open-loop gain of the PLL is the product of the gain of the phase frequency detector and charge pump, the VCO gain, and the loop filter gain, divided by the gain of the feedback counter modulus N. A plot of the open loop gain and phase for a stable loop using 2nd order loop filter is shown in Fig. 3. The phase margin ϕ_c is defined as the angle between 180 degrees and the phase of the open-loop transfer function at the frequency corresponding to 0dB gain, and this is typically set more than 45 degrees [7].

We would ideally like to shift the curve of Fig. 3 over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open-loop gain and phase relationships. These curves give the same phase margin and so the PLL will usually be stable. To maintain the same relationship between gain and phase at twice the original cutoff frequency, the open-loop bandwidth equation should be compensated.

Increasing the charge pump current by a factor of K^2 while reducing the loop filter resistance by K increases the loop bandwidth by K while leaving the phase margin unchanged. For example, to increase the loop bandwidth by a factor of 2 for the wide bandwidth mode, the charge pump current may be increased by a factor of 4 while the loop filter

resistance is decreased by a factor of 2. Similarly, to decrease the loop bandwidth to the narrow bandwidth mode, the charge pump current may be reduced by a factor of 4 while the loop filter resistance is increased by a factor of 2. In these designs, when the PLL has locked or is close to lock, the loop bandwidth is reduced again to lower phase noise and spurious by alleviating the charge pump current to the charge pump's minimum value. Simultaneously, the loop filter switch is off to increase the zero resistance again to restore the phase margin.

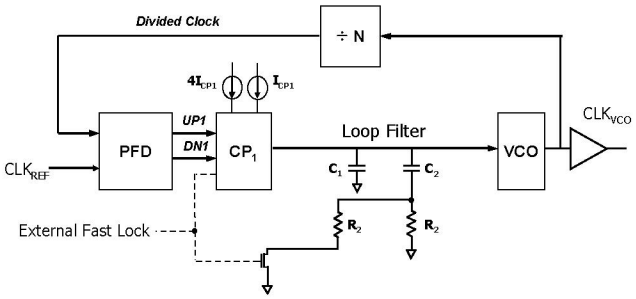

Fig. 4 An existing fast-locking PLL architecture [8]

Fig. 4 shows an existing fast-locking PLL design [8]. This circuit can be tuned to achieve a stable loop and fast locking by changing the loop filter resistance and the charge pump current. The charge pump circuit receives an input which makes it deliver 4 times the normal current per unit phase error, while an open- drain CMOS on-chip device switches in a second resistor element, R_2, which is connected to ground. The device configuration ensures that if a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations. Once locked on to the correct frequency, the PLL will then return to its standard, low-noise operation. The change between fast-locking and low-jitter mode is effectively seamless. However, this design requires a larger area because of the extra resistor that must be connected in parallel to halve the value of the loop filter resistance. What is more significant is that a higher charge pump current is needed to guarantee the stability of the loop. Additionally, this design suffers from an excessively large disturbance to the frequency and phase settling transients when the bandwidth is reduced. This disturbance takes a long time to settle out since the bandwidth is reduced and the loop time constants have increased. The major cause of this disturbance is that the current flowing in the loop filter resistor can still be large when the loop filter resistance is increased. Achieving fast-locking or low-jitter by changing the resistance also disturbs the control voltage during the transition between fast-locking and low-jitter modes. Furthermore, the VCO frequency may jump out of the capture range.

However, to mitigate the above problems, increasing the charge pump current by a factor of K while decreasing the loop filter capacitance by K increases the loop bandwidth by K while leaving the phase margin unchanged. For the same case, to increase the loop bandwidth by a factor of 2 for wide bandwidth mode, the charge pump current may be increased by a factor of 2 while the loop filter capacitance is decreased by a factor of 2. In the same way, to decrease the loop bandwidth to narrow bandwidth mode, the charge pump current may be reduced by a factor of 2 while the loop filter capacitance is increased by a factor of 2.

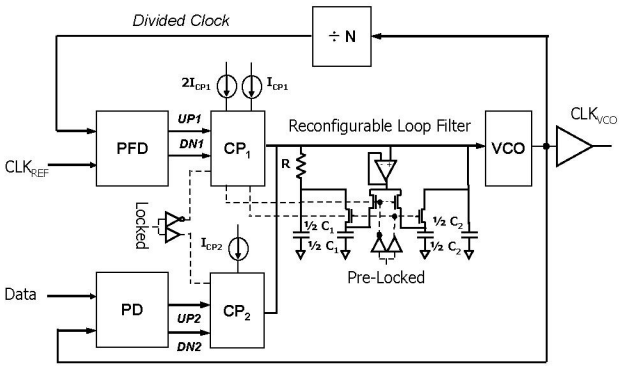

Fig. 5 Autonomously reconfigurable architecture

Fig. 5 shows the structure of our autonomously reconfigurable charge pump and loop filter. Compared to Fig. 4, we present a lock detector which is integrated on chip and includes *PRELOCK* signal that is used for an autonomously reconfigurable charge pump and loop filter. It is difficult to change K_{VCO} directly, but the charge pump current and loop filter parameters are relatively easy to adjust. The charge pump current only needs to be doubled to achieve a fast-locking mode. Changing the capacitance has an effect on the charge pump current and loop filter capacitance, which is related to charge injection and clock feed-through of the mode transition switch. To minimize these negative effects, half-size dummy switches controlled by complementary signals are added to compensate for the charge injected from the channel. Furthermore, we use wider channel switches to reduce the turn-on time and series resistances. In addition, we employ a voltage buffer to maintain a constant voltage between the two capacitances and to prevent charge sharing during the transition between fast-locking and low-jitter modes.

III. MEASUREMENT RESULT

Two CDR circuits have been fabricated in a 0.18μm CMOS process. Fig. 6 shows a microphotograph of the 1.25Gb/s serial link's receiver in which the proposed CDR circuit including deserializer and word aligner and test logic such as BER detector are incorporated. The die is packaged and the package is on to a 4-layer FR4 board for the purpose of measurement.

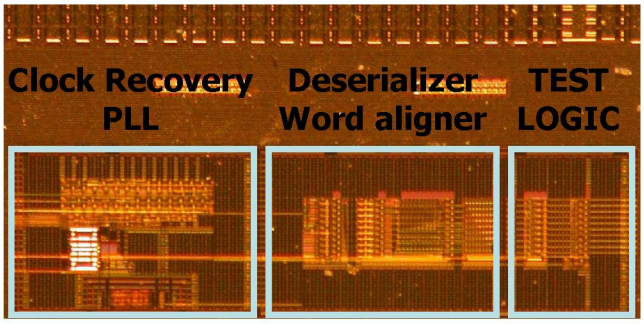

Fig. 6 Microphotograph of the 1.25Gb/s serial link including autonomously reconfigurable architecture

We compared a CDR of two-loop architecture without a *PRELOCK* signal with our CDR with its autonomously reconfigurable structure. The 1.25GHz clock jitter is measured in the fast-locking mode: its rms jitter is 13.46ps and its peak-to-peak jitter is 88ps.

Fig. 7 Comparison of the locking times: (a) CDR without a *PRELCOK* signal (b) CDR with an autonomously re-configurable structure

Fig. 7 compares the locking time of a non-reconfigurable CDR with that of our circuit. Compared to Fig. 7 (a), we includes *PRELOCK* signal that is used for an autonomously reconfigurable charge pump and loop filter. The locking time of an autonomously reconfigurable structure is smaller than that of a non-reconfigurable one.

IV. Conclusions

Clock and data recovery (CDR) is critical function in a high-speed transceiver. We have presented a 1.25Gb/s CDR circuit with a reduced locking time that is achieved by introducing an autonomously reconfigurable charge pump and loop filter into a conventional CDR circuit structure. The charge pump current is tuned to achieve a stable loop at the same time as fast locking. The charge pump current only needs to be doubled to achieve a fast-locking mode which is combined with low power consumption and low jitter, without compromising loop stability. Our experimental prototype was fabricated in 0.18μm standard CMOS technology with a 1.8V supply. Our CDR circuit has an active area of 380 μm ×350 μm.

Acknowledgment

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