58.4: 10-Bit Column Driver with Split-DAC Architecture

Jong-Kwan Woo, Dong-Yong Shin, Won-Jun Choe, Deog-Kyoon Jeong and Suhwan Kim
Inter-University Semiconductor Research Center & EECS, Seoul National University, Seoul, Korea

Abstract
An 8-bit coarse digital-to-analog converter (DAC), which adopts both array and tree-type decoders, is combined with a 2-bit fine interpolation DAC to reduce RC time delay and die area of a column driver for LCD-HDTV applications. Error amplifiers drive a pair of column lines in the output buffer to realize rail-to-rail voltage swing with a high slew rate. The design has been fabricated in 0.3 μm LV-HV CMOS technology.

1. Introduction
LCD-HDTV requires high-performance display with good brightness, color saturation, resolution, together with a digital interface. Customers also want softer and more natural colors, which means that it is necessary to use a 10-bit grayscale column driver, which allows a billion colors to be represented [1].

A typical column driver consists of registers, data latches, digital-to-analog converters (DACs), and output buffers. DACs in conventional designs of column drivers take the form of a resistor-string digital-to-analog converter (DAC) in every channel. It is composed of two global resistor strings for inverting the polarity of the liquid crystal, and each channel has a decoder block which selects one of the voltages generated in the resistor string. This form of DAC has the merits of providing a monotone response, in-built gamma correction, and immunity against process variation. However, the area of this type of DAC doubles for every extra bit of color depth.

Many methods have been proposed to reduce the area of column driver ICs. One method of reducing the area is to use shared DAC and sample-and-hold circuit [2, 3]; but with this design the output voltage of the source driver is not sufficiently uniform because the sample-and-hold circuit is susceptible to process variation, clock feedthrough, and charge injection. Another approach is to use a charge re-distributed DAC [4], which is very efficient in terms of area. However, this solution is not appropriate for true TFT-LCDs. For, example, this form of DAC can achieve 10-bit resolution in video data from the timing controller, but the output of the DAC is linear so that its effective grayscale performance is only equal to that of an 8-bit gamma-corrected column driver. A different approach that is widely used to achieve high resolution is a split-DAC architecture. This architecture combines coarse DAC with a fine DAC [1]. This way, the die area is reduced compared to resistor-string DAC-only architecture. Gamma correction can be achieved by using a resistor-string DAC as the coarse DAC. The fine DAC can be any type that is economic in die area.

TFT-LCD panels for today's LCD-HDTV and multimedia applications have become large and therefore, impose heavy loads on the scan and data lines. For this reason, the output buffers are the bottleneck in achieving good speed, resolution, voltage swing and power dissipation of the column drivers. There are important constraints on the output buffers of an LCD-HDTV column driver: it should occupy a small die area, because the thousands of output buffer amplifiers must be built into a single chip; its static power consumption should be small; it should drive a voltage swing that is almost rail-to-rail, so as to achieve the highest intensity levels; and its settling time should be smaller than the horizontal scanning time.

We propose a split DAC architecture in which an 8-bit resistor-string DAC is combined with a 2-bit interpolation DAC to reduce die area. 8-bit resistor string DAC in our design utilizes both array and tree type decoders to further reduce the die area and the RC time delay. Additionally, our design incorporates a low-power, high-speed output buffer amplifiers with a large input dynamic range and output swing, which are better suitable for the large TFT-LCDs used today.

2. New Column Driver

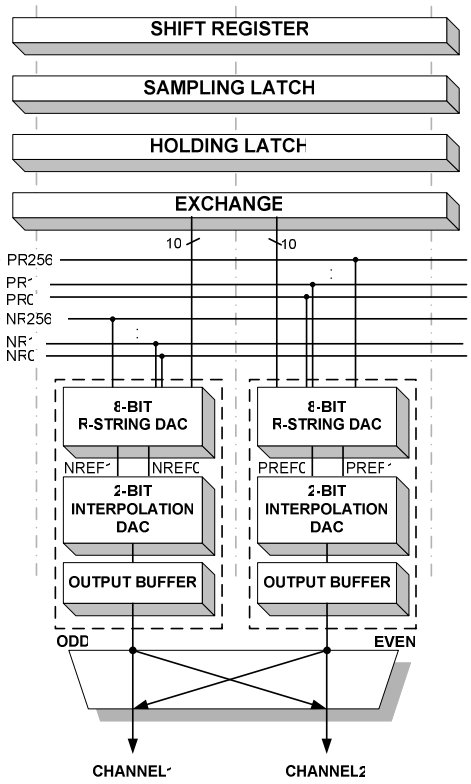

Figure 1. Block diagram of a 10-bit column driver with an 8-bit resistor-string DAC and a 2-bit interpolation DAC

Fig. 1 is the block diagram of the proposed 10-bit column driver, which consists of a shift register, a sampling latch, a holding latch, an exchange block for inversion, the 1st and 2nd DAC stages, and an output buffer. The digital input codes are stored into the shift register serially by the timing controller. Different paths are taken for two different polarity operations. The odd-numbered DACs and buffers form the path for negative polarity operations, and the

 ISSN/008-0966X/08/3902-0892-$1.00

even DACs and buffers form the path for positive polarity operations. When the odd column lines have negative polarity and the even column lines have positive polarity, the input codes and the output buffers are in the normal order. When the polarities of the column lines are exchanged, the order of the input codes and output buffers should also be reversed. But the PMOS input buffers and the odd DACs remain performing the negative polarity operations while the NMOS input buffers and the even DACs perform positive operations. Therefore, we need two paths to drive column lines.

As shown in Fig. 1, each DAC is made up of an 8-bit resistor-string DAC coupled to a 2-bit interpolation DAC. Since both DACs are monotonic, the entire 10-bit DAC is inherently monotonic. The 8-bit resistor-string DAC is made up of a decode block and a large number of resistors which are electrically connected in series to provide many voltage levels. The decoder circuit selects two neighboring voltage levels, which are determined by the 8-bit MSB sub-word. The 2-bit interpolation DAC interpolates the final analog output signal from the two neighboring voltage levels as specified by the 2-bit LSB sub-word.

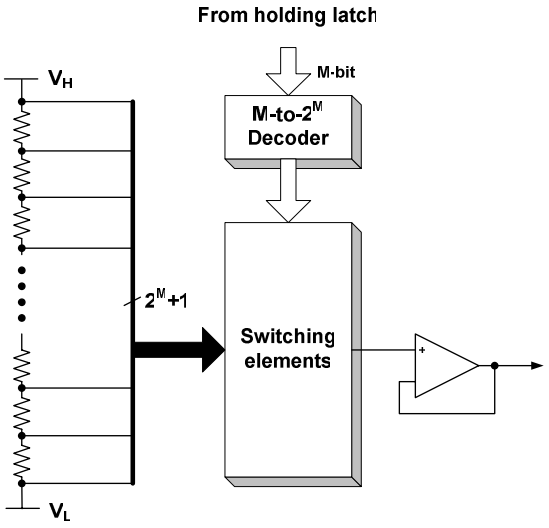

Figure 2. Conventional resistor-string DAC

Fig. 2 shows the conventional resistor-string DAC architecture. It includes a decoder block and resistors of many different values. The resistors are connected in series between high and low reference voltage. The connections between the resistors are also tap points which are selectively switched to an output node as specified by the digital input. The decoder block includes many switching elements, which are MOS transistors. The switching elements select a single line from a large numbers of lines to the output under digital control, which is provided by an *M*-bit input word. The voltage of the tap point switched to the output node becomes an inherently monotonic analog representation of the digital input.

In a conventional 8-bit resistor-string DAC, either an array type or a tree type decoder can be used depending on the need. Generally, the array type decoder necessitates more pass-gate switching elements than the tree-type counterpart, thus has a much longer RC time delay. But the array-type consumes less area than the tree-type decoder because of its arrangement of switching elements and signal lines.

A general resistor string for *M*-bit digital-to-analog conversion requires 2^M resistors, but this is only practical up to around 8 bits. M-bit digital-to-analog conversion also requires $2\times(M-1)\times 2^{M-1}+2$ switching elements with an array-type decoder, and $2\times(2^M-2)+2$ switching elements with a tree-type decoder. For example, for 3-bit digital-to-analog conversion, 9 voltage levels are required, which means 9 tap points, and so 8 resistors are required in the resistor-string DAC. And, in the array-type decoder, 18 switching elements are required to represent two neighboring voltage levels, whereas in the tree-type decoder, 14 switching elements are required.

In both cases, the number of switching elements increases exponentially with the number of bits in the digital input. Consequently, it becomes inevitably large in die area. Therefore, since the number of switching elements and resistors are critical in determining width and height of the chip, it is preferable to keep the length of the digital input to a reasonable level to conserve the die area. In terms of speed, the RC time delay in the switch-array is the dominant time constraint of the resistor-string DACs. This delay could be reduced if there are fewer transistors in the current path or if these transistors are wider. However, reducing the number of switches in the current path requires more logic gates to be presented. If the switch array of the DAC is decreased to reduce the RC time delay, the number of logic gates used in decoding, such as DFF, NAND, NOR, need to be increased. In short, the trade-off between the RC time delay and the number of logic gates is unavoidable.

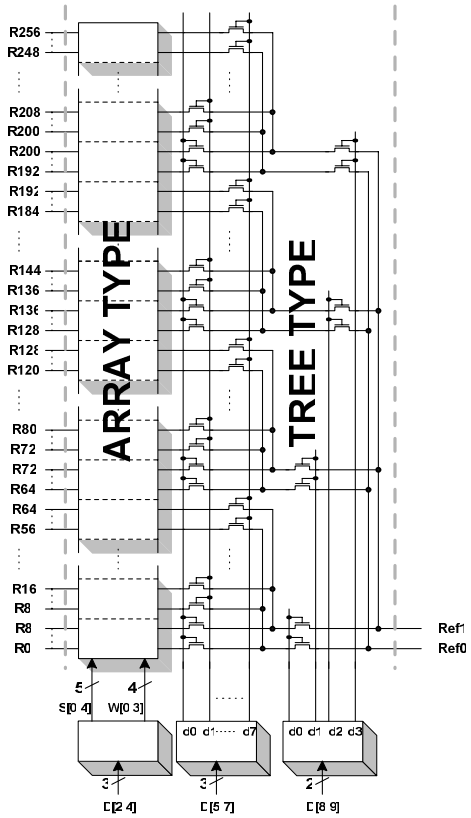

Figure 3. 8-bit resistor-string DAC using a mixed decoder

Therefore, optimizing a resistor-string DAC should aim to reduce the complexity of logic gates, lower the circuit loading and decrease the die area simultaneously. We propose a new optimum resistor-string DAC which uses a combination of three types of decoder in the decoder block to serve this purpose. The proposed scheme is shown in Fig. 3: a 3-bit array-type decoder block, a 3-bit tree-type decoder block, and a 2-bit tree-type decoder block. This architecture uses fewer switching elements and logic gates, thus reduces the circuit loading, the RC time delay and the die area compared with a conventional one.

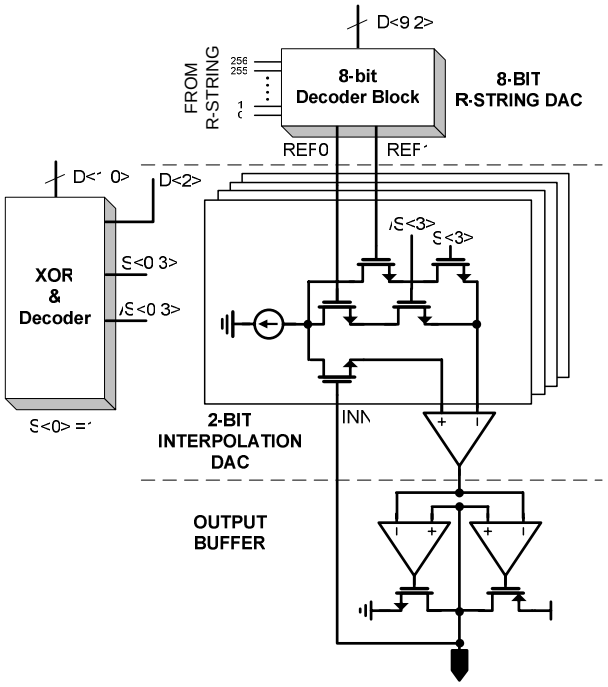

Figure 4. Details of the 2-bit interpolation DAC and the output buffer

The 2-bit interpolation DAC in Fig. 4 performs fine interpolation between REF0 and REF1 which are two outputs from the previous 8-bit resistor-string DAC controlled by D<9:2>. The interpolation DAC consists of an "XOR & Decoder" block, four differential trans-conductance stages and a differential current summing stage. In the "XOR & Decoder" block, each bit of D<1:0> is XORed with D<2> and the resulting code is decoded into a thermometer code S<1:3> which increases its value from S<3>. At the same time, S<0> is equal to D<2>. The value of S<0:3> represents the weight of REF1 for interpolation. When D<2> is low, REF0 is closer than REF1 to the output voltage for the all-zero input of D<9:0> and the weight of REF1 increases from 0 as the value of D<1:0> increases. On the other hand, when D<2> is high, REF1 is closer to the all-zero output voltage, the weight of REF1 decreases from 4 and , in other words, the weight of REF0 increases from 0. In this way, we can monotonically interpolate a selected interval between REF0 and REF1 without missing any output levels. Each bit of the S<0:3> and its inversion signal have their own differential stage which includes a pair of switching transistors controlled by them. The differential stage has three input transistors of the same size which have a common source terminal. A tail current source is connected to the common source. Each differential trans-conductance stage has its own tail current source to increase linearity. One of the input transistors has its gate coupled to REF1 and its drain connected to the negative input terminal of the differential current summing stage via a switching transistor controlled by one bit of S<0:3>. Another input transistor has its gate coupled to REF0 and its drain connected to the negative input terminal for the differential current summing stage via the other switching transistor. The last input transistor has its gate coupled to the output of the interpolation DAC which, in this case, is buffered by an class-AB output buffer composed of two error amplifiers and a pair of pull-up and pull-down transistors as shown in Fig. 4.

The driving capability of an output buffer can be improved by increasing the sizes of its output transistors. However, this will increase the quiescent current and the total power consumption. In our design, error amplifiers are added to improve the driving capability without increasing the quiescent current. By using error amplifiers in the negative feedback between the input and the output of the buffer, it becomes capable of accurately controlling the quiescent current through the output transistors. This method can achieve highly power-efficient, less-distorted, high-swing common-source output stage. These error amplifiers need to have a relatively low gain to guarantee stable operation of the loop: otherwise, a typical input offset voltage of tens of mV would cause a huge change in the quiescent output current [5, 6].

3. Measurement Results

The proposed column driver has been fabricated using 0.3 μm LV-HV CMOS technology. The performance of the proposed concepts and circuits were verified by HSPICE simulation and measurement. Fig. 5 shows post-layout simulated waveforms for the dot inversion 10-bit column driver with 10 kΩ , 300 pF RC load. The input voltage range was 0.2–11.8 V. At the input node of the RC load, the time for the output to settle within 0.2% (0.5 LSB) of the final voltage was 1.8 and 2 μs for the rising and falling edges respectively.

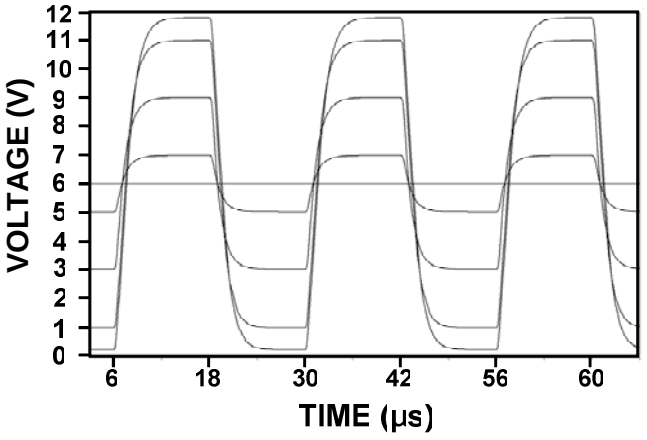

Figure 5. Post-layout simulation results for the proposed 10-bit column driver at the end node of the RC load

Fig. 6 shows the measured gamma-corrected transfer curve of the DAC with its output buffer. The voltages below 6V correspond to

negative polarity and those above 6V to positive polarity. The differences between the calculated and the measured output voltage are within 4mV. The deviations are caused by the mismatch between the resistors in the DAC and the offset voltage of the amplifiers. Our column driver for positive polarity consumes a quiescent current of 5.2 μA, and the driver for negative polarity consumes 5.4 μA.

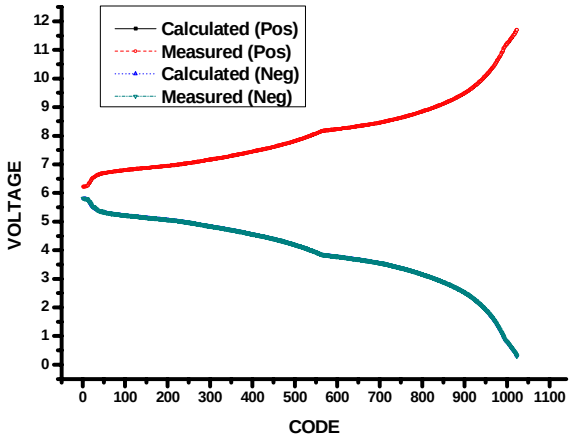

Figure 6. Measured transfer curve for the proposed 10-bit column driver

4. Conclusions

We have presented a column driver architecture and high-speed rail-to-rail buffer amplifier which are suitable for driving the large column line capacitance in LCD-HDTV. Prototype column drivers were implemented in 0.3 μm LV-HV CMOS technology.

In our design, 8-bit resistor-string DAC and 2-bit LSB interpolation DAC are used due to fewer switching elements and smaller die area than conventional 10-bit DAC. Further reduction in die area is achieved by mixing array and tree-type decoders in the 8-bit resistor-string DAC. Also, better driving capability is obtained by using error amplifiers which also have elaborate quiescent current control.

The combination of reduced circuit loading and die area with increased slew rate makes our column driver suitable for large flat-panel displays.

5. Acknowledgement

This work was supported by “System IC 2010” project of Ministry of Commerce, Industry and Energy. This work was also supported in part by Synerchip.

6. References

[1] J.-H. Kim *et al.*, "1-billion-color TFT LCD TV with full HD format," *IEEE Transactions on Consumer Electronics*, vol. 51, no. 4, pp. 1042-1050, Nov. 2005.

[2] E. G. Kim *et al.*, "A compact LCD driver and timing controller system," *SID Symposium Digest Tech Papers*, vol. 31, pp. 46-49, May. 2000.

[3] C. Zajac *et al.*, "System design considerations for TFT-LCD panels using sample and hold based column drivers," *SID Symposium Digest Tech Papers*, vol. 34, pp. 333-336, May 2003.

[4] M. Bell, "An LCD column driver using a switch capacitor DAC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2756-2765, Dec. 2005.

[5] B. K. Ahuja *et al.*, "A programmable CMOS dual channel interface processor for telecommunications applications," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, pp. 892-899, Dec. 1984.

[6] J. Ki *et al.*, "Class-AB large-swing CMOS buffer amplifier with controlled bias current," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1350-1353, Dec. 1993.