Power Efficient SAR ADC Adaptive to Input Activity for ECG Monitoring Applications

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***Abstract*—The proposed 1.8-V 10-bit 1-kS/s successive approximation register (SAR) analog-to-digital converter (ADC) for electrocardiographic (ECG) monitoring applications has two operation modes suitable for the dichotomous activity of ECG signals: full and reduced switching modes. MSBs tracking and LSBs extrapolation run in full and reduced switching mode, respectively, for smooth mode changes adaptive to the input activity. A prototype chip was fabricated in 0.18-µm CMOS technology. The suitability of the proposed adaptive switching was proved by the measurements that the total power consumption was reduced by 15.3% compared to the full switching case.**

Keywords—SAR; ECG; input activity; adaptive switching

I. INTRODUCTION

Electrocardiography (ECG) is the process of measuring and recording the electrical activity of the heart, which is an important source for diagnosis of heart diseases. For a single period, typical ECG signals have a high degree of variation around just a few specifically designated portions, i.e. P wave, QRS complex, and T wave; otherwise, they have quite a low degree of variation. From this observation, ECG signals can be said to have dichotomous activity. It is though known that the informative content is within a frequency band up to 100 Hz [1], [2]. In practice, ECG signals are recommended to be lowpass filtered with a corner frequency of 150 Hz and sampled with a rate of at least 500 samples per second (S/s), in order to obtain small measurement error and unambiguous results [1], [2]. Low power consumption is a critical factor in the circuit design for ECG monitoring applications [3]–[5]. For the power hungry ADC, power efficient successive approximation register (SAR) is a popular choice of topology. In order to further cut down power consumption, the characteristics of the ECG are often exploited to reduce the number of bit-cycles of the SAR ADC while retaining the resolution [3]–[5]. [3] starts with an initial guess equal to the previous sample, and corrects it from the least significant bit (LSB) upwards. However it is less efficient than the conventional SAR ADC for a highly active input, losing its advantage. [4] prevents unnecessary switching of most significant bits (MSBs) if the previous and current samples differ only in a few LSBs but at the expense of an additional clock cycle and unary weighted MSB capacitors in the DAC. [5] tracks the samples and looks for the rightmost 01 or 10 pattern and just locks all bits left to them. But it could suffer from frequent errors. It does not have means to predict error occurrence either.

We propose a 10-bit SAR ADC with adaptive switching, which selects the suitable operation mode out of two adaptively to the input activity. By default, it digitizes all bits as usual (full switching mode), but when the input activity is quite low, it digitizes just 5 LSBs (reduced switching mode). Each operation mode is accompanied with MSBs tracking and LSBs extrapolation, respectively. These additional functions examine the input activity and determine the next operation mode, as shown in Fig. 1. They provide more reliable bases to determine the input activity hence fewer error occurrences than those of the adaptive locking [5]. They run in parallel with the main SAR operation, so that additional clock cycles are not required, unlike [4]. Moreover, it affords a fully differential capacitive DAC topology by partial sampling, which is unavailable in [4], [5].

II. PRINCIPLES OF THE PROPOSED OPERATIONS

A. MSBs Tracking in Full Switching Mode

In full switching mode, the SAR ADC operates in an ordinary manner, except that the 5-bit MSB code is tracked and equality of three consecutive MSB codes is checked. If the three consecutive MSB codes are equal, the input activity is assumed to have subsided enough that the MSB code will not change, and the ADC enters reduced switching mode from the next period. Fig. 2 shows an example of this procedure. In this example, the MSB code first becomes 10110 at $(N-3)T_S$ and the code is kept for three successive periods, until $(N-1)T_S$. Here T_S denotes the sampling period. The ADC enters reduced switching mode at NT_S, and the MSB code of 10110 is used as the preset MSB code throughout reduced switching mode.

B. Sampling and Conversion in Reduced Switching Mode

In reduced switching mode, only the 5-bit LSB portion of the input is sampled. Figs. 3(a) and 3(b) illustrate how this partial sampling and its conversion are achieved, respectively, on one side of the differential capacitive DAC. Charge conservation of the capacitors enables the partial sampling [6]. The input is applied on the top plates of the capacitors while the voltages on the bottom plates of the 5 MSB capacitors are

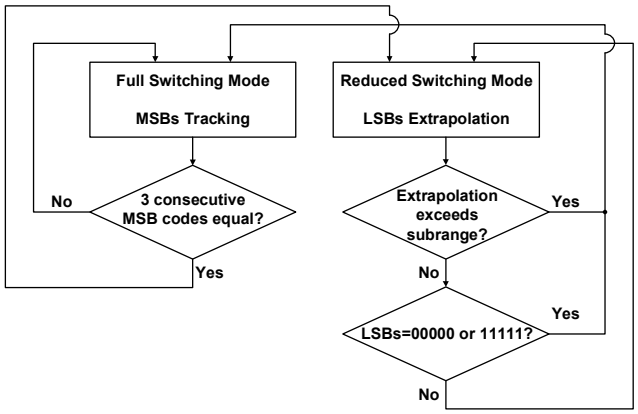


Fig. 1. Flowchart of the proposed operations overall.

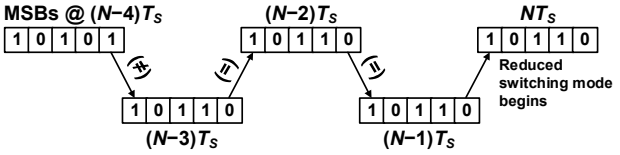


Fig. 2. Operation of the tracking of the MSBs.

preset to either the reference voltage V_{ref} or 0 V according to the preset MSB code. The total charge stored in the capacitors corresponds to the input (top plates) minus the 5-bit MSB portion of the input (bottom plates), yielding only the 5-bit LSB portion to be sampled. In the conversion phase, the bottom plates of the MSBs are connected to V_{cm} and the digitization is done by switching just 5 LSB capacitors. The ADC is idle for the last 5 cycles of the period, which further helps reduce power consumption.

C. LSBs Extrapolation in Reduced Switching Mode

Linear extrapolation of the LSB code is carried out to determine whether the MSB code will change in the next period. If the extrapolation exceeds the boundaries of the 5-bit code, the ADC enters full switching mode. An example of this procedure is demonstrated in Fig. 4. There is however a possibility that it fails to predict a change of the MSB code. It could happen if the input changes more than predicted. In this case, the LSB code of the output will be stuck to either 00000 or 11111, unable to resolve the excessive difference from the reference. If this pattern in the LSB code is detected, the ADC enters full switching mode from the next period, thus avoiding further error occurrences.

III. Circuit Implementation

Fig. 5 shows the block diagram of the proposed SAR ADC. The capacitive DAC is designed to have a fully differential tri-level split-array topology using top-plate sampling. The full-switching mode logic is made up by the ordinary SAR logic and the MSBs tracking logic. The reduced switching mode logic includes the LSBs extrapolation logic.

The control signals are denoted by C and D in Fig. 5. The C signals are associated with V_{cm}, and the D signals are with V_{ref} or 0. If a C signal is high, the bottom plate of the corresponding

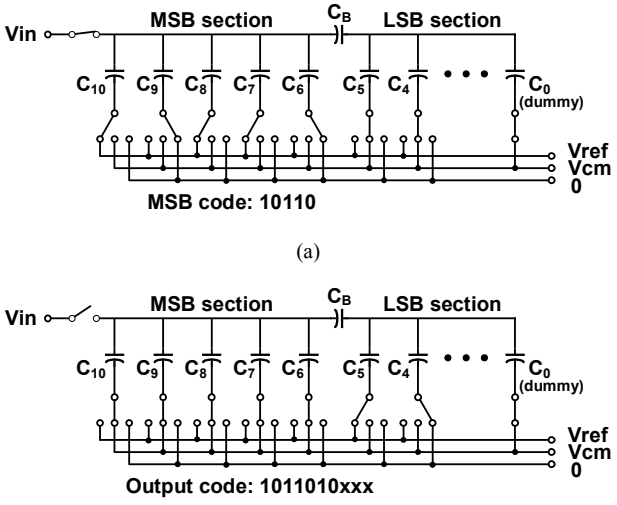


Fig. 3. Operations in reduced switching mode: (a) in the sampling phase, and (b) in the conversion phase.

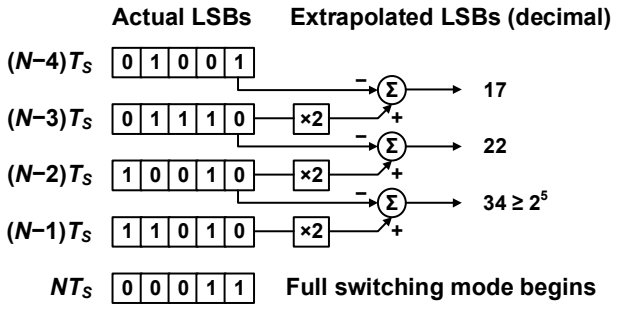


Fig. 4. Operation of the extrapolation of the LSBs in reduced switching mode.

capacitor is connected to V_{cm}. If a D signal is high, the bottom plate of the corresponding capacitor is connected to V_{ref} or 0, with respect to the comparator output. For a particular capacitor, both C and D cannot be turned on at the same time.

Both modes generate their own set of control signals and the proper set is selected by signal "opmode." Most of the differences in the control signals are in the C and D signals for the MSB section, i.e. C[9:5] and D[9:5], as can be inferred from the operation principles explained in the previous section.

The signal opmode is the output of an SR flip flop. If it is logic 1, it indicates full switching mode, and logic 0 is associated with reduced switching mode. The set and reset inputs to the flip flop are generated by the LSBs extrapolation and MSBs tracking logics, respectively.

A. MSBs Tracking Logic

Fig. 6 depicts the MSBs tracking logic. It makes use of the existing output register. By taking the input and output of the register, the equality of the current and previous MSB codes can be checked. An additional flip flop holds the equality information of the previous pair. Using these above, the equality of three consecutive MSB codes is examined in every

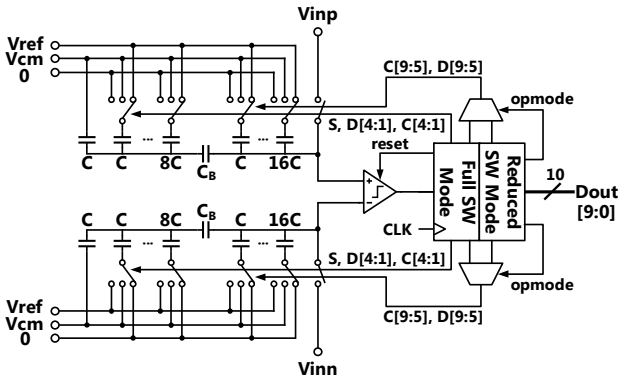


Fig. 5. Block diagram of the proposed adaptive switching SAR ADC.

period. If three consecutive MSB codes are equal, the opmode reset signal, R, becomes 1 and reduced switching mode begins from the next period. The MSB portion of the output register is frozen to hold the last code for the use as the preset MSB code in the upcoming reduced switching mode operations.

Unlike the most logic timed at signal S, which indicates the sampling phase, the flip flop is timed at signal SE, which has a slightly earlier phase than that of S. The decision of the next mode is made during the interval between the rising edges of SE and S, and mode change is carried out without additional cycles.

B. LSBs Extrapolation Logic

The linear extrapolation of the LSB code is realized by left shifting and a 6-bit subtractor as exhibited in Fig. 7. If the MSB of the output of this operation is 1, the next LSB code is predicted to go beyond the reach limited by the preset MSB code. In conjunction with the above case, the current LSB code being 00000 or 11111 makes the opmode set signal, F, logic 1 and full switching mode begins from the next period.

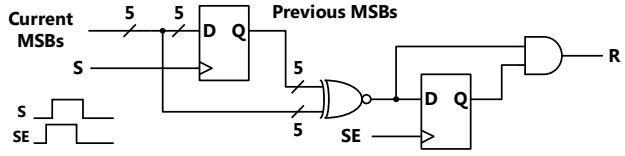


Fig. 6. Block diagram of the MSBs tracking logic.

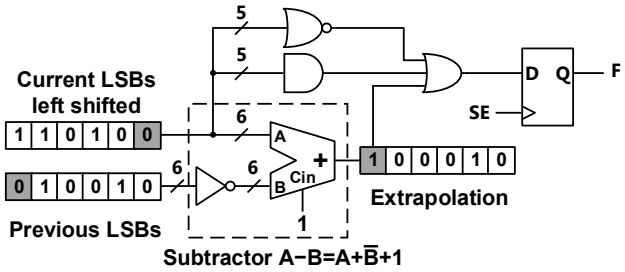


Fig. 7. Block diagram of the LSBs extrapolation logic.

C. LSBs Extrapolation Logic

The linear extrapolation of the LSB code is realized by left shifting and a 6-bit subtractor as exhibited in Fig. 7. If the MSB of the output of this operation is 1, the next LSB code is predicted to go beyond the reach limited by the preset MSB code. In conjunction with the above case, the current LSB code being 00000 or 11111 makes the opmode set signal, F, logic 1 and full switching mode begins from the next period.

D. Control Signals

Fig 8 shows the timing diagram of the control signals for both operation modes. The sampling phase of a period takes first two clock cycles and the remaining 10 cycles are for the conversion phase. In reduced switching mode, the conversion finishes 5 cycles earlier. The ADC is idle for the remaining time.

IV. Prototype and Experimental Results

The prototype of the proposed SAR ADC was fabricated in a 0.18-μm CMOS process. The ADC was designed to operate at a 1.8-V supply voltage and have a sampling rate of 1kS/s which is suitable for ECG monitoring applications. The active area is 0.096 mm^2. The layout and die photograph are exhibited in Fig. 9. For measurement, a differential ECG type signal was generated using Keysight 81160A. Its waveform is shown in Fig. 10(a), and the measured digital output code and opmode are displayed in Fig. 10(b). Figs. 10(a) and 10(b) demonstrate that mode change is conducted so smoothly that the reconstructed ECG waveform from the digital output maintains good quality.

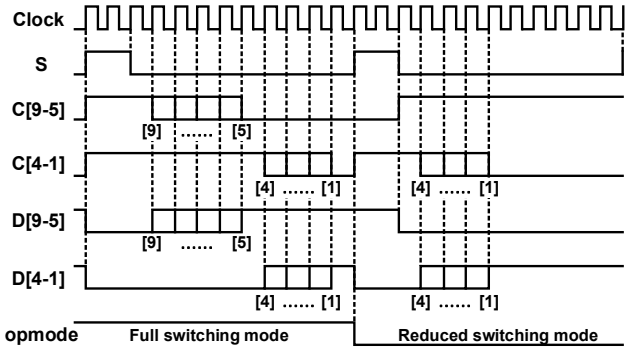


Fig. 8. Timing diagram of the control signals to the capacitive DAC.

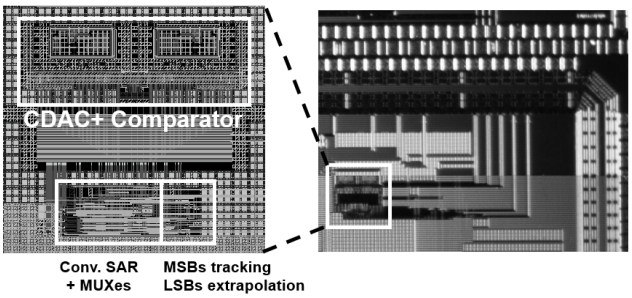
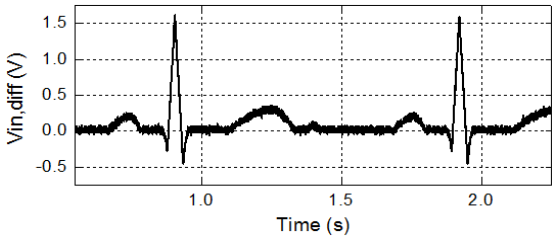
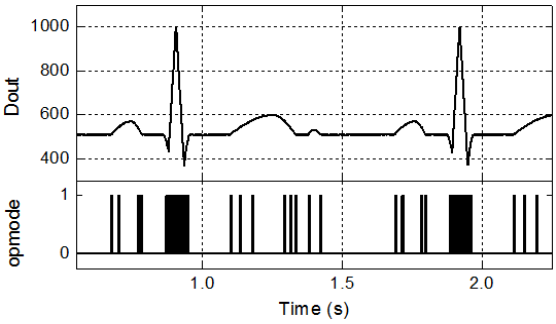


Fig. 9. Die photograph and layout of the proposed ADC.

Table I presents the measurements. The total power consumption is the sum of the ADC power per se and the reference power. The proposed adaptive switching consumed 91.02 nW. When the operation mode was fixed to full switching, it was 107.51 nW. Thus the adaptive switching reduced the power consumption by 15.3%. The SNDR and the SFDR were measured while the ADC was forced into full switching mode and a differential sinusoidal input with an amplitude of 3.15V peak-to-peak and a frequency of 93.153 Hz was applied to the ADC. The measured SNDR and SFDR are 56.25 dB and 64.60 dB, respectively. The power spectral density is presented in Fig. 11.



(a)



(b)

Fig. 10. Measured waveforms of (a) the differential ECG type input and (b) the reconstructed ouput code and opmode for the ECG type input.

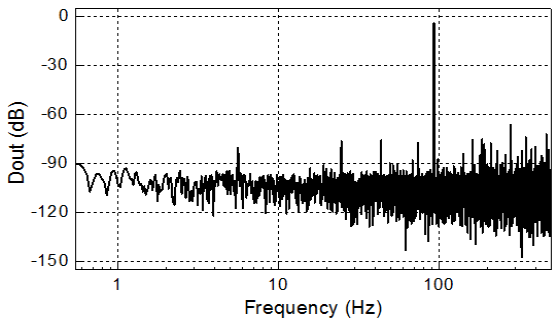


Fig. 11. Power spectral density of the measured ADC output for the differential sinusoidal input.

TABLE I. SPECIFICATIONS OF THE PROPOSED ADC

Specification	**Value**
Technology	0.18μm CMOS
Resolution	10 bits
Supply Voltage	1.8 V
Sampling Rate	1.0 kS/s
Diff. Input Range	3.15 V_{P-P}
Power Consumption	91.02 nW (adaptive) 107.51 nW (full switching)
SNDR	56.25 dB
SFDR	64.60 dB
Active Area	0.096 mm^2

V. CONCLUSION

The proposed SAR ADC with the input activity adaptive switching method utilizes the dichotomous nature of the ECG signal activity for power efficient operations. As demonstrated in the experiment with an ECG type input, mode change was successful that the ADC resolves active QRS complexes and P and T waves in full switching mode, and the rest little active parts in reduced switching mode. The adaptive switching helps reduce power consumption while the resolution is retained. The measurements showed that the adaptive switching achieved a reduction in power consumption by 15.3% compared to the case fixed to full switching all the time.

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