Comparison of phase rotator performance and proposal of design method

Jihwan Park*, Gi-Moon Hong, Suhwan Kim†
Department of Electric Engineering and Computer Sciences
Seoul National University, Seoul 157-742, Republic of Korea
Tel: +82-2-882-9571, Fax: +81-2-882-9571
E-mail: *Jihwan.Park@amic.snu.ac.kr, †suhwan@snu.ac.kr

***Abstract*— In this paper, we consider the phase rotator(PR) which generates sampling clock signal used in clock and data recovery(CDR) circuits. There are three main types of PRs: the phase interpolator(PI), the phase rotator using weighted charge pump, and the injection locked oscillator(ILO)). We examine the implementation and operation of these circuits and compare the pros and cons. Then, we propose a new type of PR with the loop filter(LF) designed for being capable of phase rotation**

I. INTRODUCTION

As technology progresses deeper into submicron CMOS, chip speed and the capacity of memory rises. Therefore, there is a need for I/O interface which is optimized for high-speed chip-to-chip communication. However, the data rate in a serial link receiver is limited by the speed of technology process, so it is essential to solve this problem. As a solution, the multi-channel serial link can be utilized. In this system, the Tx transmits multi-bit data in a cycle, and the Rx recovers the data by sampling with multiphase clock. This makes the chip operate at a lower speed than the data rate. In this paper, we analyze the PR which makes the function mentioned above possible. The PR circuit includes phase shifting and phase rotation function as well as multiphase generation.

II. PHASE ROTATOR

A. Phase Interpolator

The phase interpolator(PI) receives two different phase signals as inputs and generates a new signal with a phase between the phases of the input signals. PI can be designed by using simple inverter based circuits or by giving different weights to the two input signals.

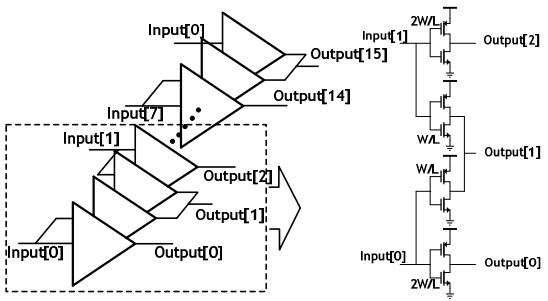

Fig. 1. Architecture of inverter based PI

The inverter based PI is shown in Fig 1. In this circuit, the output nodes of the inverters are connected to each other. Therefore the phase of the superposition output signal is placed at the equally divided point between the two input signal phases. This circuit can perform phase shifting and phase rotation. However it needs as many inverters as the number of target phases, so there is a power consumption issue. In addition, to generate multiphase inputs as the inputs of the PI, it is necessary to design an additional DLL or PLL.

The PI which utilizes the current source weighting method is shown in Fig 2. This circuit takes two differential inputs with different phases. By controlling control codes to change the size of current sources, the differential output signal has a phase which is located at the internal division point. The resolution of this PI is determined by two components: the phase difference between two inputs and the number of current sources.[1]

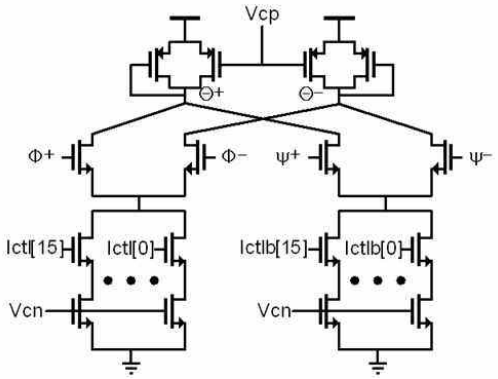

Fig. 2. Architecture of current source based PI

This PI generates a new phase output easily by controlling digital codes. However, this circuit also needs as many PIs as the number of phases that we want which can be a problem for multiphase clock generation. Moreover the mismatch of current sources can degenerate linearity.

B. Phase Rotator using weighted charge pump

Fig. 3 shows the overall architecture of the PR using weighted charge pumps. This circuit consists of two phase frequency detector(PFD)s, weighted charge pump(WCP)s and a VCO. The WCPs multiply the outputs of the two PFDs by

different weights. This PR generates multiphase signals by the VCO, so phase rotation can be achieved with only one PR. This leads to an advantage in terms of area and power dissipation. However it requires a main PLL for generation of the reference clock, and this degenerates power and area efficiency.[2]

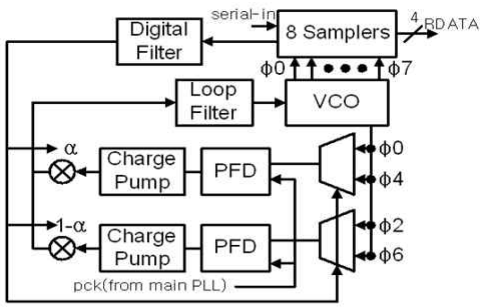

Fig. 3. The overall scheme of PR using WCP

C. *Injection Locked Oscillator*

The injection locked oscillator(ILO) has been gaining attention recently, because of its better performance than other PRs. ILOs are classified into two types: ILO with LC oscillator and injection locked ring oscillator(ILRO). The LC oscillator type ILO has an advantage in noise and jitter performance. However, there is an LC tank in the oscillator, so it has a large circuit area. Furthermore, to carry out phase rotation and multiphase generation, additional circuitry is necessary. [3]

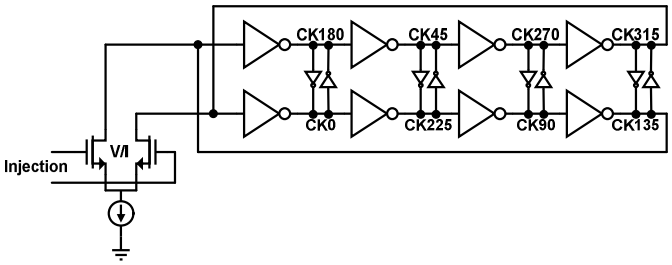

Fig. 4. Injection locked ring oscillator architecture

As shown in Fig 4, the ILRO is introduced as an alternative to the LC oscillator type ILO. This circuit is designed by connecting the injecting signal node to the free running ring type oscillator. The free running signal in the oscillator and the injection signal are overlapped, and frequency and phase transition can be achieved. The ILRO does not need a reference clock or other additional blocks. However it is hard to design this circuit because of its high degree of accuracy, narrow tuning range, and linearity issues at the injection node.[4]

III. CONCLUSION

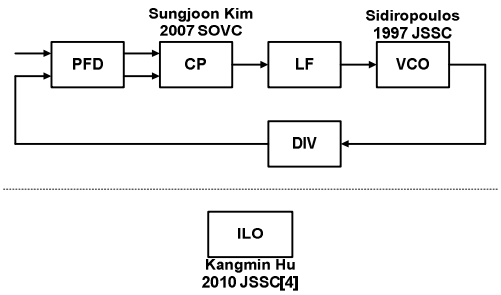

Fig. 5. Methods of phase shifting

Performance comparison of the mentioned PRs is shown in Table 1. Several PRs are proposed, and each PR has pros and cons following implementation. The notable point is that most PRs use a PLL architecture. However they alter specific parts to suit their respective operation principles. Fig. 5 indicates this point in a PLL block diagram. In this paper, thus, we propose the possibility of designing a PR by changing the LF part. The biggest concern is to design the PR for a source synchronous system without losing design simplicity.

To design a PR for a source synchronous system, high loop bandwidth is needed. Thus, if we use dual loop, we can solve this issue. By injecting the two outputs of the multiphase signals into the dual loop PFD and changing weights by resistor ratio in the LF, we propose a new type of PR. This method would make the circuit simple and enhance many performances.

TABLE I
PR PERFORMANCE SUMMARY

	PI	PR using WCP	ILRO
Process	90nm CMOS	130nm CMOS	90nm CMOS
Data rate	2.5GHz	1.25GHz	2.5GHz
Resolution	2.94ps	13.3ps	2.0 - 4.0ps
Power Diss.	20mW	3.6mW	1.3mW(2GHz)

REFERENCES

[1] S. Sidiropoulos and M. Horowits, "A semi-digital dual delay-locked loop," IEEE J. Solid-State Circuits, vol. 32, no. 11, pp. 1683-1692, Nov. 1997.

[2] Sungjoon Kim, et al., "A dual PFD phase rotating multi-phase PLL for 5Gbps PCI Express Gen2 multi-lane serial link receiver in 0.13um CMOS," in IEEE symp. VLSI Circuit Dig. Tech. papers, June. 2007, pp. 234-235.

[3] B. Razavi, "A study of injection pulling and locking in oscillators," inProc. IEEE Custom Integrated Circuits Conf., San Jose, CA, Sep. 2003, pp. 305-312.

[4] Kangmin Hu, et. al., "A 0.6mW/Gbps, 6.4-8.0Gbps Serial Link Receiver Using Local Injection-Locked Ring Oscillators in 90nm CMOS," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 899-908, Apr. 2010.