

# Level-shifting Low-pass Filter Using DC-decoupled Capacitance Multiplication for Integrated Input Interface of Automotive MCUs

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**Abstract**—A level-shifting low-pass filter is presented for integrated input interface of automotive microcontrollers. The level-shifting low-pass filter captures battery-level inputs and attenuates high-frequency noise. By using DC-decoupled capacitance multiplication, our level-shifting low-pass filter withstands large voltage spikes and improves a cut-off frequency from 3 MHz to 10.5 kHz regardless of the sensor output DCs, thus eliminating the expensive external components. The level-shifting low-pass filter occupies 0.016 mm<sup>2</sup> per channel, which is only 0.45% of the size of the input interface. The input interface achieves 60.7 dB signal-to-noise-plus-distortion ratio. A prototype is fabricated in 0.18  $\mu\text{m}$  BCDMOS technology.

**Index Terms**—Level shifter, low-pass filter, automotive, microcontroller, input interface, analog front-end

## I. INTRODUCTION

The amount of electronics in modern motor vehicles has increased rapidly since the introduction of electronic control units (ECUs) [1]. They have enabled integration which has reduced costs and increased reliability, but

many challenges still remain. A typical ECU contains both digital and analog function modules including microcontrollers (MCUs), controller area network (CAN) transceivers, and input interfaces. An input interface which receives automotive sensor signals with a wide range of DC-levels consists of level-shifter, low-pass filter and an analog-front-end (AFE). The level-shifter protects the internal circuit by reducing the voltage of battery-level sensor signals, and the low-pass filter reduces the high-frequency noise from the sensor. These functions are generally merged into a single circuit with shared passive components, as shown in Fig. 1(a). Dealing with large voltage spikes and achieving a low cut-off frequency require a large capacitor, and therefore level-shifters and low-pass filters are generally implemented using external components. However, these increase the cost and reduce the robustness of the module. Sensor integrated circuit products for automotive applications are already removing external components such as capacitors for external filters [2], but previous automotive MCUs still require external components. Wang et al. [3] and Specks et al. [4] presented the MCUs with analog function modules on the same die. However, external passive components are required to protect the MCUs from battery-level voltages arriving through sensors. In addition, expensive high-quality passive elements are used for linearity. They do not provide the necessary functions such as gain control and filtering which are essential for signal processing of these signals. We present an automotive MCU constructed with 0.18  $\mu\text{m}$  BCDMOS (bipolar, CMOS, and DMOS) technology with an integrated input interface that can

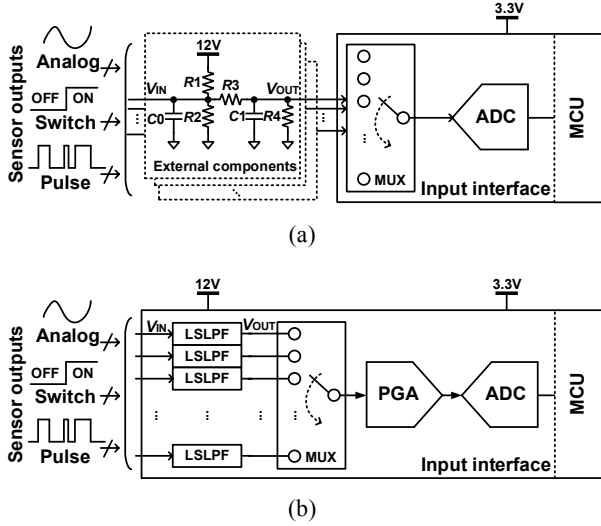
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Manuscript received Jul. 7, 2020; reviewed Aug. 25, 2020; accepted Aug. 26, 2020

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**Fig. 1.** Input interface for acquiring sensor outputs (a) conventional input interface with external components on a PCB, (b) our on-chip input interface with integrated level-shifting low-pass filter.

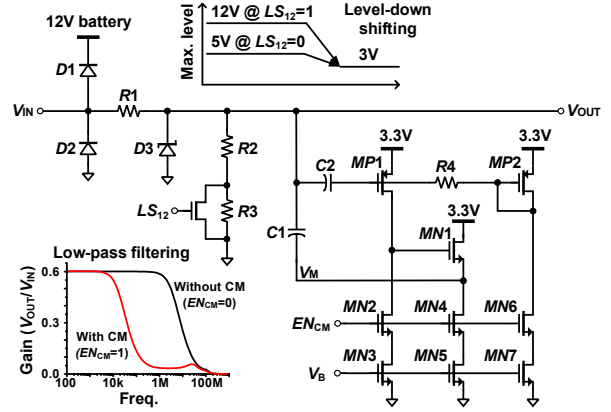
handle analog and pulse signals as well as switches. It supports sensors with a wide range of output voltages while requiring fewer external components than previous circuits.

## II. CIRCUIT IMPLEMENTATIONS

### 1. Input Interface

A typical input interface for automotive MCUs [5] is shown in Fig. 1(a). There is an external capacitor  $C_0$  to cope with surges in voltage; pull-up and pull-down resistors  $R_1$  and  $R_2$ ; a resistor  $R_3$  to limit the current reaching the MCU; a capacitor  $C_1$  for passive low-pass filtering of the high-frequency noise from the sensor and wiring harness; and resistors  $R_3$  and  $R_4$  form a voltage down-shifter. Fig. 1(b) is our 32-channel input interface which includes a level-shifting low-pass filter (LSLPF) and an AFE. The LSLPF reduces the amplitude of sensor signals from the battery-level voltage of 12 V to a voltage below 3.3 V and also reduces the high-frequency noise from the sensor and wiring harness.

The AFE digitizes the output of the sensor. In order to change the characteristics of each channel of the input interface to suit a particular type of sensor without requiring or trimming external components, our AFE includes various analog building-blocks. After the sensor output has been level-shifted and low-pass filtered by the



**Fig. 2.** The level-shifting low-pass filter (LSLPF).

LSLPF, a channel-selector with an analog multiplexer selects each channel sequentially. A PGA amplifies the output of the analog multiplexer to match the input range of a 12-bit 1 MS/s successive-approximation-register (SAR) analog-to-digital converter (ADC). In order to make full use of the full scale of the ADC, which ranges from 0.15 V to 3.15 V, the gain of the PGA can be adjusted in 5 steps of 2, 3, 4, 6, and 12 V/V.

### 2. Level-shifting Low-pass Filter

In our input interface, the function of the passive components in a conventional interface is performed by an on-chip LSLPF for each channel, as shown in Fig. 1(b). The circuit of an LSLPF is shown in Fig. 2. The diodes  $D_1$  and  $D_2$  included in the I/O pads protect the MCU from battery over-voltage. The resistors  $R_1$  and  $R_2$  form a level-shifter to reduce the peak voltage coming from a sensor from 12 V to 3 V required by the rest of the circuit.  $R_1$  also act as a current limiter and  $R_2$  acts as a pull-down resistor.  $R_3$  is provided when the sensor output voltage is 5 V and is brought into play when  $LS_{12}$  is low. The Zener diode  $D_3$  is an additional safety device. When there is a simultaneous spike in  $V_{IN}$  and the battery voltage,  $D_1$  is ineffective. The presence of  $D_3$  ensures that  $V_{OUT}$  never rises above its breakdown voltage of 5 V.

The input interface requires a low-pass filter and the low-frequency range of the output of a typical sensor requires a large capacitor. To implement this capacitor in silicon using a metal-insulator-metal (MIM) capacitor that only provides a few fF/ $\mu\text{m}^2$ , we use a DC-decoupled

capacitance-multiplication (CM) technique that utilizes the Miller effect [6, 7]. Our circuit consists of a single-stage amplifier made up of the transistors  $MP1$  and  $MN3$ , a DC-decoupling capacitor  $C2$ , and a replica-bias generator comprising  $R4$ ,  $MP2$ , and  $MN7$ . The charge on  $C1$  is multiplied by the gain of the single-stage amplifier.  $C2$  prevents DC from the sensors from reaching the amplifier while accommodating for the various output DCs of the sensor. The gate voltage of  $MP1$  decoupled from the sensor output DCs is generated by the replica-bias generator. The resistor  $R4$  allows the gate node of  $MP1$  to offer high impedance to both the AC component of  $V_{IN}$  and the DC component generated by  $MP2$  and  $MN7$ .

The size of the transistor in the replica-bias generator is the same as that in the single-stage amplifier and so this scheme always operates in the saturation region regardless of the DC component of  $V_{OUT}$ . The transistors  $MN1$  and  $MN5$  form a source follower to increase the bandwidth of the single-stage amplifier, improving the rejection of out-of-band frequencies. The CM can be activated for each channel independently by the input signal  $EN_{CM}$ . When  $LS_{12}$  and  $EN_{CM}$  are both asserted and the gain of the source follower is approximately 1, the cut-off frequency  $f_{3dB}$  can be derived as follows:

$$\frac{V_M}{V_{OUT}} = -gm_{MP1}(ro_{MP1} // ro_{MN3}), \quad (1)$$

$$\begin{aligned} C1_{Miller} &= C1 \left( 1 - \frac{V_M}{V_{OUT}} \right) \\ &= C1(1 + gm_{MP1}(ro_{MP1} // ro_{MN3})), \end{aligned} \quad (2)$$

$$f_{3dB} = \frac{1}{2\pi(R1 // R2)C1(1 + gm_{MP1}(ro_{MP1} // ro_{MN3}))}, \quad (3)$$

where ‘//’ indicates that impedances are connected in parallel.  $C1_{Miller}$  represents the effective capacitance caused by Miller effect. The variable  $gm_{MP1}$  is the transconductance of  $MP1$ , and  $ro_{MP1}$  and  $ro_{MN3}$  are the output impedances of  $MP1$  and  $MN3$ . The gain of the amplifier is  $gm_{MP1}(ro_{MP1} // ro_{MN3})$ .

In our design, the values of  $R1$ ,  $R2$ ,  $R3$ , and  $R4$  are 79.5 k $\Omega$ , 26.5 k $\Omega$ , 92.7 k $\Omega$ , and 35 M $\Omega$ , respectively.

$C1$  and  $C2$  are both 2.4 pF. The gain of the single-stage amplifier is 50 dB.  $V_B$  is generated by a current mirror which copies the current from an internal reference generator. The drain current through  $MN3$ ,  $MN5$ , and  $MN7$  is 2  $\mu$ A. Therefore, the total current added in the LSLFP is only 6  $\mu$ A per each channel.

The simulation result with these parameters is shown in the lower left of Fig. 2. It suggests that our CM technique can be expected to reduce  $f_{3dB}$  from 3 MHz to 10.5 kHz. Without the CM technique,  $f_{3dB}$  is the result of the resistors  $R1$  and  $R2$  and the gate capacitance of a multiplexer.

### III. MEASUREMENT RESULTS

A prototype of an automotive MCU including our LSLPFs was fabricated in 0.18  $\mu$ m 1-poly 5-metal BCDMOS technology, and the input interface used 3.3 V thick-gate-oxide MOS transistors. Fig. 3 shows the die micrograph. The magnified layout shows the LSLPF which only takes up a small area. Each of the 32-channel LSLPFs occupies an area of 50  $\mu$ m $\times$ 320  $\mu$ m which is only 0.45% of the input interface.

To assess the effectiveness of the filtering function in the LSLPF, we generated a 50 mV<sub>pp</sub> sinusoid regarded as noise on top of 6 V DC and applied the signal to one input channel. The sinusoid passes through the LSLPF, PGA, and SAR ADC, and the output codes of the ADC can be seen as shown in Fig. 4. When the CM technology is activated, it can be seen that the 500 kHz sine wave peak-to-peak output code is reduced from about 50 LSBs to 15 LSBs, which signifies that the noise has been filtered. The Nyquist theorem indicates that the  $x$ -axis cannot extend beyond 500 kHz. The measured signal-to-noise-plus-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) of the input interface are shown in Fig. 5(a). The SNDR remains above 60 dB up to an input frequency of 20 kHz, as shown in Fig. 5(b). In addition, the prototype was tested in the temperature range of -40  $^{\circ}$ C to 150  $^{\circ}$ C considering automotive applications, and the measured SNDR is maintained above 60 dB as shown in Fig. 5(c). The total current consumption of the input interface is 3.1 mA, and the current used by the LSLPF is 6  $\mu$ A for each channel. Therefore, each of the 32-channel LSLPFs consumes

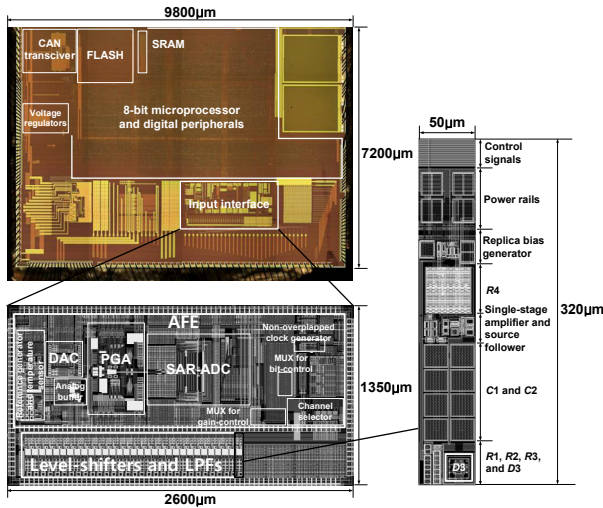


Fig. 3. Die micrograph with magnified layouts.

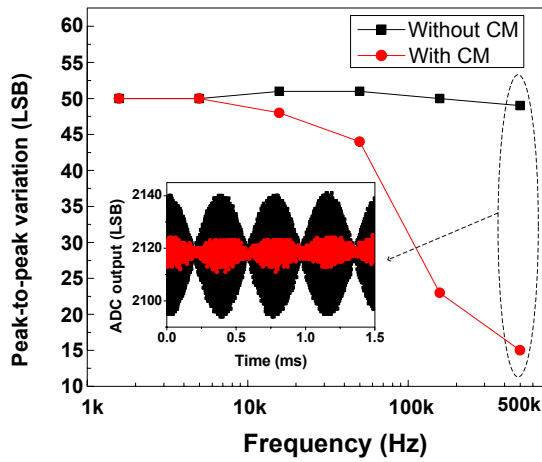
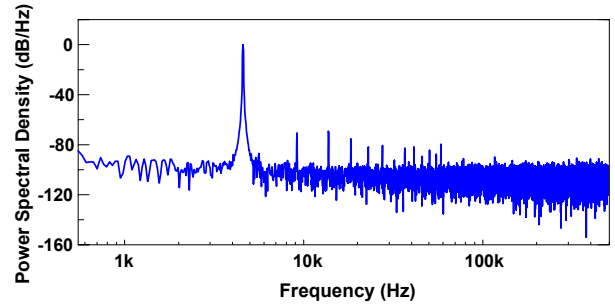


Fig. 4. Measured filtering function of the LSLPF.

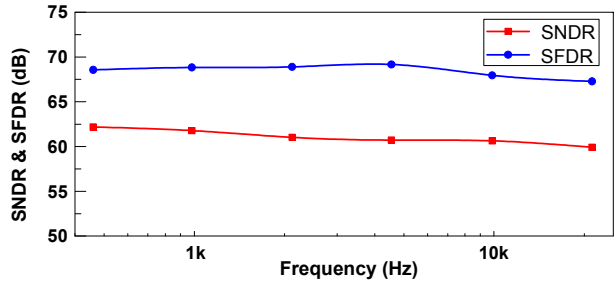
only about 0.2% of the total current. Table 1 summarizes the key parameters of our input interface included in the automotive MCU and compares them with previous works.

#### IV. CONCLUSION

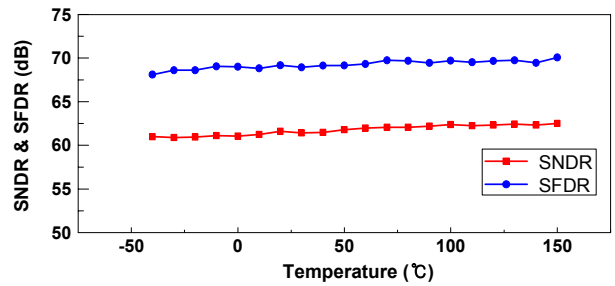
We have shown how a LSLPF using DC-decoupled capacitance multiplication can be used in the integrated input interface of an automotive MCU to reduce the requirement for external components. Each of the 32-channel LSLPFs draws  $6 \mu\text{A}$  which is only about 0.2% of the total current consumed by the input interface, and each channel takes up about 0.45% of the area of the input interface. To provide the programmability of input



(a)



(b)



(c)

Fig. 5. Measured output of the input interface (a) output spectrum for a  $4.8 V_{pp}$  4.58 kHz sinusoidal input signal, (b) SNDR and SFDR versus input frequency, (c) SNDR and SFDR versus temperature.

signals, our input interface not only receives battery-level inputs, but also provides analog-specific functions such as low-pass filtering by capacitance multiplication and gain control using a PGA. Inputs are digitized by a 12-bit 1 MS/s SAR ADC and a channel is selected using multiplexers.

#### ACKNOWLEDGEMENTS

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT).

**Table 1.** Key parameters of our MCU and its input interface

Parameter		This work	Wang et al. [3]	Specks et al. [4]
Technology		0.18 $\mu\text{m}$ BCDMOS	0.18 $\mu\text{m}$ flash CMOS	0.18 $\mu\text{m}$ HV flash CMOS
Operating temperature		-40 °C to 150 °C	-40 °C to 125 °C	-40 °C to 125 °C
MCU	CPU	8b 8 MHz	8b 40 MHz	16b 8 MHz
	Memory	32 KB flash, 4 KB SRAM	128 KB flash, 6 KB SRAM, 2 KB EEPROM	60 KB flash, 2 KB SRAM, 1 KB EEPROM
Input interface	Supply voltage	3.3 V	1.8 V	5 V
	Input range	12 V	1.8 V	14 V (switch), 5 V (analog and pulse)
	Level-shifter	12 V or 5 V to 3 V	No	14 V to 5 V (switch)
	Low-pass filter	Internal with capacitance multiplication	No	No
	A/D conversion	32-channel 12b 1 MS/s SAR	16-channel 10b 1 MS/s SAR	12-channel 10b
	Analog gain	Up to 12	No	No
	Performance	60.7 dB SNDR 70.1 dB SFDR	60.64 dB SNDR 73.60 dB SFDR	-
	Current consumption	3.1 mA	-	-
Area	Total	70.56 mm <sup>2</sup>	10.62 mm <sup>2</sup>	88 mm <sup>2</sup>
	Input interface	3.51 mm <sup>2</sup>	-	-
	32-channel LSLPFs	0.512 mm <sup>2</sup>	-	-

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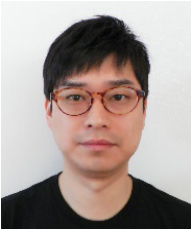
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