A PVT-compensated 2.2 to 3.0 GHz Digitally Controlled Oscillator for All-Digital PLL

Anil Kavala, Woorham Bae, Sungwoo Kim, Gi-Moon Hong, Hankyu Chi, Suhwan Kim, and Deog-Kyoon Jeong

Abstract—**We describe a digitally controlled oscillator (DCO) which compensates the frequency variations for process, voltage, and temperature (PVT) variations with an accuracy of ±2.6% at 2.5 GHz. The DCO includes an 8 phase current-controlled ring oscillator, a digitally controlled current source (DCCS), a process and temperature (PT)-counteracting voltage regulator, and a bias current generator. The DCO operates at a center frequency of 2.5 GHz with a wide tuning range of 2.2 GHz to 3.0 GHz. At 2.8 GHz, the DCO achieves a phase noise of -112 dBc/Hz at 10 MHz offset. When it is implemented in an all-digital phase-locked loop (ADPLL), the ADPLL exhibits an RMS jitter of 8.9 ps and a peak to peak jitter of 77.5 ps. The proposed DCO and ADPLL are fabricated in 65 nm CMOS technology with supply voltages of 2.5 V and 1.0 V, respectively.**

Index Terms—**Digitally controlled oscillator, ring oscillator, PVT compensated DCO, PT-counteracting voltage regulator, all-digital phase-locked loop**

I. INTRODUCTION

The ring-type DCO is perhaps the most widely used element in mixed-signal applications over its LC-type counterpart, with the advantages of generating a multiphase clock with a wide frequency tuning range in a small area. Apart from its advantages, its frequency is quite sensitive to process, voltage, and temperature (PVT) variations, which limits its use in many applications. In order to ensure correct locking across all these frequency variations in all-digital phase-locked loops (ADPLLs) [1, 2], the DCOs are designed with an extremely wide tuning range which leads to decrease in DCO frequency resolution. This decrease in resolution causes high quantization noise, which is one of the main noise sources of an ADPLL. Also, the loop stability and bandwidth of the ADPLL are strongly dependent on the DCO gain which varies widely due to PVT variations. Therefore, a PVT-tolerant DCO with high frequency resolution is essential to achieve better performance.

The ring-type DCOs with a digitally controlled resistor (DCR) were proposed for high-frequency resolution applications with a wide frequency tuning range [3, 4]. However, their phase noise deteriorates at low supply voltages, due to the voltage drop in their DCR in the main current path of the oscillation. Also, the DCR implemented with on-chip resistors is quite sensitive to PVT variations, which results in a wide DCO resolution variation.

A lot of effort has already been put into overcoming the oscillator frequency PVT variations. The recent oscillator designs [5, 6, 9] which were aimed at compensating these variations while saving area without using bandgap reference (BGR) or regulator are able to compensate partially across all PVT variations. In the design of 130-MHz ring oscillator [5], the effect of PVT variations is reduced by a temperature and process compensation circuit and a replica feedback bias circuit.

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This achieved a frequency variation of ±11.52% across all PVT corners. A compensation technique shown in [6] uses an addition-based current source to supply the bias current to the oscillator. But this design does not offer supply compensation, and the accurate generation of its gate bias voltage is quite challenging without using a BGR. The oscillator in [9] which operates at high frequency is able to compensate only process and temperature variations, and also reported that its process variations are over compensated by aiming to achieve better supply compensation. Also, it is expected that there would be a trade off with temperature variations while only achieving process and supply variations which leads to increase in the temperature variations. To achieve accurate frequency compensation for all these PVT variations, the oscillators [7, 8] incorporated a BGR or a regulator. However, these oscillators are able to provide only a moderate compensation of ±5% for process and temperature variations. In one of the oscillators [8] compensation circuit composed of a constant-gm bias circuit and a regulator consumes no small current of 2.6 mA. Also, the frequency variation of these oscillators [5-8] is expected to increase at higher operating frequencies [10].

To overcome such limitations, we present a PVT-compensated high resolution DCO with a PVT-insensitive digitally controlled current source (DCCS) and a process and temperature (PT)-counteracting voltage regulator. The DCCS provides a digitally controlled current which is insensitive to PVT variations using a PVT-insensitive bias current generator with a BGR. The PT-counteracting regulator provides to the ring oscillator the supply voltage which is varied to counteract to the effect of process and temperature variations while providing supply and load regulation.

The rest of this paper is organized as follows. Section II describes our proposed DCO approach and its implementation in ADPLL. In Section III, we present measurement results from the prototype, and we summarize the paper with conclusions in Section IV.

II. PROPOSED DIGITALLY CONTROLLED OSCILLATOR

Fig. 1 shows the block diagram of the proposed PVT-compensated DCO, which consists of an eight-phase current-controlled ring oscillator, a DCCS, a bias current generator, and a PT-counteracting voltage regulator. The DCCS generates PVT-insensitive digitally controlled integral- and proportional-path currents, $I_{DCCS,INT}$ and $I_{DCCS,PROP}$, set by the integral-path frequency control code word (FCW) and the proportional-path FCW, respectively. Its PVT-insensitive reference bias current, $I_{BIAS,DCCS}$, is generated by the bias current generator. The PT-counteracting voltage regulator generates a variable supply voltage, V_{SUPPLY}, in response to PVT variations using the PVT-insensitive bias current, $I_{BIAS,REG}$, of the bias current generator and the negative-to-absolute temperature (NTAT) current, $I_{NTAT,REG}$, of the BGR. The variable supply voltage, V_{SUPPLY}, supplies the DCCS and the ring oscillator. The eight-phase current controlled ring oscillator generates equally-spaced multiphase clock signals, *Clkn[0:3]* and *Clkp[0:3]*, with a frequency controlled by $I_{DCCS,INT}$ and $I_{DCCS,PROP}$. The bias current generator and the regulator are supplied by an external supply voltage, V_{DD}.

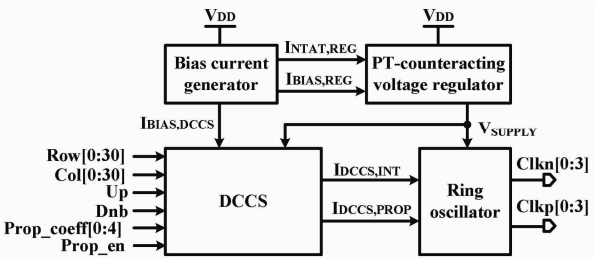


Fig. 1. DCO architecture.

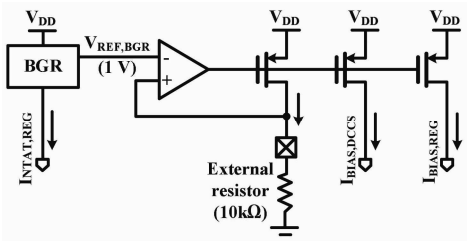


Fig. 2. Bias current generator.

1. Bias Current Generator

Fig. 2 shows a bias current generator circuit which converts the reference voltage of BGR, $V_{REF,BGR}$, into the PVT-insensitive bias currents $I_{BIAS,DCCS}$ and $I_{BIAS,REG}$, which are supplied to the DCCS and the PT-counteracting voltage regulator. It also provides the

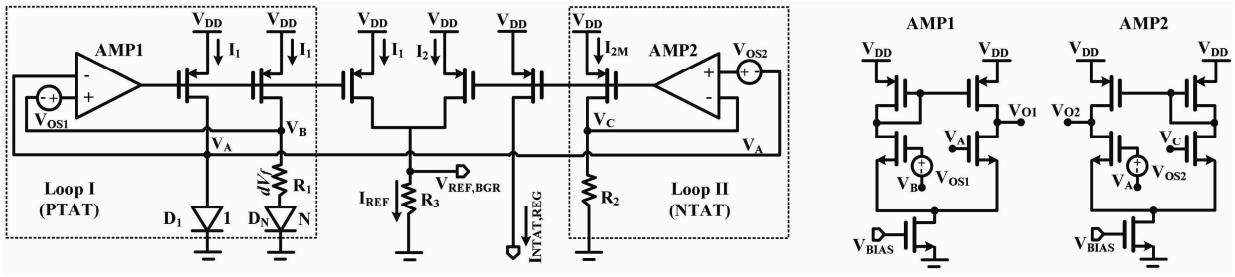


Fig. 3. (a) BGR, (b) BGR operational amplifiers.

$I_{NTAT,REG}$ current from its BGR to the regulator. A stable external resistor is used in this bias current generator as a reference. Current mirroring is used to distribute bias currents for various sub-blocks in the chip.

The BGR used in the bias current generator consists of a special current-summing method that reduces the output sensitivity to the operational amplifiers offset voltages of the operational amplifiers as shown in Fig. 3(a). The BGR circuit has two loops: a proportional- to-absolute temperature (PTAT) loop generates a variable current with a positive temperature coefficient (TC), and an NTAT loop which generates a current with a negative TC. In the PTAT loop, the voltage difference between the inputs of diodes D_1 and D_N is d_{Vf}, which is proportional to the product of the thermal voltage V_T and $ln(N)$, where N represents the ratio of the junction areas of the two diodes. The PTAT current I_1 has a positive TC, since the thermal voltage V_T is proportional to the absolute temperature. In the NTAT loop, the forward bias voltage V_{f1} of D_1 changes in the opposite direction to the temperature variation, so the current I_2 will have a negative TC. The summing of these two currents by choosing appropriate values for the resistors (R_1, R_2, and R_3), we generate a zero TC reference voltage, $V_{REF,BGR}$. The operational amplifiers bias voltage, V_{BIAS}, is generated using a diode-connected PMOS transistor and a resistor. The two operational amplifiers used in the BGR have systematic and random offset voltages, leading to current errors in their outputs. We partially overcome this by taking advantage of the offset-matching characteristic of these operational amplifiers. The errors in the output currents cancel each other if the systematic offsets of these two operational amplifiers are made to oppose each other by connecting the outputs of the differential pairs directly in one operational amplifier, and making a cross connection in the other, as shown in Fig. 3(b). The output errors due to the matching offsets, V_{OS1} and V_{OS2}, will then cancel each other, as expressed by the following expression for $V_{REF,BGR}$:

$$V_{REF,BGR} = \left(\frac{R_3}{R_1}\right)\cdot dV_f + \frac{R_3}{M\cdot R_2}\cdot V_{f1} - \left(\frac{R_3}{R_1}\cdot V_{OS1} - \frac{R_3}{M\cdot R_2}\cdot V_{OS2}\right). \quad (1)$$

2. Digitally Controlled Current Source

The proposed DCCS is implemented with integral- and proportional-path tuning circuits, as shown in Fig. 4. Its integral-path tuning is implemented with 1024 PMOS unit current sources rather than the unit resistors of [3, 4]. All these unit cells are identical and connected in an array, but they are arranged with even- and odd-numbered cells. The 10-bit integral-path FCW is converted into row and column thermometer codes to control the segmented array of current sources. Progression of an example integral-path FCW is discussed in [3] and shows how to avoid glitches with the thermometer code when FCW is incremented or decremented by one. The unit cell current source is composed of two current source PMOS transistors, M_1 and M_2, and a digital logic implemented with an or-and-invert (OAI) gate. All the transistors of the bias circuit as well as the unit cell transistors, M_1 and M_2, operate in saturation. All these unit cells generate a PVT-insensitive current over all PVT variations, since they are mirrored by the PVT-insensitive bias current, $I_{BIAS,DCCS}$, via Pcs and $Pcas$. The DCCS produces a PVT-insensitive integral-path current, $I_{DCCS,INT}$, with FCW by adding all these unit-cell currents together.

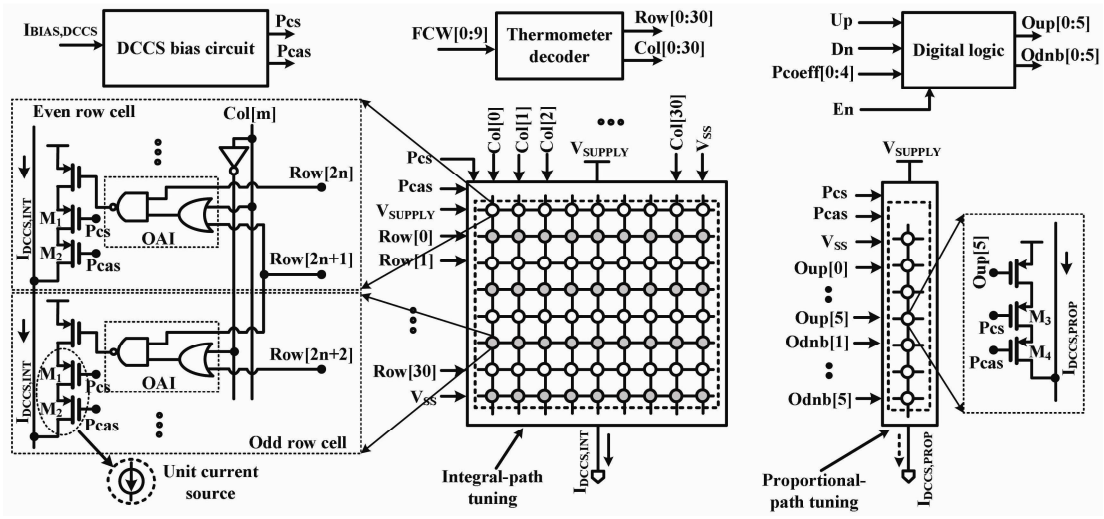


Fig. 4. DCCS integral and proportional tuning.

The DCCS proportional-path tuning is composed of twelve PMOS unit current sources in a linear array and a digital logic, unlike the capacitors at the delay cell output of [4]. Its PMOS unit current source is similar to the design of the DCCS integral tuning PMOS unit cell. The proportional-path tuning circuit is enabled by the *En* signal and its change in current polarity is determined by the *Up* and *Dn* signals. These unit cell currents are added together to generate a DCCS proportional-path tuning current, $I_{DCCS,PROP}$. The tuning circuit is used for adaptive proportional gain control of the ADPLL, using 5 bits of the proportional coefficient to reduce the ADPLL jitter [4].

3. Ring oscillator

The ring oscillator is composed of four identical differential delay cells, as shown in Fig. 5, each of which consists of two main inverters, two latch inverters, and two NMOS current source transistors (M_5 and M_6). The delay cells currents, $I_{OSC,INT}$ and $I_{OSC,PROP}$, are determined by the NMOS current source transistors, which are in turn controlled by mirroring the DCCS integral- and proportional-path tuning currents, $I_{DCCS,INT}$ and $I_{DCCS,PROP}$, to generate eight multiphase clock signals, *Clkn[0:3]* and *Clkp[0:3]*.

Therefore, the frequency of the ring oscillator varies proportional to its DCCS tuning current. The frequency of an *N*-stage ring oscillator, F_{OSC}, is expressed primarily as

$$F_{OSC} = \frac{I_{OSC,INT} + I_{OSC,PROP}}{2 \cdot N \cdot C_L \cdot V_{SWING}} = \frac{\alpha \cdot I_{DCCS,INT} + \beta \cdot I_{DCCS,PROP}}{2 \cdot N \cdot C_L \cdot V_{SWING}}, \quad (2)$$

where N is the number of delay cells, C_L is the load capacitance of the delay cell, V_{SWING} is the rail-to-rail voltage swing of the oscillation, α and β are the integral and proportional current ratio of the oscillator and the DCCS, respectively.

From (2), we see that the oscillation frequency is primarily determined by the PVT-insensitive DCCS integral- and proportional-path tuning currents and the oscillator voltage swing, V_{SWING}, which is same as V_{SUPPLY}. However, the PVT-insensitive DCCS current with a constant V_{SUPPLY} alone cannot achieve the frequency compensation fully for PVT variations, since various other factors such as variations in transistor threshold voltage, mobility, channel length, width, gate oxide capacitance, and load capacitance due to process and temperature variations can have secondary effects on the oscillation [6-11]. To compensate these secondary variations further, the oscillator supply voltage, V_{SUPPLY}, must be varied instead of just regulating the output voltage at a constant value.

4. PT-counteracting Voltage Regulator

In our voltage regulator, we have adapted a regulator which compensates the oscillator process and

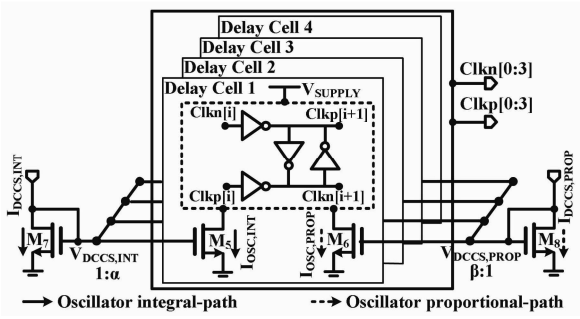


Fig. 5. Ring oscillator.

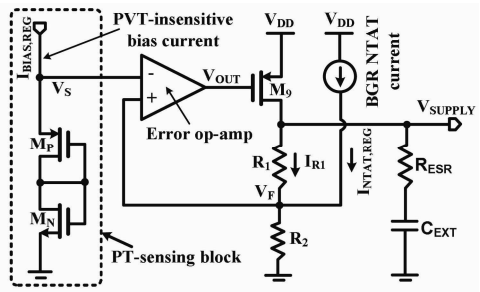


Fig. 6. PT-counteracting voltage regulator.

temperature variations [8] to generate V_{SUPPLY} which reflects PT variations to counter-act the effect of the PT variation of the ring oscillator due to secondary effects. As shown in Fig. 6, it consists of a PT-sensing block with diode-connected NMOS and PMOS transistors, M_N and M_P, an error op-amp, a PMOS pass transistor M_9, and feedback resistors R_1 and R_2.

The PT-counteracting voltage regulator uses the PVT-insensitive bias current, $I_{BIAS,REG}$, from the proposed bias current generator instead of using a separate constant-g_m bias circuit current [8]. This approach also helps to overcome the power overhead of constant-g_m bias circuit. The PT-sensing block generates a process and temperature-dependent voltage, V_S, from $I_{BIAS,REG}$, from which the regulator generates a supply voltage which reflects PT changes. Here, the transistors M_N and M_P are the replica of ring oscillator delay cell transistors. The sense output V_S is expressed as

$$V_S = V_{TH,N} + \left|V_{TH,P}\right| + \sqrt{\frac{2 \cdot I_{BIAS,REG}}{C_{OX,N} \cdot \mu_N} + \frac{2 \cdot I_{BIAS,REG}}{C_{OX,P} \cdot \mu_P}}. \tag{3}$$

The NTAT current, $I_{NTAT,REG}$, from the BGR, having a negative temperature coefficient, is used to compensate

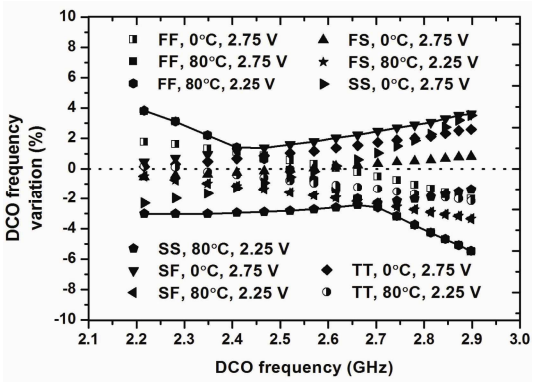


Fig. 7. Simulated overall DCO frequency variations for PVT.

the V_{SUPPLY} dependency with temperature variations. The feedback node voltage, V_F, is expressed as

$$V_F = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V_{SUPPLY} + \left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right) \cdot I_{NTAT,REG.} \tag{4}$$

Thus, the output voltage of regulator is expressed as

$$V_{SUPPLY} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_S - R_1 \cdot I_{NTAT,REG.} \tag{5}$$

From (5), the generated V_{SUPPLY} is a function of V_S and $I_{NTAT,REG}$ and it can be adjusted by properly selecting the resistances R_1 and R_2.

Under process variations, for example, when the circuit is in FF[1] process corner, the node voltage V_S decreases, since the mobilities, μ_N and μ_P, increase and the threshold voltages, $V_{TH,N}$ and $\left|V_{TH,P}\right|$, decrease [9]. Hence, from (5), the V_{SUPPLY} decreases causing the ring oscillator to slow down. Basic assumption is that the voltage across the diode-connected pair flowing the constant current tracks the voltage required to yield a constant delay time. Hence, with SS process corner, V_{SUPPLY} will increase to speed up the delay time of the cell. However, under skewed process corners such as FS and SF corner, the delay tends to be determined by the sum of variations and therefore its effect is equivalent to TT process corner. Under supply voltage variation, V_S does not change since the PT-sensing block is supplied by the PVT-insensitive bias current.

[1] The process corner 'XY' refers to 'NMOS: X and PMOS: Y', with X and Y replaced by either of F=fast, S=slow, and T=typical.

Table 1. DCO required and achieved variable supply voltages

PT Corners (V_{DD}= 2.5 V)	Required	Achieved			
	V_{SUPPLY}(V)	V_S(V)	V_{SUPPLY} (V)	F_{OSC} (GHz)	Frequency Error (%)
FF, 0°	0.889	0.823	0.896	2.517	0.676
FF, 40°	0.896	0.782	0.898	2.504	0.144
FF, 80°	0.902	0.743	0.905	2.506	0.220
FS, 0°	1.044	0.886	1.043	2.498	-0.072
FS, 40°	1.060	0.845	1.044	2.478	-0.868
FS, 80°	1.079	0.805	1.050	2.463	-1.488
TT, 0°	1.041	0.893	1.060	2.523	0.924
TT, 40°	1.061	0.852	1.062	2.500	0.000
TT, 80°	1.089	0.813	1.068	2.483	-0.684
SF, 0°	1.045	0.901	1.077	2.538	1.504
SF, 40°	1.066	0.860	1.080	2.516	0.628
SF, 80°	1.084	0.821	1.087	2.504	0.172
SS, 0°	1.245	0.967	1.225	2.483	-0.672
SS, 40°	1.285	0.926	1.226	2.456	-1.760
SS, 80°	1.332	0.887	1.233	2.431	-2.780

When the temperature increases, the threshold voltages and the mobilities of M_P and M_N transistors decrease [11]. Since the decrease in threshold voltages dominate the decrease in mobilities unless the currents flowing through those transistors are much larger than their zero temperature coefficient (ZTC) currents [11], V_{SUPPLY} decreases along with V_S. At the same time, the decrease in $I_{NTAT,REG}$ due to the negative temperature coefficient helps to increase the V_{SUPPLY}. Hence, combined effect of V_{SUPPLY} can be made to increase slightly in order for the ring oscillator to speed up with the overall effect of constant oscillation frequency.

The second column in Table 1 shows the simulation results of the required supply voltages for the oscillator to generate an oscillation frequency of 2.5 GHz under process and temperature variations shown in the first column. The numbers in the fourth column indicates the generated V_{SUPPLY} by the PT-counteracting regulator which would ideally be identical to the numbers in the second column under the same PT conditions. R_1 (190 kΩ), R_2 (156 kΩ) and $I_{NTAT,REG}$ (4.3 μA) are selected to give the minimum errors over all process and temperature corners as well as all DCCS FCWs. In our design, V_{SUPPLY} is also used as DCCS supply voltage to track PVT variations more closely. The simulation results of our overall DCO frequency variations from its typical PVT corner (TT, 40°C, 2.5 V) across all FCWs with the frequency range of 2.2 GHz to 2.9 GHz are shown in Fig. 7. The DCO frequency variation is 3.8% to -3.0% at 2.2 GHz, 1.5% to -2.8% at 2.5GHz, and 3.6% to -5.5% at 2.9 GHz.

5. DCO Implementation in ADPLL

The block diagram of an ADPLL is shown in Fig. 8 which consists of a phase-frequency-detecting time-to-digital converter (PFD-TDC) [12], a second-order synthesizable digital loop filter (DLF), an 8-bit first-order delta-sigma modulator (DSM) for DCO, a DCO, a divider for the DLF, and a feedback divider. The ADPLL uses a reference clock, *Refclk*, of 40-MHz frequency. The PFD-TDC compares the arrival time of the *Refclk* edge with that of divided DCO clock, *Divclk*, edge, and generates *Up, Dn* signals, and also a thermometer code, *Thermo*. The DLF is used to filter the phase noise, and the resulting values are fed into the DSM to dither the output clock of the DCO with its generated FCW to improve the frequency resolution. The output frequency of the DCO is divided by a feedback divider having a dividing factor of *N* to generate *Divclk*. A second-order DSM is used to randomize the dividing factor of the feedback divider through its digital divider controller.

III. MEASUREMENT RESULTS

The proposed DCO is implemented in a fractional-*N* ADPLL to verify its applicability to enhance the ADPLL performance. The ADPLL with the proposed DCO has

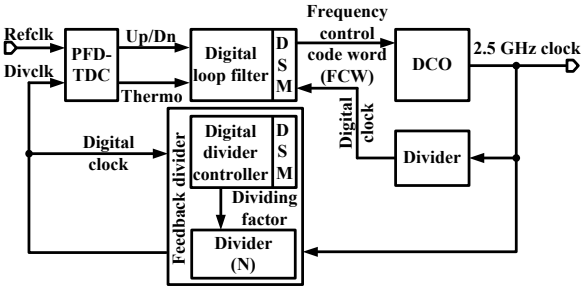


Fig. 8. Fractional-N ADPLL block diagram.

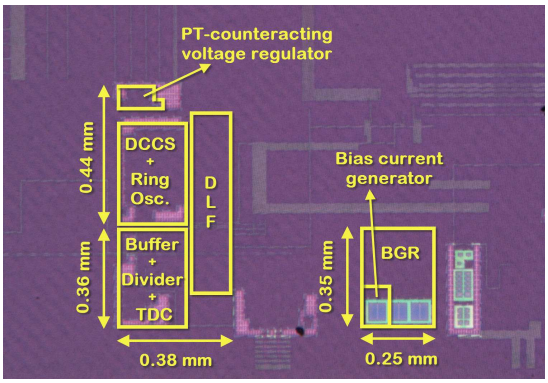


Fig. 9. ADPLL die microphotograph.

been fabricated using 65 nm CMOS technology and its die photomicrograph is shown in Fig. 9. Excluding BGR, the DCO occupies 0.074 mm^2. The area consumed by the BGR is excluded since it is a common block shared with other blocks.

Fig. 10 is a plot of measured DCO frequency gain curve for four sample devices at room temperature with 2.5 V supply voltage. The frequency variation at the minimum frequency of 2.24 GHz is ±1.69% and that at the maximum frequency of 3.07 GHz is ±1.00%. At 2.5 GHz, the measured frequency variation at room temperature is ±1.4% which is in good agreement with the simulated process variation of +0.58% to -1.70%. Therefore, the accurate PVT-insensitive current of DCCS and the additional process compensation by the PT-counteracting voltage regulator achieve good frequency compensation across all process variations. The DCO operates with the tuning range of 0.83 GHz and with an average resolution of 0.81 MHz. The resolution varies between 0.59 MHz and 1.08 MHz because, although the DCCS tuning current is linear with the control code, the DCO frequency is nonlinear. For better linearity, the size of the DCCS unit cells can be varied [4].

The measured DCO frequency variations at room

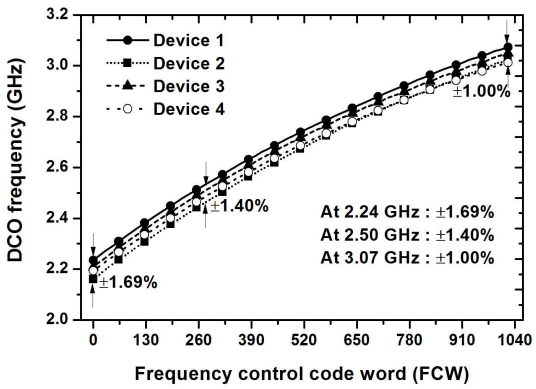


Fig. 10. Measured tuning frequency with FCW.

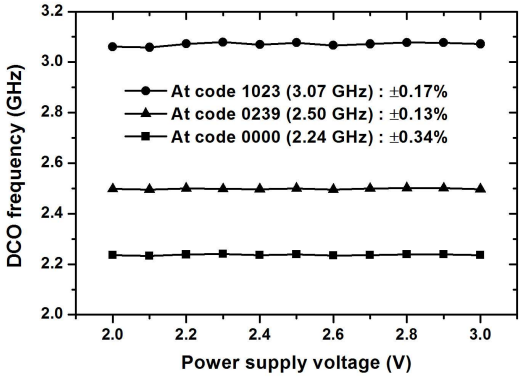


Fig. 11. Measured DCO frequency against supply variation.

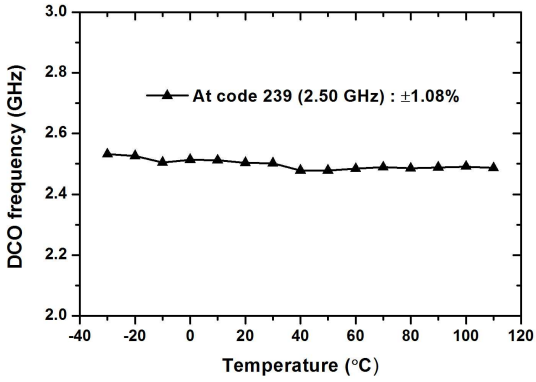
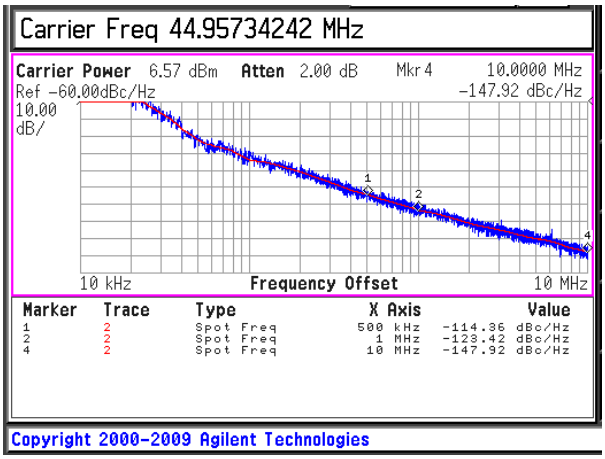


Fig. 12. Measured DCO frequency against temperature.

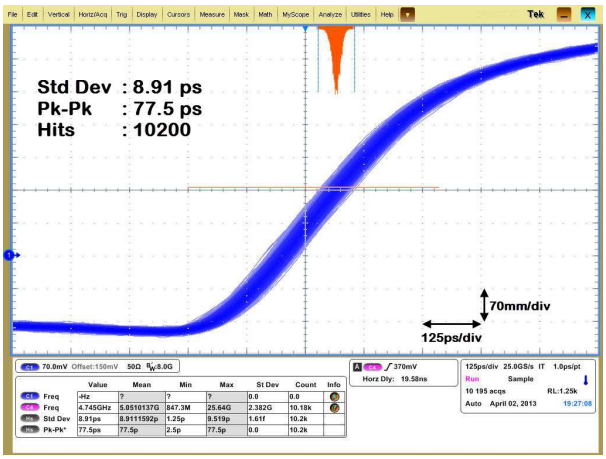
temperature for Device 1 against the supply voltage variation are shown in Fig. 11. For the supply voltage variation from 2.0 V to 3.0 V, the measured frequency varies by ±0.13% at 2.5 GHz which is quite small as the PT-counteracting voltage regulator provides a constant supply voltage across supply variations to both the DCCS, which is itself supply insensitive, and the ring oscillator. Fig. 12 shows that the measured DCO

Table 2. Performance comparison of the DCO

		[5]	[6]	[7]	[8]	This work
Technology		CMOS 0.18 μm	CMOS 90 nm	CMOS 0.18 μm	CMOS 0.13 μm	CMOS 65 nm
Supply Voltage		1.8 V	1 V	1.8 V	3.3 V	2.5V
Number of Phases		6	3	6	4	8
Center Frequency		130 MHz	1.8 GHz	632 MHz	1.25 GHz	2.5 GHz
Tuning Range		N/A	N/A	N/A	380 MHz	830 MHz
Phase Noise at 10 MHz offset		N/A	-103.87 dBc/Hz at 2 GHz.	-92 dBc/Hz at 632 MHz	-108dBc/Hz at 1.25 GHz	-112 dBc/Hz at 2.8 GHz
Frequency Variation for PVT	Process	±1.13%	5.80% (167 chips)	4.40% (6 chips)	±5% (15 chips and - 40°C~125°C)	±1.40% (4 chips)
	Temperature	±4.99% (0°C~100°C)	0.47% (6.8°C~61.8°C)	5.60% (0°C~80°C)		±1.08% (-30°C~110°C)
	Voltage	±5.40% (1.62V~0.12V)	N/A	N/A	N/A	±0.13% (2.0V~3.0V)
BGR and Regulator		NO	NO	YES	YES	YES
Current Consumption		1.52 mA @ 130 MHz	0.087 mA @ 1.8 GHz	0.74 mA @ 632 MHz	3.4 mA @ 1.25 GHz	2.3 mA @ 2.24 GHz 3.1 mA @ 3.07 GHz



(a)



(b)

Fig. 13. ADPLL (a) DCO phase noise, (b) Jitter performance.

frequency varies by ±1.08% at 2.5 GHz for temperatures from -30°C to 110°C. The measured DCO frequency variation for temperatures from -30°C to 110°C is in good agreement with the simulation result of +1.71% to -0.92% at the TT process corner. Therefore, the DCCS PVT-insensitive current achieves better temperature compensation. Moreover, its small frequency under-compensation is compensated by the slight increase in the supply voltage of the PT-counteracting voltage regulator as the temperature increases. The temperature variations of the DCO frequency were measured at intervals of 10°C, using a temperature chamber. As shown in Fig. 13(a), the DCO has a phase noise of -112 dBc/Hz at 10 MHz frequency offset with the operating frequency of 2.8 GHz. The DCO frequency and the phase noise were measured at the divider output due to limited number of package pins, having a dividing factor of 62.5. At its locking condition, the ADPLL with the bandwidth of 1.3 MHz exhibits an RMS jitter of 8.9 ps and a peak-to-peak jitter of 77.5 ps as shown in Fig. 13(b).

The DCO consumes a current varying from 2.3mA at 2.24 GHz to 3.1 mA at 3.07 GHz. The buffer used in this oscillator consumes 1.2 mA to drive the ADPLL blocks with a 50% duty cycle. The bias current generator including BGR and the regulator circuits consume less than 280 μA and 28 μA, respectively, across all PVT corners. Table 2 compares this DCO with other PVT compensation oscillator designs [5-8]. It is observed that the proposed DCO has lower phase noise than the other PT or PVT-compensated oscillators, and also it has a

wide tuning range whereas the others have no tuning range [5-7] or only a moderate tuning range [9]. Also, it operates at a high operating frequency while generating eight multiphase clock signals. The current consumption of this DCO is relatively higher than the other oscillators except [8] due to its high frequency of operation and a wide tuning range. Overall, the proposed DCO achieved the lowest frequency variation of ±2.6% at 2.5 GHz for a wide range of PVT variations among the oscillators which are able to achieve only a moderate frequency compensation across either PVT or only PT variations.

V. CONCLUSIONS

We present a 2.5 GHz digitally controlled oscillator with a PVT-insensitive DCCS, PT-counteracting voltage regulator and bias current generator for offering a PVT-invariant and predictable oscillation frequency with low variations. It reduces the frequency variations down to ±2.6% at 2.5 GHz across all PVT corners. The oscillator control current is generated by the DCCS PVT-insensitive tuning current using bias current generator with BGR to compensate PVT variations and its variable supply voltage is generated by the PT-counteracting voltage regulator to counter act the process and temperature variations further. The ADPLL with the proposed DCO has been fabricated using a CMOS 65nm technology. The 10-bit DCO has a wide tuning range of 2.24 GHz to 3.07 GHz with a high resolution of 0.81 MHz and with an 8-bit DSM of 3.1 kHz, while consuming between 2.3 mA and 3.1 mA. It exhibits a phase noise performance of -112 dBc/Hz at a 10 MHz offset, and the ADPLL has an RMS jitter of 8.9 ps.

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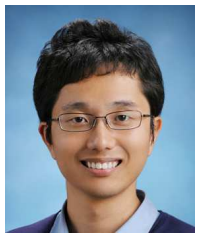

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