A 12-bit 3 MS/s Asynchronous Comparator-Based Cyclic ADC with an Adjustable Threshold Voltage Comparator

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Abstract

In this paper, we propose an asynchronous comparator-based cyclic analog-to-digital converter (ADC) with an adjustable threshold voltage to improve the conversion rate that is limited by the long charging and discharging time in the conventional comparator-based switched capacitor (CBSC) circuit. Our asynchronous timing and the adjustable threshold voltage of the comparator improves the conversion rate by reducing undesired undershoot and overshoot of the residual signal, keeping the advantages of the CBSC circuit such as low supply voltage operation and low power consumption. Post-layout simulation results show that the signal-to-noise and distortion ratio (SNDR) is 64.9 dB and a spurious-free dynamic range (SFDR) is 69.7 dB at the sampling rate of 3 MS/s and the Nyquist rate input frequency. The chip is designed with a 0.18 μm CMOS process and has an effective area of 0.25 mm^2 and a power consumption of 1.6 mW at 1.8V supply.

Keywords: Asynchronous circuit, comparator-based switched capacitor (CBSC) circuit, cyclic analog-to-digital converter (ADC).

1. Introduction

In recent years, portable devices have become more popular and demand for small and low power circuits is increasing. As technology scaling continues, digital circuits operate faster and consume less power with shortened gate lengths and lower supply voltages, but it results in problems in the design of analog circuits such as opamps. The technology scaling makes it difficult to design high-performance opamps, which also makes it difficult to increase the resolution and speed of the readout integrated circuits such as analog-to-digital converters (ADCs). Among the various types of ADCs, a cyclic architecture features moderate resolution, small chip area, and low power consumption [1-2].

To overcome the design challenges for opamps, various alternatives such as an open-loop residue amplifier [3], a comparator-based switched-capacitor (CBSC) circuit [4], and a ring amplifier [5] have been proposed. However, the open-loop residue amplifier needs complicated digital calibration and the ring amplifier has a limited gain.

The CBSC technique replaces the role of opamps with comparators and current sources to reduce power consumption and chip area. However, the comparator-based cyclic ADCs have limitations in increasing sampling rate due to long charging and discharging time of the current sources while maintaining the adequate resolution. A boosted preset voltage scheme [6-7] has been suggested to increase the conversion rate, but the speed is still limited due to undershoot and overshoot of the residual signal.

In this paper, we propose a method to improve the conversion speed by applying asynchronous timing to the multi-level boosted preset (MBP) voltage scheme and changing the threshold voltage of the comparator in coarse and fine evaluation phases. We designed a 12-bit 3 MS/s cyclic ADC and verified its performance in post-layout simulation.

2. CBSC-Based Cyclic ADC with Multi-Level Boosted Preset Voltage Scheme

The CBSC-based cyclic ADC repeats sampling and charge transfer phases every bit conversion cycle. The sampling phase is the same as that of the opamp-based cyclic ADC, but the role of the opamp is replaced by a threshold-detection comparator and current sources in the charge transfer phase. The charge transfer phase consists of preset, coarse evaluation, and fine evaluation phases. As shown in Fig. 1, the voltage overshoot in the coarse evaluation phase is compensated by a small current source in the fine evaluation phase. The MBP scheme [7]

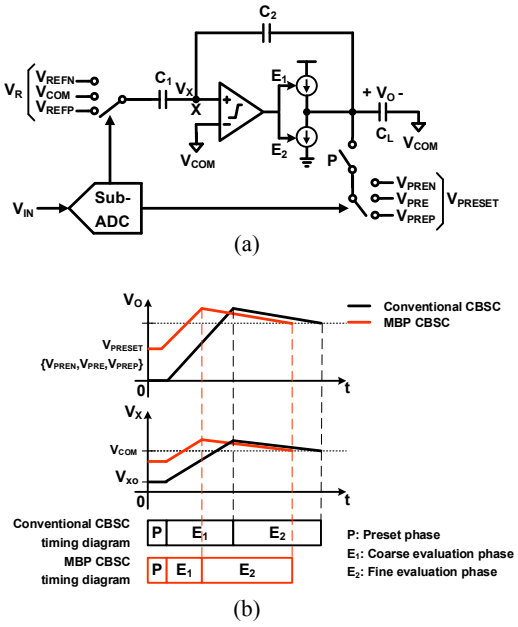

Fig. 1 (a) Gain stage and (b) transient response of 1.5-bit MBP CBSC-based cyclic ADC

reduces the charge transfer time by applying different preset voltages according to the input or residue voltage, which decreases the coarse evaluation time (E_1).

The initial voltage of V_X, V_{XO} is calculated as follows:

$$V_{XO} = V_{COM} + \frac{C_1}{C_1 + C_2} V_R - V_{IN} + \frac{C_1}{C_1 + C_2} V_{PRESET} \quad (1)$$

where V_{PRESET} is the preset voltage applied to the output node and V_R is one of voltage levels which are V_{COM}-V_{REF}, V_{COM}, and V_{COM}+V_{REF}. If the capacitance of C_1 and C_2 are equal, the constraint that the summing node voltage V_{XO} must be greater than zero and less than V_{COM} results in the following range of valid preset voltages:

$$V_{PRESET} \leq 2V_{IN} - V_R \quad (2)$$

Table 1 shows the range of V_{PRESET} and V_{XO}

Table 1: V_{PRESET} and V_{XO} range according to the input voltages

Input voltage	MAX(V_{PRESET})	MIN(V_{XO})
$V_{COM} - V_{REF} \leq V_{IN} < V_{COM} - \frac{1}{4}V_{REF}$	$V_{COM} - V_{REF}$	$V_{COM} - \frac{3}{4}V_{REF}$
$V_{COM} - \frac{1}{4}V_{REF} \leq V_{IN} < V_{COM} + \frac{1}{4}V_{REF}$	$V_{COM} - \frac{1}{2}V_{REF}$	$V_{COM} - \frac{1}{2}V_{REF}$
$V_{COM} + \frac{1}{4}V_{REF} \leq V_{IN} < V_{COM} + V_{REF}$	$V_{COM} - \frac{1}{2}V_{REF}$	$V_{COM} - \frac{3}{4}V_{REF}$

calculated from (2) and well-known 1.5-bit stage residue transfer characteristics.

3. Proposed Asynchronous Cyclic ADC with Adjustable Threshold Voltage Comparator

A. Asynchronous Operation

In the conventional synchronous cyclic ADC, each bit conversion time is fixed. That is, even if the bit conversion ends before the next bit clock is activated, the next bit conversion cannot start. Therefore, the sampling rate is limited by the maximum bit conversion time that should be long enough to distinguish small difference inputs. Fig. 2shows that the speed of a cyclic ADC using asynchronous timing is improved. In the asynchronous operation, each bit conversion can start immediately after the previous bit conversion ends. During the time remaining after all bit conversions have been completed, the cyclic ADC enters sleep mode until the next sampling phase to reduce power consumption.

Fig. 3 shows the finite-state machine (FSM) of the proposed asynchronous cyclic ADC. The sampling state moves to the preset state after the sampling period $t_{d,s}$. The preset state changes to

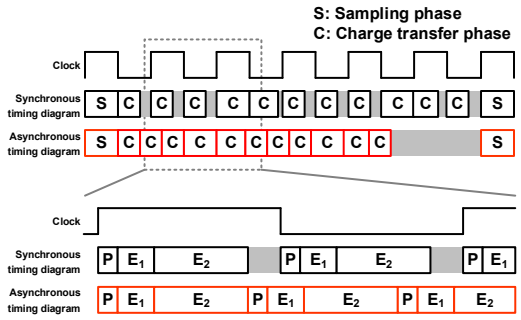

Fig. 2 The timing diagram of asynchronous cyclic ADC

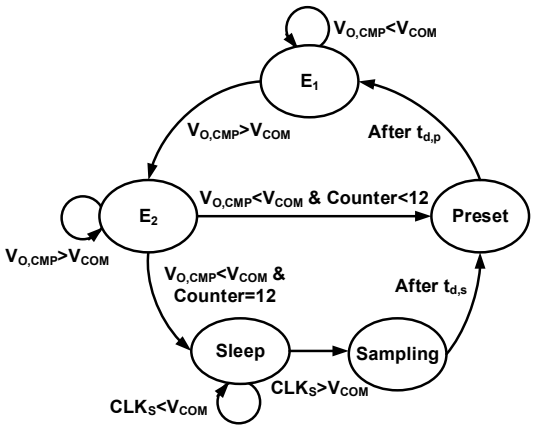

Fig. 3 The finite-state machine of the proposed asynchronous cyclic ADC

coarse evaluation state (E_1) after $t_{d,p}$. The fine evaluation state (E_2) starts when the output voltage of the comparator transitions from low to high. The sleep state is activated only when the output voltage of the comparator changes from high to low and all bit conversions are completed before the next sampling state begins. Finally, the sleep state is released when the sampling clock is activated.

B. Comparator with adjustable threshold voltage

In the CBSC-based cyclic ADC, if the amount of current used in the charge transfer phase increases to boost the operating speed, overshoot and undershoot of the residual signal occur due to comparator decision delay and logic gate delay, resulting in offset. Conventional CBSC circuits have reduced this offset to less than 1 LSB using coarse and fine evaluation phases, but this is still a limiting factor in the speed and resolution of the ADC. To further reduce this offset, the MOSFET size and power consumption of the comparator and logic gates must be increased.

The proposed comparator with adjustable threshold voltage in Fig. 4 can reduce the overshoot and undershoot amount of the residual signal without increasing the power consumption or chip area, and can further improve the speed and resolution of the ADC. The adjustable threshold voltage is implemented by controlling the bias current at the positive and negative outputs of the 1st stage comparator. MOSFET diodes connected to a 1st-stage comparator output and a 2nd-stage comparator are used to achieve high gain and fast response.

As depicted in Fig. 5 the comparator has different threshold voltages, V_{COM}-ΔV_C and V_{COM}+ΔV_F, at the coarse and the fine evaluation phases, respectively. When the threshold voltage of the comparator is changed from V_{COM} to V_{COM}-ΔV_C in the coarse evaluation phase (E_1), the overshoot voltage V_{OS2} of the proposed circuit becomes smaller than the overshoot voltage V_{OS1} of the conventional circuit even though the decision delays, $T_{d,C1}$ and $T_{d,C2}$, are the same. This shortens the conversion time. Likewise, changing the threshold voltage of the

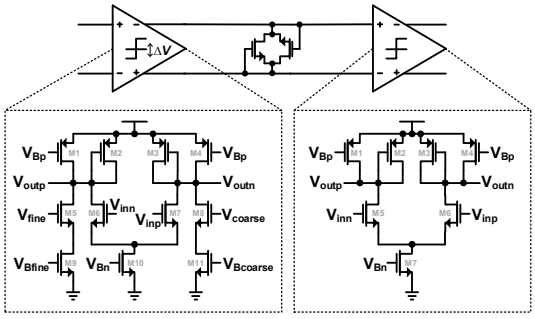

Fig. 4 The schematic of the proposed comparator

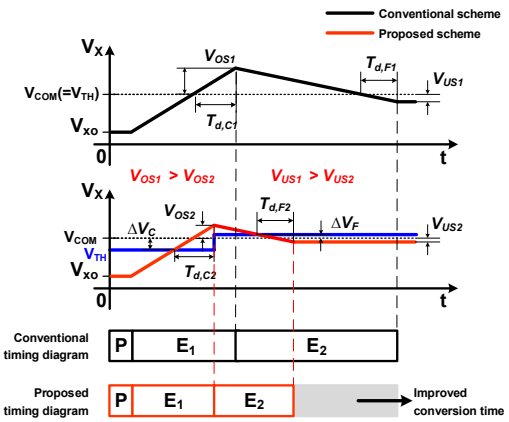

Fig. 5 The timing diagram of the proposed comparator

comparator from V_{COM} to V_{COM}+ΔV_F during the fine evaluation phase (E_2) reduces the undershoot voltage V_{US2} and shortens the conversion time. The improvement of the conversion time is calculated as follows:

$$T_{improved} = C_L\left(\frac{V_{OS1}-V_{OS2}}{I_{Coarse}} + \frac{V_{US1}-V_{US2}}{I_{Fine}}\right) \quad (3)$$

3. Simulation Results

The proposed circuit was designed in 0.18 µm CMOS technology and verified in post-layout simulations. As shown in Fig. 6, the signal-to-noise and distortion ratio (SNDR) and the spurious-free dynamic-range (SFDR) are 64.9 dB and 69.7 dB, respectively, at a sampling rate of 3 MS/s with a Nyquist-rate signal input. The power consumption is 1.6 mW with a 1.8 V supply voltage. Fig. 7 shows the layout of the designed circuit with effective area of 0.23 mm^2.

Overall performance of the proposed ADC is summarized in Table 2 in comparison with the prior art designed with 0.18 µm CMOS technology. Our ADC has the lowest figure-of-merit (FoM) of 368 fJ/conversion step.

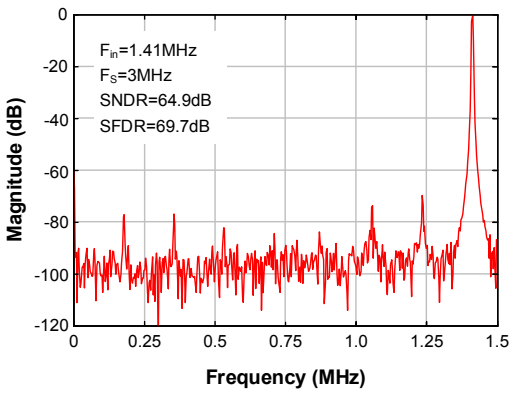

Fig. 6 Simulated output FFT spectrum

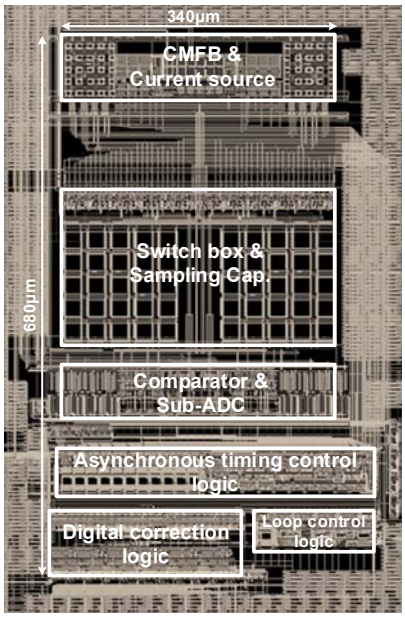

Fig. 7 The layout of the proposed cyclic ADC

4. Conclusion

In this paper, we describe an asynchronous cyclic ADC that adopts the comparator-based switched-capacitor (CBSC) technique. Asynchronous clocking reduces power consumption by putting the circuit into a sleep state after all bit conversions are completed. The comparator's adjustable threshold voltage improves resolution and sampling rate by reducing undershoot and overshoot of the residual signal. The ADC operates at 3 MS/s, and near the Nyquist-rate, the proposed ADC has a signal-to-noise and distortion ratio (SNDR) of 64.9 dB and a spurious-free dynamic-range (SFDR) of 69.7 dB. The chip was designed in 0.18 μm CMOS and it has an effective area of 0.25 mm^2 and consumes 1.6 mW from a 1.8 V supply. The figure-of-merit (FoM) is 368 fJ/conversion step.

Table 2: Summary of performance and benchmark with prior art

Parameter	[7]	[8]	[9]	This work
Supply voltage (V)	1.8	3.3	1.8	1.8
Technology (μm)	0.18	0.18	0.18	0.18
Resolution (bit)	10	10	8	12
Sampling Rate (MS/s)	2.8	14	20	3
SNDR @Nyq. (dB)	53.7	52.4	43.2	64.9
SFDR @Nyq. (dB)	61.5	65.1	N/A	69.7
Power (mW)	0.73	21.6	2.36	1.6
Effective Area (mm^2)	0.09	0.38	0.16	0.23
FoM @Nyq. (fJ/cs)	658	4,530	988	368

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