Analog Integr Circ Sig Process
DOI 10.1007/s10470-014-0406-x

A comparator-based cyclic analog-to-digital converter with multi-level input tracking boosted preset voltage

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Received: 30 June 2014 / Revised: 31 July 2014 / Accepted: 27 August 2014

Abstract In this paper, we propose a comparator-based switched-capacitor (CBSC) architecture using a multi-level input tracking preset voltage scheme. The CBSC is used to compensate for technology scaling and to reduce the power consumption of a 2.8 MS/s 10-bit cyclic analog-to-digital converter (ADC). A multi-level preset voltage tracks the input voltage in order to improve the conversion rate without consuming additional power. Additionally, a comparator, current sources, and a feedback capacitor are shared to reduce the power and area of this cyclic ADC. Near the Nyquist-rate, a prototype implemented in 0.18 μm CMOS technology has a signal-to-noise and distortion ratio of 53.69 dB and a spurious-free dynamic-range of 62.36 dB, while consuming 0.73 mW of power.

Keywords Cyclic ADC · Algorithmic ADC · Comparator-based switched-capacitor circuit (CBSC) · Boosted preset voltage · Multi-level input tracking preset voltage

1 Introduction

Integrated circuits with their own sensors are now used in many devices, running applications from automotive to biomedical. This has fueled a growing interest in low power and low voltage system with small area especially in analog-to-digital converters (ADCs), since it is difficult to realize high resolution, small area, and low power consumption simultaneously at significantly reduced supply voltages.

Successive approximation register (SAR) ADCs are currently considered to have the most power-efficient architecture [1–3]. However, their input capacitances need to be large due to the design consideration of mismatch requirement. Hence, the preceding stages, such as low-noise amplifiers or filters, are necessary in order to provide high driving capabilities. Thus the reduced power consumption of SAR ADCs may be outweighed by additional power consumption in other circuit blocks. Furthermore, the large input capacitance of an SAR ADC requires a significant area of silicon.

The pipelined ADC is an alternative architecture that largely dominates medium-to-high resolution applications. However, this architecture consists of low-resolution cascaded stages to obtain a final conversion and these stages tend to be the dominant source of power dissipation and area. Therefore, pipelined ADCs are much faster than serial-based structures such as the SAR ADC, but their area and power dissipation are larger. Additionally, as the scale of CMOS processes continues to shrink, it has become difficult to improve or even maintain the accuracy of pipelined ADCs, because they rely on a high-gain operational amplifier (opamp), which is difficult to realize with reduced supply voltage and device gain [4, 5].

The cyclic ADC [6–9] is an alternative design which can combine high resolution with a small chip area and low power, since it performs a conversion by the repeated use of a single gain stage. The conversion rates achievable by cyclic ADCs have been increasing steadily as technology

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Published online: 09 September 2014

changes and digital circuits operate faster and consume less power because of shortened gate lengths and lower supply voltages. However, scaling also causes problems similar as pipelined ADCs in the design of analog circuits such as opamps. This issue can be addressed by the use of multi-stage opamp structures, gain boosting techniques, and long channel devices biased at low current density. Additionally, techniques such as correlated level shifting [10], open-loop residue amplifier [11], gain calibration [12], and the comparator-based switched-capacitor (CBSC) technique [13] have been developed to address some of these challenges. These techniques maintain a high open-loop gain even at reduced power supply voltages, allowing the gain requirements for a given resolution to be reduced, or the opamp to be eliminated completely.

The usual CBSC technique involves a brief preset phase to ensure that one of the inputs of comparator starts below the virtual ground condition, which corresponds to the lowest system level voltage. In [14], a single boosted preset voltage scheme was proposed to enhance the operation speed without increasing power consumption. Despite the advantage in operation speed in [14], the speed is still limited by the input signal. In this work, we introduce a multi-level input tracking boosted preset voltage scheme to alleviate the problem. By changing the preset voltage in response to the input voltage, we obtain a further improvement in speed.

The design presented in this paper has additional features as follows: unlike the pipelined architecture, a cyclic ADC essentially recycles the sample-and-hold amplifier (SHA) and the multiplying digital-to-analog converter (MDAC). Using CBSC, we replace the opamp in a switched-capacitor circuit with a comparator and current sources while maintaining the same function ability. This entirely removes opamps from the design, and with them the need to stabilize a high-gain, high-speed feedback loop. As well as reducing complexity, this circumvents the trade-off between bandwidth and power, resulting in a circuit that is more suitable for scaled technologies than those using opamps. Second, there is no SHA, an extra set of MDAC and sub-ADC (SADC) stages [15] are adopted to reduce the area and power consumption. Thus, a single comparator, set of current sources, and feedback capacitor are shared between two MDACs alternately. This is akin to the opamp and capacitor sharing [16–18], and produces a further reduction in power consumption and chip area.

The rest of this paper is organized as follows: in Sect. 2, we introduce our multi-level input tracking boosted preset voltage scheme. The architecture and circuit implementation of a comparator-based cyclic ADC with the preset voltage scheme is described in Sect. 3. Measured results are presented in Sect. 4 and we conclude the paper in Sect. 5.

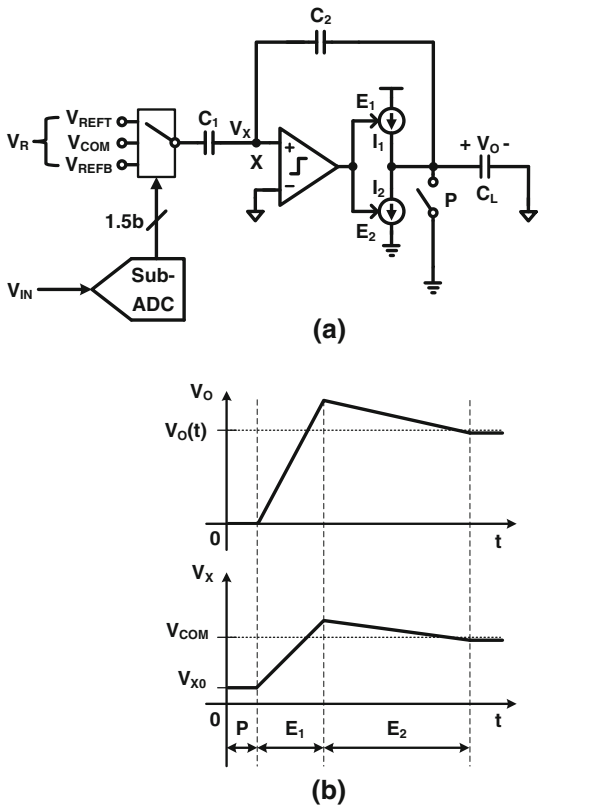

Fig. 1 **a** Charge transfer phase of a conventional comparator-based switched-capacitor gain stage and **b** its transient response

2 Multi-level input tracking boosted preset voltage scheme

A CBSC gain stage needs similar sampling and charge transfer phases as an opamp-based switched-capacitor gain stage. The sampling phase is functionally identical, even though the opamp is replaced by a threshold-detection comparator and current sources. The charge transfer phase of a comparator-based gain stage is divided into three sub-phases: a preset phase (P), a coarse charge transfer phase (E_1) and a fine charge transfer phase (E_2). In the conventional CBSC architecture of Fig. 1, a brief preset phase (P) ensures that V_X starts at the lowest available voltage, below the virtual ground condition V_{COM}. The current sources are then turned on and off sequentially, and this charges and discharges the capacitor network consisting of C_1, C_2 and C_L, which generates the ramp waveforms V_O and V_X. At the end of the coarse and fine charge transfer phases (E_1 and E_2), the voltage V_X is nearly equal to V_{COM}. The relationship between the input and the output voltages can be expressed as follows:

$$V_{X0} = V_{COM} + \left(\frac{C_1}{C_1 + C_2}\right) V_R - V_{IN}, \quad (1)$$

where V_R is $V_{COM} - V_{REF}$, V_{COM} or $V_{COM} + V_{REF}$, depending on V_{IN}, and V_{REF} is a reference voltage. This

equation shows how the time required to complete the charge transfer depends on the voltage V_{X0}, which in turn depends on the nature of the input signal. The charge transfer is self-timed, but correct operation requires it to be completed during the time allocated for that phase.

Previously [14], it showed how to enhance the speed of a conventional CBSC by switching its output node V_O to a single preset voltage, which makes the V_X start slightly below the virtual condition V_{COM}. We can verify that this condition is met by determining the voltage V_{X0} from the preset voltage. As shown in Fig. 1, V_X is raised from its initial value V_{COM} by closing switches at C_1, connecting to V_R, and at C_2, connecting to V_{PRESET}, which is the preset voltage applied at the output node instead of ground. Equation (1) can now be rewritten to express the preset voltage at the summing node V_{X0}:

$$V_{X0} = V_{COM} + \left(\frac{C_1}{C_1 + C_2}\right) V_R - V_{IN} + \left(\frac{C_2}{C_1 + C_2}\right) V_{PRESET}. \quad (2)$$

Since the conventional CBSC and single boosted preset CBSC architectures both have a fixed preset voltage, the time required to complete the charge transfer depends on the input signal and V_R which is determined by same input as we see from Eqs. (1) and (2). This motivates us to introduce multi-level input preset voltages which track the input voltage so as to improve the conversion rate. This architecture uses the same form of digital output as an SADC, which is determined by V_{IN}. This digital output is used to select the preset voltage V_{PRESET} which brings V_{X0} closer to the virtual ground condition V_{COM}.

Figure 2 shows a simplified block diagram of our scheme and its transient response. The multi-level input tracking boosted preset voltage ensures that the input node of the comparator is brought just below the virtual ground voltage during the short preset phase (P). The coarse charge transfer phase (E_1) is used to get a fast, rough estimate of the output voltage and virtual ground condition. When the comparator makes its decision, the current source (I_1) is turned off. The delay in the comparator and the high output ramp-rate cause the voltage to overshoot the correct value. In the fine charge transfer phase (E_2), a more accurate value is obtained for the output voltage. The fine-phase current (I_2) is much less than the coarse-phase current I_1, and flows in the opposite direction.

If the values of the capacitors C_1 and C_2 are equal, then the constraint that the summing node voltage V_{X0} must be less than V_{COM} results in the following range of preset voltages:

$$V_{PRESET} \leq 2V_{IN} - V_R. \quad (3)$$

Supposing that V_{COM} is located about half-way between the supply rail voltages, the valid range of input voltages is constrained by:

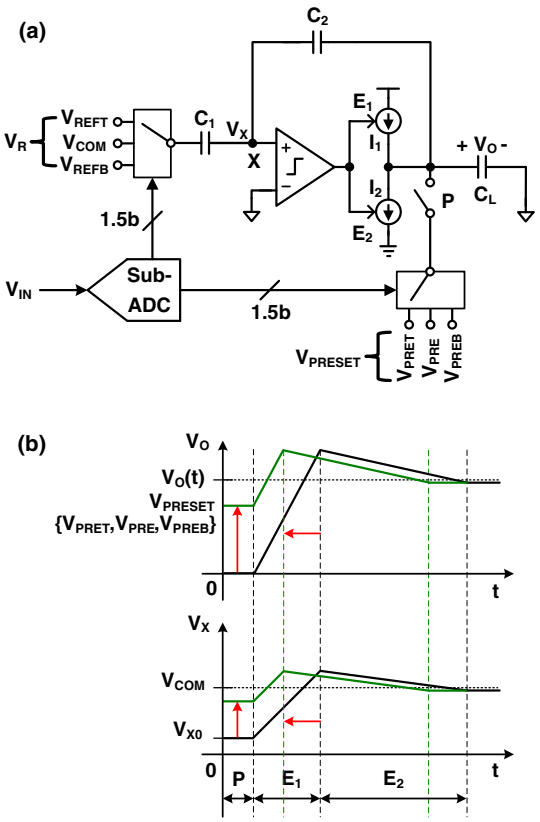

Fig. 2 **a** Charge transfer phase of a comparator-based switched-capacitor gain stage using a multi-level input tracking boosted preset voltage scheme and **b** its transient response

$$V_{COM} - V_{REF} \leq V_{IN} \leq V_{COM} + V_{REF}. \quad (4)$$

As shown in Fig. 2, due to the 1.5-bit-per stage, this range is split by input voltage, and then Eq. (4) becomes:

$$\begin{aligned} V_R &= V_{COM} - V_{REF} \text{ when } V_{IN} < V_{COM} - \frac{V_{REF}}{4} \\ V_R &= V_{COM} \text{ when } V_{COM} - \frac{V_{REF}}{4} \leq V_{IN} \leq V_{COM} + \frac{V_{REF}}{4} \\ V_R &= V_{COM} + V_{REF} \text{ when } V_{COM} + \frac{V_{REF}}{4} < V_{IN}. \end{aligned} \quad (5)$$

Substituting these inequalities into Eq. (3) yields the range of valid preset voltages in terms of V_{COM} and V_{REF}, as follows:

$$\begin{aligned} \max(V_{PRESET}) &= V_{COM} - V_{REF} \text{ when } V_{IN} < V_{COM} - \frac{V_{REF}}{4} \\ \max(V_{PRESET}) &= V_{COM} - \frac{V_{REF}}{2} \text{ when} \\ & V_{COM} - \frac{V_{REF}}{4} \leq V_{IN} \leq V_{COM} + \frac{V_{REF}}{4} \\ \max(V_{PRESET}) &= V_{COM} - \frac{V_{REF}}{2} \text{ when } V_{COM} + \frac{V_{REF}}{4} < V_{IN}. \end{aligned} \quad (6)$$

Since the switching threshold is signal-independent, no additional error is introduced except a constant offset from the comparator; but this can be expected to have negligible effect at 10-bit resolution. However, the offset of comparators in the SADC limits the performance. If we assume that the offset of comparators is $\pm V_{OS}$, then the maximum value of V_{PRESET} can be reduced as follows:

$$\begin{aligned}
&\max(V_{PRESET}) = V_{COM} - V_{REF} \text{ when } V_{IN} < V_{COM} - \frac{V_{REF}}{4} \\
&\max(V_{PRESET}) = V_{COM} - \frac{V_{REF}}{2} - 2V_{OS} \text{ when} \\
&\quad V_{COM} - \frac{V_{REF}}{4} \le V_{IN} \le V_{COM} + \frac{V_{REF}}{4} \\
&\max(V_{PRESET}) = V_{COM} - \frac{V_{REF}}{2} - 2V_{OS} \text{ when} \\
&\quad V_{COM} + \frac{V_{REF}}{4} < V_{IN}. \qquad (7)
\end{aligned}$$

From Eq. (7), it is observed that the time required to obtain a rough estimate of the output and virtual ground can be extended, compared to the ideal case where there is zero offset in the comparators. Therefore, to maximize the effectiveness of the proposed scheme, a high-precision comparator with low offset [19] could be considered as a threshold detection comparator.

The time reduction by this scheme can be calculated using Kirchhoff's current law assuming that the current source of the coarse charge transfer phase (E_1) has a large charging current and a finite resistance.

$$I_1 = C_E \frac{dV_O(t)}{dt} + \frac{V_O(t)}{R_0}, \qquad (8)$$

where C_E is the capacitance at the output node, V_O is the output voltage, I_1 is the current from the current source of the coarse charge transfer phase (E_1), and R_0 is the output resistance of the current source. Solving this equation for the initial condition $V_O(0) = V_{PRESET}$ yields

$$V_0(t) = I_1 R_0 \left(1 - e^{-\frac{t}{R_0 C_E}}\right) + V_{PRESET} e^{-\frac{t}{R_0 C_E}}. \qquad (9)$$

The maximum charging time is determined by Eq. (4) and the relationship between V_{IN} and V_O, as follows:

$$t_{\max} = R_0 C_E \ln\left(\frac{I_1 R_0 - V_{PRESET}}{I_1 R_0 - V_O}\right). \qquad (10)$$

As a result, these equations show how a multi-level boosted preset voltage reduces the time and enhances operation speed.

Figure 3 and Table 1 compare results from the proposed and previous schemes, operating at the point at which conversion times are longest. The multi-level input tracking scheme has the lowest dropout, indicating a reduction in conversion time; but there is no increase in power consumption.

3 Cyclic analog-to-digital converter

3.1 Architecture

As shown in Fig. 4(a), the circuit consists of two 1.5-bit MDACs, each paired with a SADC ($MDAC_1$ and $SDAC_1$, $MDAC_2$ and $SDAC_2$), digital correction logic, and a clock generator. In a cyclic ADC, the SHA samples either the input signal of the ADC or the output of the MDAC. However, in our design, the sampling in the switched-capacitor circuit of $MDAC_1$ performs an equivalent function without affecting the conversion rate, and therefore there is no need for a separate SHA, which would only generate extra noise. The second MDAC and SADC pair doubles the conversion speed; but there is still a reduction in chip area and power consumption because there is no SHA. This architecture uses redundancy to eliminate the offset errors of the comparators in the SADC and relaxes the requirements of the comparators.

Opamps are generally the most power and area-consuming analog blocks in an MDAC stage. However, as the scale of CMOS processes continues to shrink, it has become difficult to improve or even maintain the accuracy of ADCs, because it relies on a high-gain opamps. Comparator-based designs are easier to scale because a comparator and its associated current sources have less stringent requirements than an opamp. The CBSC technique allows us to use a single comparator and its current sources together with a feedback capacitor, which are then shared between the two MDACs alternately, as shown in Fig. 4(b). Sharing further reduces power consumption and chip area. In addition, the proposed multi-level input tracking boosted preset scheme can achieve a better conversion time than any other previous architecture, without additional power consumption.

3.2 Circuit implementation

Figure 5 is a simplified representation of the function of $MDAC_1$ and $MDAC_2$ in our cyclic ADC. Although we use a fully differential architecture, these diagrams show single-ended circuits and omit the two SADCs for simplicity. MDAC stages are basically switched-capacitor circuits, which use two non-overlapping clocks to produce a sampling and a comparison phase. During the sampling phase, the input voltage is sampled by the two capacitors and the SADC. During the comparison phase, one of the capacitors is used as a feedback capacitor of the CBSC and the other capacitor is connected to one of the three voltages depending on the digital output from SADC. Also, the preset voltage V_{PRESET} is selected by the same digital output from the SADC so that it follows Eq. (7).

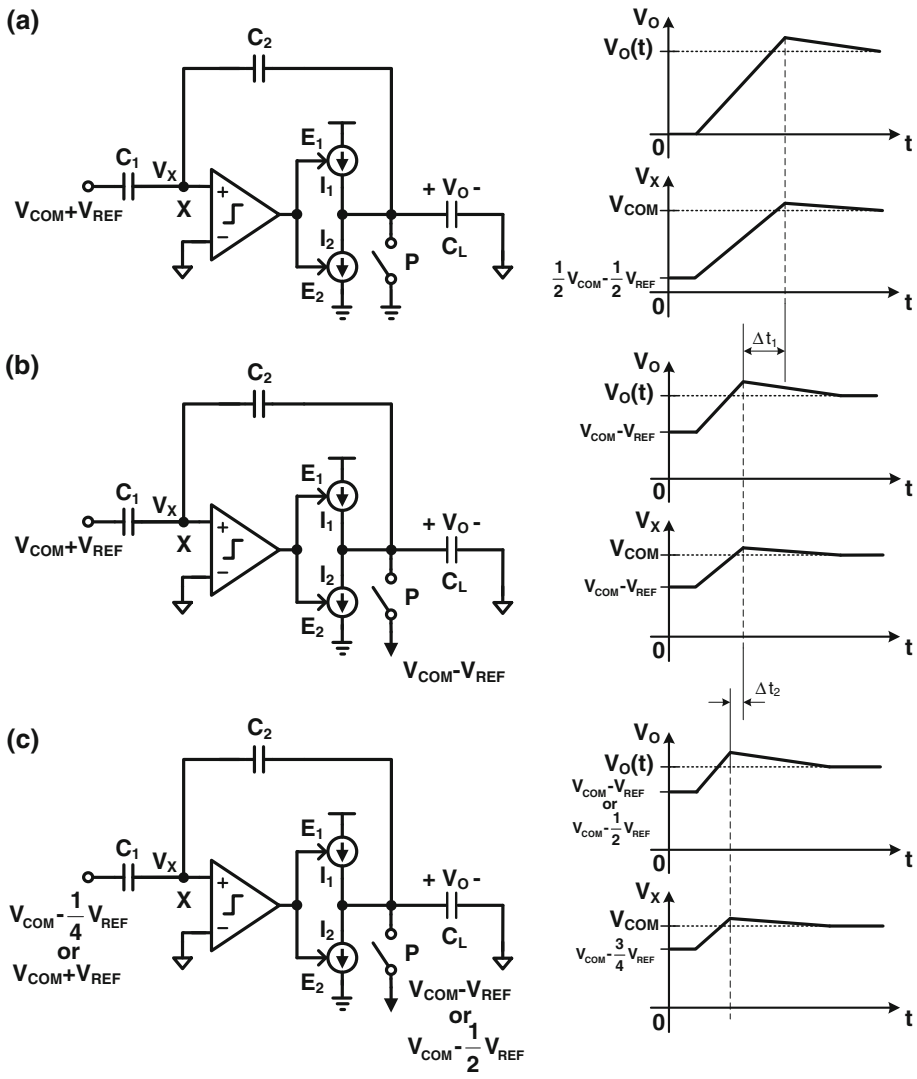

Fig. 3 Comparison of conversion times of different schemes at the point at which conversion times are longest ($\Delta t_1 > \Delta t_2 > 0$): **a** conventional scheme ($V_{PRESET} = 0$) and its transient response, **b** single boosted preset scheme ($V_{PRESET} = V_{COM} - V_{REF}$) and its transient response, and **c** multi-level input tracking boosted preset scheme ($V_{PRESET} = V_{COM} - V_{REF}$ or $V_{COM}^{-1}/2V_{REF}$) and its transient response

Table 1 Comparison of three design schemes in terms of max(v_{preset}) and min(v_{x0})

	Conventional	Single boosted Preset	Multi-level input tracking boosted preset
V_{PRESET}	Fixed	Fixed	Varied
max(V_{PRESET})	0	$V_{COM} - V_{REF}$	$V_{COM} - V_{REF}$ or $V_{COM} - \frac{1}{2}V_{REF}$
min(V_{X0})	$\frac{1}{2}V_{COM} - \frac{1}{2}V_{REF}$	$V_{COM} - V_{REF}$	$V_{COM} - \frac{3}{4}V_{REF}$

During the first sampling phase ϕ_s, the input voltage is sampled by C_1 and C_2, and determined by $SADC_1$ while the comparator is reset. During subsequent odd phase ϕ_1, the value produced by $SADC_1$ is connected to C_1. $MDAC_2$ samples the output of $MDAC_1$, and the output voltage is sampled by $SADC_2$. During each even phase ϕ_2, the value produced by $SADC_2$ is connected to C_3, $MDAC_1$ samples the output of $MDAC_2$, and the output voltage is sampled by $SADC_1$. The use of two SADCs allows each stage to use a single clock phase, by means of a clocking scheme with a half clock signal. At the end of each odd and even phase, it can be observed that the same residue voltage is present on both the load and feedback capacitors. This scheme requires the voltage at the virtual ground node to be the same as V_{COM}; and this requirement is met, because the input to the comparator can be expected to be close to V_{COM}. Since the information we want is available on the feedback capacitor, the load capacitor can be eliminated altogether and the feedback capacitor act as the load capacitor of the next stage. The feedback capacitor is split into two halves and these two halves become the input and feedback capacitors of the next stage, thereby obviating the need for a dedicated set of load capacitors and hence saving power. This capacitor sharing technique pairs well with the comparator sharing technique.

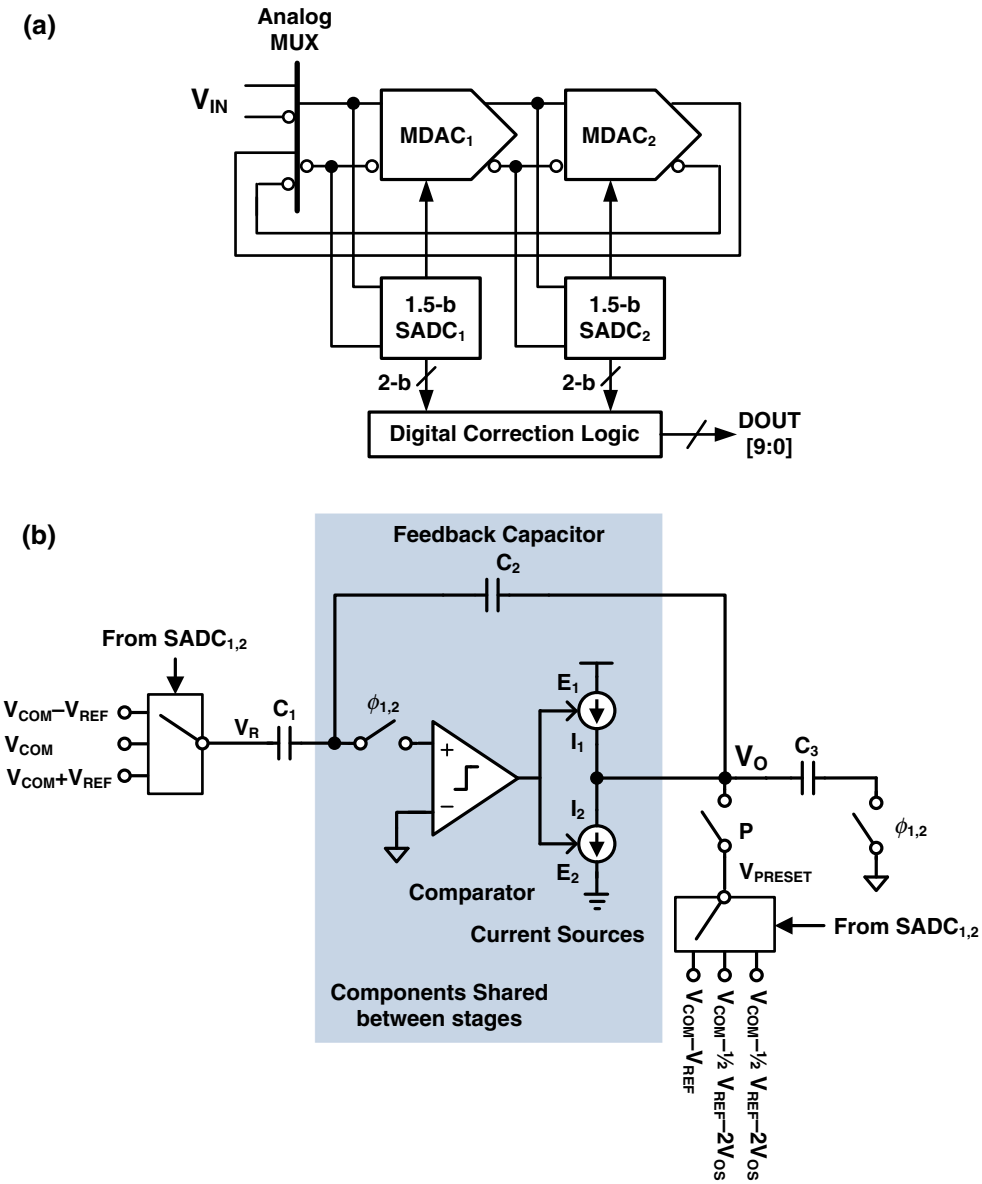

Fig. 4 The proposed cyclic ADC: **a** architecture and **b** MDAC stage

3.3 Threshold-detection comparator

The comparator, which is a critical part of the CBSC circuit, detects the virtual ground voltage accurately. To achieve a low error, the comparator needs to have a high gain because it must change its output as soon as its input crosses the virtual ground voltage. The gain of a comparator can be increased by cascading gain stages. This can compromise the stability of an opamp-based switched-capacitor circuit, because the opamp is configured as a closed loop. But the comparator in a CBSC circuit is an open loop, and so a cascading configuration poses no stability problem. Figure 6 shows a schematic diagram of our high-gain comparator, which consists of three cascaded preamplifiers. The outputs of the first stage of the comparator are connected by two MOS diodes to reduce the conversion time, and the outputs of the final stage are buffered with inverters to drive logic circuits which control the current sources.

3.4 Sub-ADC comparator

The SADC consists of two fully differential comparators. In the 1.5-bit stage architecture, the thresholds of the SADC are $V_{COM} + V_{REF}/4$ and $V_{COM} - V_{REF}/4$, and the input range of the ADC is $V_{COM} - V_{REF}$ to $V_{COM} + V_{REF}$. The comparator operates on two-phase non-overlapping clocks and consists of an input amplifier and a latched comparator with regeneration latches, as shown in Fig. 7. The comparator almost nullifies the load seen by

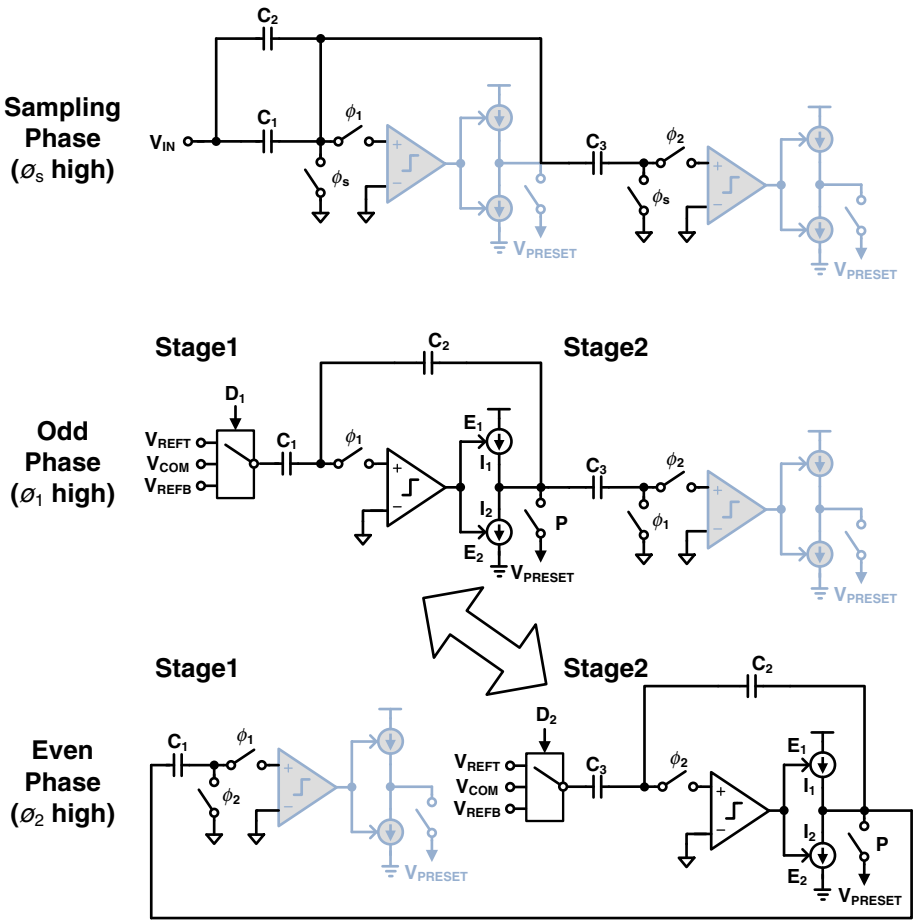

Fig. 5 Simplified circuit showing $MDAC_1$ and $MDAC_2$ stages during the odd and even phases of sampling

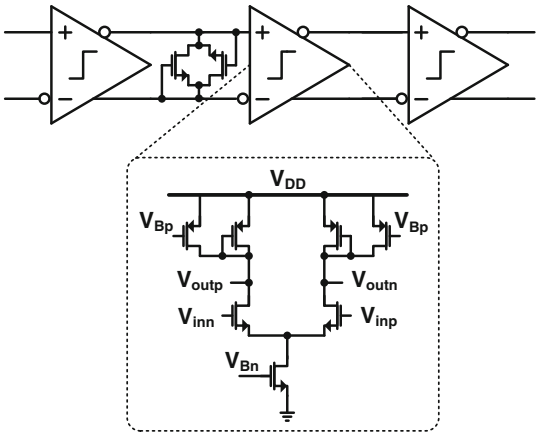

Fig. 6 Schematic diagram of the threshold-detection comparator

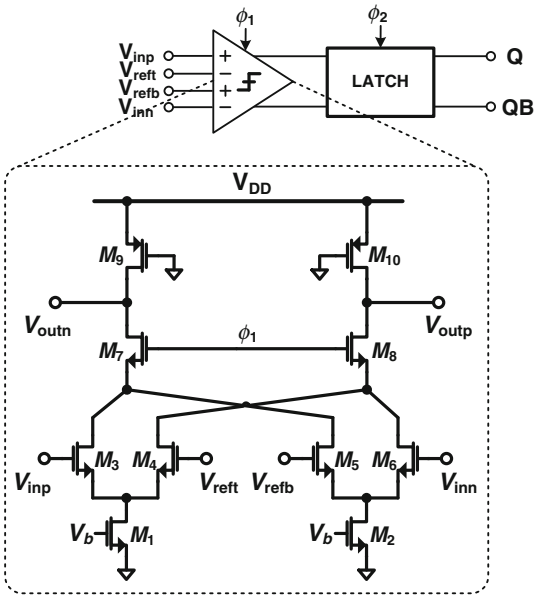

Fig. 7 Fully differential comparator inside the sub-ADC

references. This helps in V_{REFT} and V_{REFB} being reliably produced and used from a resistor ladder using $\pm V_{REF}$ thereby saving power. The input amplifier is just two simple NMOS differential pairs with current sources, which not only amplifies the input signal but also suppresses the kick-back noise from the regeneration latches. The NMOS switches, M_7 and M_8 will turn off the input differential pair during regeneration time to save power consumption. Furthermore, it can also help to reduce noise from the regeneration latches.

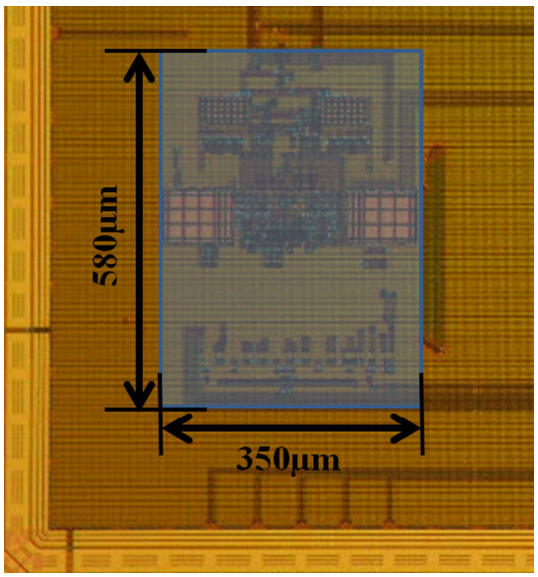

Fig. 8 Microphotograph of the prototype die

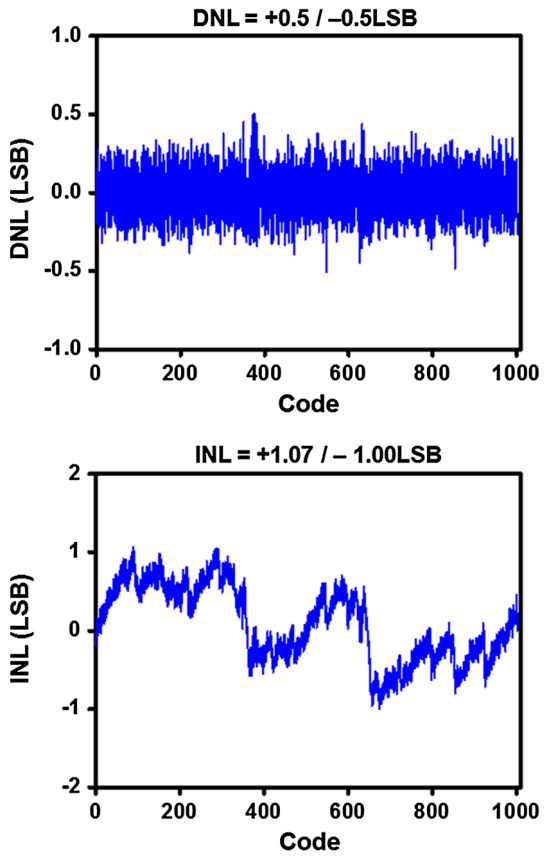

Fig. 9 Measured DNL and INL

4 Measurement results

A cyclic ADC using our multi-level input tracking boosted preset was fabricated in a 0.18 μm CMOS process with MIM capacitors. Figure 8 shows a microphotograph of the die, which has an active area of 0.09 mm^2. In order to demonstrate its effectiveness, a conventional CBSC and a single boosted preset voltage scheme were also implemented using the same design.

Figure 9 depicts the differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics of our ADC, obtained from code-density measurements. The DNL was +0.5/−0.5 LSB and the INL was +1.07/−1.00 LSB.

The measured fast Fourier transform (FFT) spectrum is shown in Fig. 10. The sinusoidal input frequency (F_{in}) was 1.201 MHz and the sampling-rate (F_S) was 2.8 MHz respectively. The signal-to-noise and distortion ratio (SNDR) was 53.77 dB and the spurious-free dynamic range (SFDR) was 61.88 dB.

Figure 11 shows the relationship between the measured SNDR and SFDR and the F_{in}. At a sampling rate of 2.8 MHz, with a 0.101 MHz sinusoidal input to the ADC,

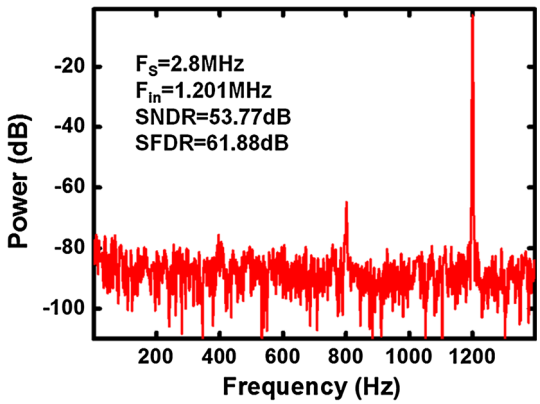

Fig. 10 FFT plot of measured data with multi-level input tracking boosted preset voltage at a sampling rate of 2.8 MS/s (F_{in} = 1.201 MHz, SNDR = 53.77 dB, and SFDR = 61.88 dB)

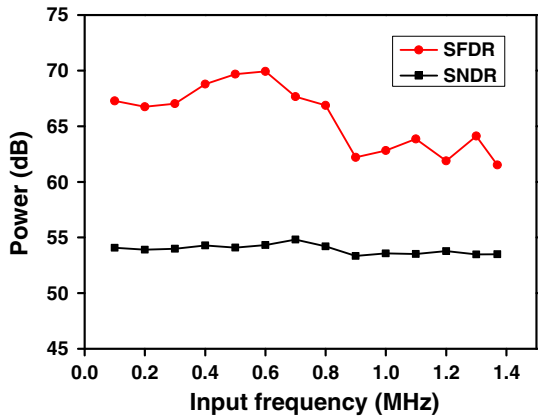

Fig. 11 Measured SNDR and SFDR versus input frequency at a sampling rate of 2.8 MS/s

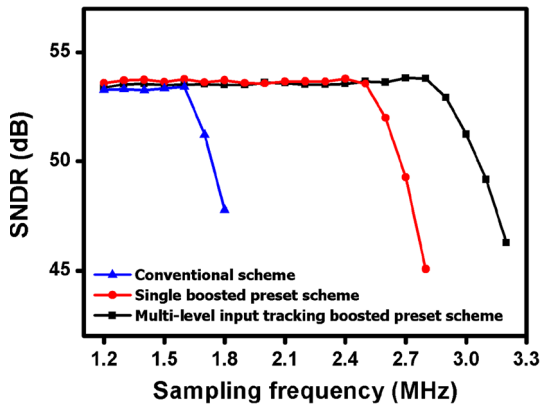

Fig. 12 Comparison of SNDR versus sampling frequency according to preset schemes

Table 2 Performance summary

Technology	0.18 μm CMOS process
Resolution	10 bit
Conversion rate	2.8 MS/s
DNL	+0.5/−0.5 LSB
INL	+1.07/−1.00 LSB
SNDR	53.69 dB (F_{in} = 1.37 MHz)
SFDR	61.53 dB (F_{in} = 1.37 MHz)
Power	0.73 mW
Active area	0.09 mm^2

the measured SNDR and SFDR were 54.08 and 67.28 dB respectively. Near the Nyquist-rate frequency, the SNDR and SFDR were 53.69 and 61.53 dB respectively, and the effective number of bits (ENOB) was 8.63. Although parasitic caused by switches degraded performance, it was possible to compare the performance between schemes, because they were all implemented using the same design.

In order to further demonstrate the effectiveness of the proposed scheme, we had experiments on comparison of three architectures: conventional CBSC, single boosted preset CBSC, and multi-level input tracking boosted preset CBSC design. The single boosted preset CBSC design is the same as the previous design [14]. Figure 11 shows measurements of SNDR plotted against the sampling frequency according to preset condition, with the F_{in} fixed at a 0.101 MHz sinusoidal input to each ADC. The preset voltages corresponded to the minimum and maximum values obtained from the appropriate equations for each scheme. Without a boosted preset voltage, no performance degradation was observed up to a maximum conversion rate of 1.6 MS/s. The single boosted preset scheme raised this sampling rate above 2.5 MS/s. If our multi-level input tracking boosted preset voltage scheme was applied, the sampling frequency increased more than the previous schemes implemented on the same die. That is, the sampling frequency enhancements of 75 and 12 % can be obtained by our scheme. These results also indicate that our scheme enhances the conversion rate effectively without using additional power (Fig. 12).

Table 2 summarizes the performance of our cyclic ADC. Operating at a 2.8 MHz sampling rate, with a $1V_{P-P}$ range, it consumes 0.73 mW at 0.18 μm CMOS technology.

Table 3 shows the comparison of the proposed ADC with those of previous works with more than 10-bit resolutions and process technologies [14], [15], [20], and [21]. The design of ADC [14] is same as the present work with a single boosted preset scheme. For fairness, [14] has been re-implemented with the same active area of this work on the same die for an apple-to-apple comparison. As compared with the previous works, our ADC achieves the lowest FOM as listed in Table 3.

5 Conclusion

We have presented a comparator-based cyclic ADC with multi-level input tracking boosted preset voltage. The use of a CBSC circuit saves a significant amount of power, compared to conventional opamp-based designs. Additionally, a scheme that boosts the preset voltage according to the input voltage to enhance the conversion rate without using any extra power has been implemented and

Table 3 Comparison of cyclic ADCs with more than 10b resolutions and process technologies

	[20]	[21]	[15]	[14][a]	This work[b]
Resolution	12b	10b	11b	10b	10b
Technology	130 nm	180 nm	130 nm	180 nm	180 nm
Conversion rate	0.04 MHz	14 MHz	10 MHz	2.5 MHz	2.8 MHz
SNDR	63.3 dB	52.4 dB	56 dB	53.56 dB	53.69 dB
Supply voltage	1.8 V	3.3 V	3 V	1.8 V	1.8 V
Power consumption	0.07 mW	21.6 mW	15 mW	0.72 mW	0.73 mW
Active area	0.04 mm^2	0.38 mm^2	0.24 mm^2	0.09 mm^2	0.09 mm^2
FOM	1,465 fJ/Conv.	4,530 fJ/Conv.	2,910 fJ/Conv.	739 fJ/Conv.	658 fJ/Conv.

[a] Has been re-implemented for comparing the performance with that of this work

[b] On the same die

evaluated. This approach is more suitable for scaled technologies than equivalent opamp-based circuits because it is based on the comparator-based architecture. Other aspects of design, we employed several techniques such as the use of two MDAC stages without an SHA and a comparator, current sources and a feedback capacitor sharing between stages, which make further savings of power and area.

Our prototype was fabricated in 0.18 μm CMOS, has an active area of 0.09 mm^2, and consumes 0.73 mW. It is shown that when the input is near the Nyquist-rate, the SNDR is 53.69 dB and the SFDR is 61.53 dB, at 2.8 MS/s.

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