A 2.1Gbps 12-Channel Transmitter with Phase Emphasis Embedded Serializer for UHD Intra-panel Interface

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***Abstract*— A 2.1Gbps 12-channel transmitter with phase emphasis embedded serializer for an intra-panel interface is presented. Phase emphasis is introduced into the final 2:1 stage of a 20:1 serializer to reduce the data-dependent jitter without increasing IO capacitance, by making the transition timing depend on previous data. This is combined with LVDS channel drivers which control the common-mode voltage and swing of the output signal over a wide range to match the condition of each channel. Using both phase and amplitude emphasis, the transmitter can compensate for channel losses exceeding 10dB, and eye jitter is reduced by 38%: phase emphasis is responsible for about half of this reduction. Fabricated in 28nm CMOS, the transmitter occupies 1.35mm^2. The proposed transmitter is verified with 55-inch UHD (3840x2160) resolution TFT-LCD intra-panel interface.**

Keywords*— transmitter; phase emphasis; data-dependent-jitter; UHD resolution; intra-panel interface

I. INTRODUCTION

As the Thin-film transistor liquid crystal displays (TFT-LCDs) have become popular and large-screen TVs using the high resolution of full-HD (FHD) have become very successful in the market, the trend of the TV market is moving toward a higher resolution called ultra-HD (UHD) resolution. Since UHD TV has to support at least 3840 x 2160 resolution, 10-bit large color depth, and 120Hz frame rate, the data interface is a bottleneck in such a high-end LCD system.

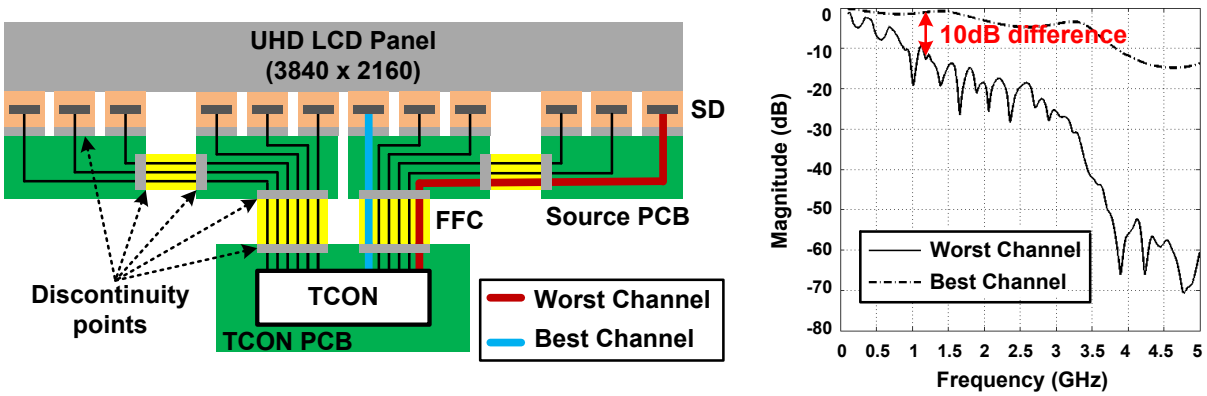
Fig. 1.(a) shows the intra-panel interface between the timing controller (TCON) and the source driver (SD) of a UHD TV. The channels consist of long PCBs and flexible flat cables (FFCs), and their lengths are not uniform. This gives the designers two challenges in achieving signal integrity: First, since signal loss can vary between the worst channel and the best channel by more than 10dB at frequency over 1.05GHz, as shown in Fig. 1.(b), the characteristics of the output signal such as the common-mode level, swing, and emphasis levels, must be independently adjustable. Second, an equalization scheme is needed to compensate for the degradation in signal integrity by the worst channel with at least a 10 dB loss and many discontinuities.

The second problem is more critical in a UHD intra-panel interface. A feed-forward equalizer (FFE) which is used as an amplitude emphasis scheme [1][2] is commonly used in a transmitter, and this is inefficient to compensate for an insertion loss of more than 10dB. Increasing the amplitude emphasis level severely causes problems such as a reduction in the signal swing and data distortion due to the fluctuation of the common-mode level at signal transition. This issue has motivated the development of ways of introducing variable tap spacing to the FFE [3] and applying phase emphasis to the quadrature-rate output driver [4] with the aim of attaining the necessary compensation despite low amplitude emphasis. These schemes reduce the amount of total jitter for which the amplitude emphasis has to compensate by decreasing the data-dependent jitter (DDJ), which is a major jitter component. However, a lot of current is consumed by the CML delay cell required to control variable tap spacing. With the latter scheme, increasing the number of input MOS to the output driver makes IO capacitance increase, which limits bandwidth. Also, the skew difference between the quadrature-clocks tends to degrade the signal quality with this scheme.

We address these problems by introducing a 12-channel transmitter with both phase emphasis and amplitude emphasis. Phase emphasis is implemented by modifying the 2:1 serializer, so there is no need to make the output driver more complicated, or increase its IO capacitance. In addition, the serializer can easily delay data through its synchronous logic to detect data transitions, so that is better able to deal with timing constraints and reduce current consumption. In addition, this transmitter is able to control the characteristics of the output signal over a sufficiently wide to maintain signal integrity across different channel environments.

II. TRANSMITTER ARCHITECTURE

As shown in Fig. 2, our 12-channel transmitter consists of 12 data channels, a SSCG_PLL, a band gap reference (BGR). The TCON link delivers 20-bit parallel data and three kinds of control signals for controlling the output signal of each channel. In order to reduce the skew in the output signal between adjacent channels, channels are configured in pairs, sharing bias circuits such as the resistor DAC (RDAC) and the bias generator.



(a) (b)

Fig. 1. (a) The intra-panel interface configuration, and (b) the insertion loss (S_{13}) of worst/best channel.

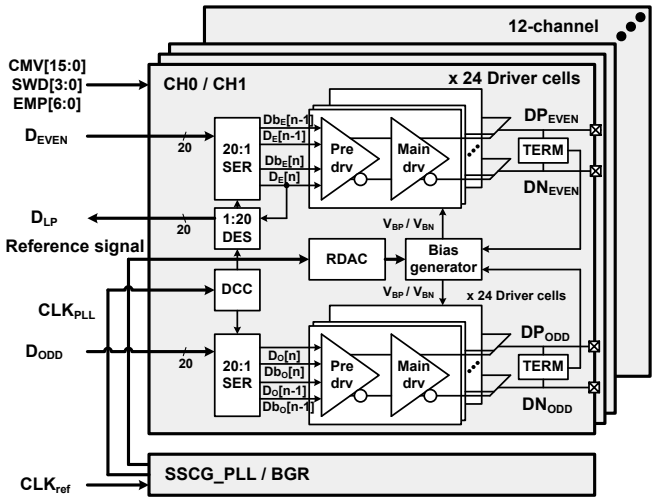


Fig. 2. Overall architecture of the proposed 12 channel transmitter.

A 20:1 serializer on each channel converts 20-bit parallel 1-bit serial data. Since the transmitter uses a low-voltage differential-signaling (LVDS) driver with 1-tap amplitude emphasis, the serializer outputs the current bit (D[n], Db[n]) and the previous bit (D[n-1], Db[n-1]). The driver is composed of 24 identical cells, each of which consists of a main driver sub-cell and pre-driver sub-cells, and each cell outputs the data by selecting either the current bit or the previous bit, depending on the emphasis command (EMP[7:0]). There is also a loopback path through the 1:20 deserializer to check the result of serialization.

III. Circuit Implementation

A. LVDS driver with wide tuning range

The driver that controls the common-mode voltage (V_{CM}) and swing (V_{SW}) is shown in Fig. 3. The driver receives the register values (CMV[15:0], SWD[3:0]) through the TCON link. To control the common mode voltage, the differential output of driver is divided by resistors, and the central value is an input to the common-mode feedback (CMFB) control-loop. The resistor DAC generates 16 reference voltages in a range

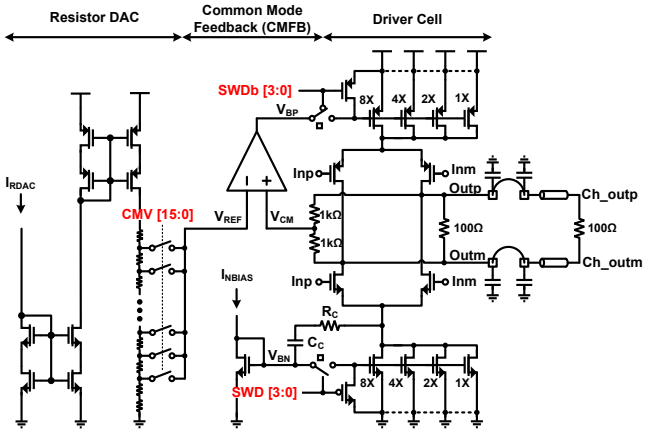


Fig. 3. LVDS driver with wide common mode and swing level controllability

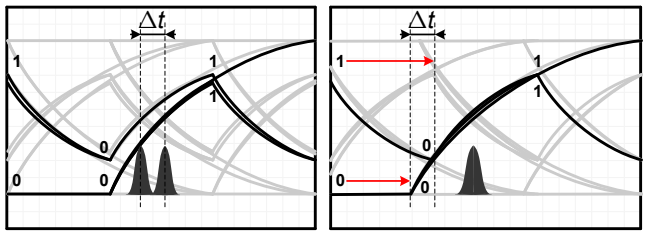


Fig. 4. (a) Eye diagram and jitter histogram at receiver front-end with same sampling timing, and (b) those with different sampling timing for phase emphasis

from 300mV to 600mV, selects the target voltage (V_{REF}) determined by CMV[15:0], and sends it to the CMFB control-loop.

The swing control register SWD[3:0] controls the number of NMOS cells which are turned on to mirror the reference current. In order to reduce the effect of swing control on the common-mode voltage, the same number of PMOS and NMOS cells are always turned on. This allows the driver to provide an output swing range of 600mV while maintaining an acceptable common-mode voltage.

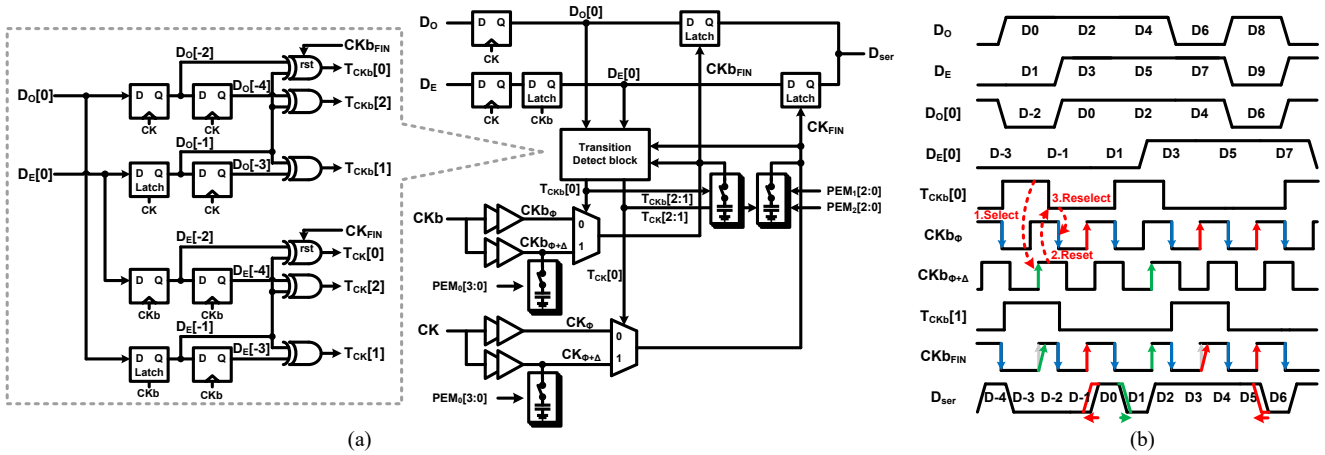


Fig. 5. (a) The proposed 2:1 serializer with phase emphasis technique and the transition detect block, and (b) the timing diagram of proposed 2:1 serializer.

B. *Phase emphasis embedded 20:1 serializer*

The 20:1 serializer consists of a 5:1 serializer cascaded with two 2:1 serializers. The 5:1 serializer multiplexes 5-bit input data based on a selection signal, and the 2:1 serializer has 5 parallel latches. The phase emphasis scheme is applied to the second 2:1 serializer, that sends its output to the driver.

Without phase emphasis, the eye opening of the received signal is narrowed by jitter, as shown in Fig. 4.(a). we can analyze this issue using the total jitter probability distribution function (PDF) which is the convolution of the PDF of random jitter (RJ) and deterministic jitter (DJ) [5]. Unlike RJ, which is modeled as a Gaussian distribution, the distribution of DJ can be modeled as two impulse functions [6], and then characterized by the distance between the impulses. Data-dependent jitter which is a kind of DJ can be modeled as two impulse functions. Also, since DDJ is the inter-symbol interference (ISI) applied to the next bit by the long tail of the single bit response, its value depends on previous data. Therefore, the phase emphasis scheme is designed so that the starting time of the transmission signal varies with the previous data, as shown in Fig. 4.(b). When the data is equalized by phase emphasis, the rising curves of all data pattern overlap at the decision threshold voltage of the receiver.

The second 2:1 serializer is modified, as shown in Fig. 5.(a), to provide phase emphasis by varying the phase of the sampling clock depending on whether there is a transition between the current bit (D[0]) and previous bits (D[-2], D[-3], D[-4]). The output signal of the transition detect block (T_{CKb}[2:0]) adjusts the delay of the sampling clock using three banks of capacitors.

As shown in Fig. 5.(b), there are two ways to adjust the delay depending on the required resolution. The first tap, which has a large phase resolution (up to 40ps), is implemented by selecting CKb_{Φ} or the delayed clock $CKb_{\Phi+\Delta}$; but the 2nd and 3rd taps, which produce much smaller phase resolutions (up to 16ps), are implemented by changing the value of the capacitor bank at the sampling clock node. If all three taps were implemented by switching signals, there would be a need for eight multiphase clocks, leading to an overcomplicated design. Conversely, if all three taps were implemented by changing the load of sampling clock node, meta-stability in driving data might occur because of the large load on the sampling clock node. Our approach also synchronizes the falling edge of the sampling clock to the falling edge of the early-phase clock to prevent both paths from driving the output while the sampling clocks overlap.

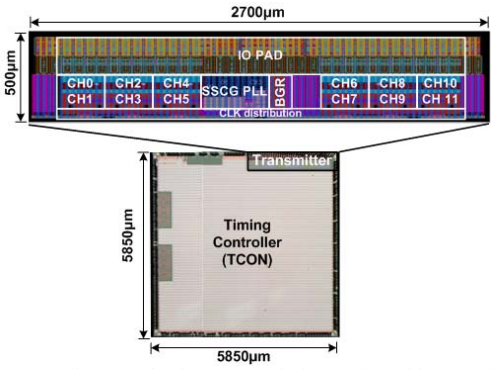


Fig. 6. The microphotograph of TCON including enlarged layout of 12-channel transmitter.

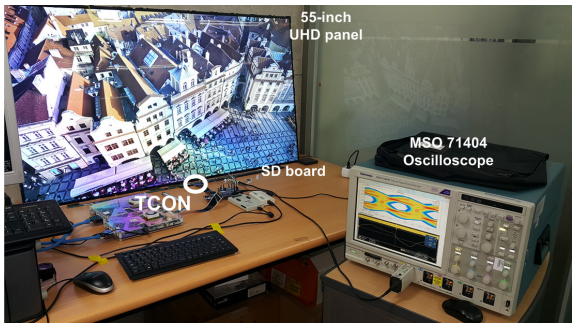


Fig. 7. 55-inch UHD TFT-LCD panel prototype to verify the proposed TCON transmitter of intra-panel interface.

IV. Experimental Results

A timing controller, including our 12-channel transmitter, was implemented in a 28nm CMOS process, and its microphotograph is shown in Fig. 6. The total area of the transmitter is 1.35mm^2. Fig. 7 shows a 55-inch UHD

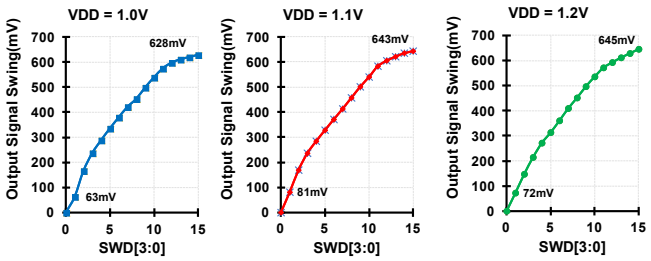


Fig. 8. Measured single-ended output swing level with supply variation .

resolution TFT-LCD panel prototype system with an intra-panel interface that supports a 10-bit color depth and a frame-rate of 120Hz. The measurements shown in Fig. 8 indicates that the swing of the transmitted signal is widely controlled up to 628mV regardless of the supply voltage variation.

Fig. 9 shows the measured eye diagrams with and without a connected channel while adjusting only the 1st tap coefficient of the phase emphasis. When there is no channel, the jitter increases with the coefficient, as expected; but with a channel the jitter is reduced by 22% from 316ps to 247ps. Fig. 10 shows how much the eye opening is improved by phase and amplitude emphasis. Without emphasis, the jitter is 339ps but it decreases by 38% to 211ps when equalized by emphasis.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS DESIGNS

	This work	[1]	[2]	[4]
Technology	28nm	65nm	130nm	90nm
Supply	1.0	1.2	1.2	1.0
Data rate [Gb/s]	2.1	20	1.62	6
Cable loss [dB]	12	12.78	12.3	10
Equalization type	FFE[a] PE[b]	FFE[a]	FFE[a]	PE[b]
Swing level (V_{pk-pk}) [V]	1.2	0.3	0.2	0.6
Transmitter power [mW]	12.7	58.8	32.4	24
FoM[c] [pJ/bit·V]	5.05	9.8	100	6.67

[a] FFE =feed forward equalizer (amplitude emphasis)

[b] PE = phase emphasis

[c] Figure of merit (FoM) = Transmitter Power / (Data rate x Swing level)

V. CONCLUSION

We have presented a 2.1Gbps 12-channel transmitter for a UHD intra-panel interface, fabricated in 28nm CMOS technology. Common-mode, swing, and emphasis levels can be controlled independently so as to match different channel conditions. Both phase and with amplitude emphasis are used to compensate for channel losses of 12dB. The performance of this proposed transmitter is summarized and compared with previous designs in Table I. When a 2.1Gbps signal with PRBS of 2^7-1 passes through a PCB trace with a 12dB loss, the measured eye jitter is reduced by 38% by applying both

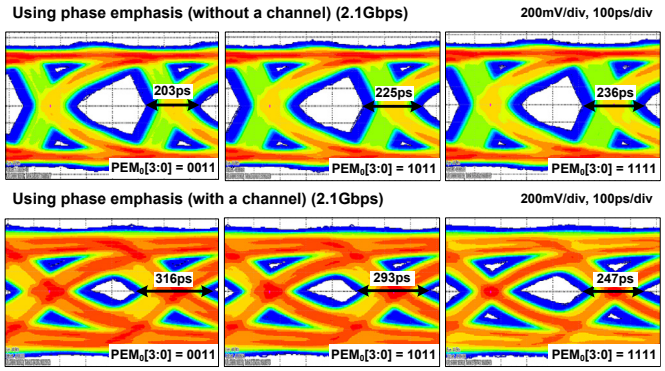


Fig. 9. Measured 2.1Gbps eye diagrams using only phase emphasis.

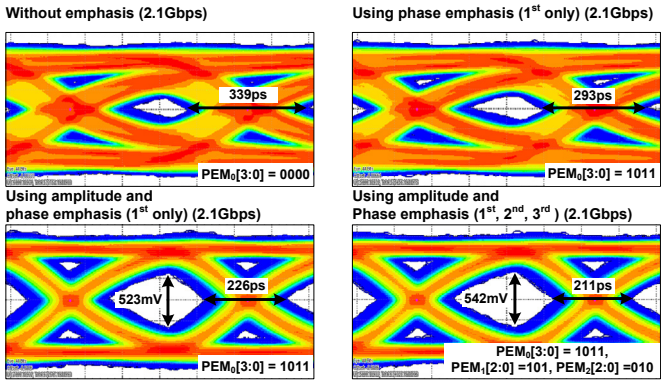


Fig. 10. Measured 2.1Gbps eye diagrams at the channel output with different emphasis condition.

emphasis techniques. The transmitter consumes 12.7mW at 2.1Gb/s, giving a FoM of 5.05pJ/bit·V.

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