A 19-bit Range and 4.5-ps Resolution Fully-Synthesizable Time-to-Digital Converter with Quad-Edge Offset Cancellation

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***Abstract*—This presents a fully-synthesizable cyclic Vernier time-to-digital converter (TDC) which cancels the offsets by a quad-edge offset cancellation (QOC) scheme. The system delays its internal clocks and uses the clock offsets to compensate for many types of offsets altogether, which includes the wiring mismatches, the duty cycle skews, and the long-term jitters of the clocks. During calibration, the QOC-TDC measures the offsets of the clock paths. The measured offsets are then canceled in the normal mode. An additional scheme of coarse-fine boundary synchronization further enhances the output monotonicity. Consisting of only standard library cells offering fully-automated implementation, the QOC-TDC achieves a 19-bit range, a 4.5-ps resolution, and the throughput of 22MS/s, while drawing 3.4mW from a 1.0V supply, as shown by the post-layout simulations in 28nm CMOS.**

Keywords— offset cancellation, synthesizable, standard library cell, cyclic Vernier, time-to-digital converter.

I. Introduction

Time-to-digital converters (TDCs) with high resolution have been popular in recent mixed-signal circuits for many applications, including test instrumentation and phase-locked loops (PLLs) [1-6]. However, conventional delay-line-based TDCs suffer from limited resolution due to physical delay constraints [2,7,8].

A successive approximation [9] offers better precision but sacrifices power and area [1]. Timing amplification in [10,11] relaxes the delay requirement, but it amplifies the noise [1]. Other analog works including delay locked loops [12], gated ring oscillators [13], interpolators [14], Vernier delay-lines [15], and delay-less TDCs [16] also suffer from either mismatches or limited throughput [1,2,7,8].

Hence, digital-based designs have been the popular replacement of analog designs due to many advantages including area, power, cost, robustness [2,17,18], and speed [8]. The digital design also benefits portability and scalability from the scale-down of CMOS processes [17-20]. In addition, fully-synthesizable designs based on the standard library cells (SLCs) further offer fully-automated implementation, so the design and validation procedures can be simplified [4,18]. However, they still suffer from the mismatches.

Synthesizable stochastic TDCs [1,7] have been proposed to alleviate the mismatch issues. However, they are limited in the measurement range [21] since the range is proportional to the total number of delay stages. Besides, they require polyphase signaling [22] which costs area. Work in [17] has introduced a synthesizable cyclic Vernier TDC, and a more portable design only using the SLCs is proposed in [18]. Recent work in [22] has proposed another synthesizable

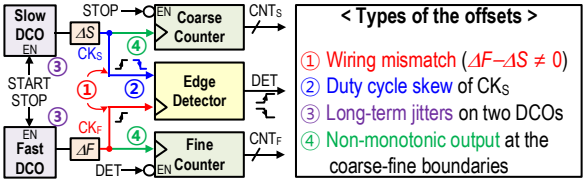

Fig. 1. Block diagram of a fully-synthesizable cyclic Vernier TDC and the causes of offsets.

design with calibration and throughput-enhancing features. However, [17] and [22] are based on soft-edged flip flops [23] that require custom layouts to minimize the offset caused by the setup time. In addition, a dual-edge detection scheme used in [17], [18], and [22] suffers from the mismatches by duty cycle skews of internal clocks. Moreover, the asynchronous clocking of the two counters in the cyclic Vernier TDC may result in non-monotonic outputs at the coarse-fine boundaries.

To address the issues outlined above, we present a SLC-only and fully-synthesizable TDC with a quad-edge offset cancellation (QOC) scheme. In this work, we apply additional offsets to the clock paths to avoid the output glitches of the edge detector due to the meta-stability at the beginning of calibration. The measured offsets include the wiring mismatches, the duty cycle skews, and the effect of finite setup-and-hold time. The QOC-TDC measures such offsets during calibration and cancels the offsets in the normal cyclic Vernier operation, so the offsets at the outputs are well reduced. An embedded DCO controller finely adjusts the DCOs so that the long-term jitters are limited, even in the case of long-range inputs. The QOC-TDC also enhances the output monotonicity by synchronizing the counter output values at the coarse-fine boundaries.

II. The Architecture of the Proposed Work

A conventional synthesizable cyclic Vernier TDC may suffer from the degradation of output accuracy due to several offsets. The causes of the offsets include: the wiring mismatch between CK_F and CK_S, the duty cycle skew of CK_S, the long-term jitters in CK_F and CK_S, and the non-linearity at the coarse-fine boundaries, as shown in Fig. 1.

The architecture of the proposed QOC-TDC is shown in Fig. 2. A DCO controller block limits the long-term jitters of the DCOs. It is comprised of a flip-flop PD for phase detection, a DCO control block CTRL, a divider /N, and a tunable oscillator DCO_P. The CTRL generates a control code N_{CTRL} and updates N_{CTRL} at every cycle of a reference clock CK_R. Therefore, N_{CTRL} limits the jitter accumulation. The DCO controller performs as a narrow-bandwidth PLL with a

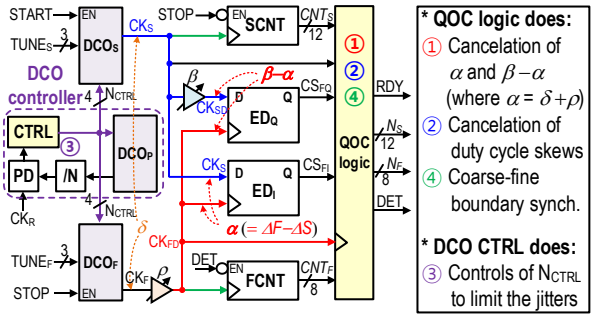

Fig. 2. Block diagram of the QOC-TDC specifying the offset cancellation.

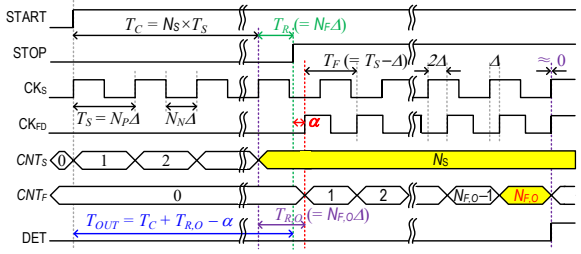

Fig. 3. Timing diagram of a cyclic Vernier TDC with non-ideal offset cases.

single target output frequency. Thus, a compact design of CTRL supporting a narrow range of N_{CTRL} is applicable, and the DCO controller can be much smaller than conventional digital PLLs. DCO_P is a ring oscillator that consists of inverters with parallel NAND cells (INV-NAND) for delay tuning [22]. The INV-NAND structure is also used to build tunable delay cells throughout this work. A pair of oscillators DCO_S and DCO_F are identical to DCO_P since they intend to generate almost the same but slightly different frequencies for the Vernier operation. DCO_S and DCO_F are calibrated by $TUNE_S$ and $TUNE_F$ so that the frequency difference between CK_S and CK_F is set to the target resolution of TDC.

Although we cannot eliminate the wiring mismatch δ between CK_S and CK_F, the extent of δ can be predictably constrained during the automated place-and-route step by limiting the wire length and the placement area [17]. A tunable delay cell ρ delays CK_F and generates CK_{FD}. Then, the offset α of CK_{FD} with respect to CK_S is tunable since $\alpha = \delta+\rho$. We calibrate ρ so that α becomes greater than the setup-and-hold time of edge detectors ED_I and ED_Q. The calibration provides a margin for avoiding the output glitches of ED_I and ED_Q due to the meta-stability at the beginning of calibration.

CK_{FD} and CK_S are then used as the operating clocks of the counters FCNT and SCNT, respectively. Another delay cell β generates a signal CK_{SD} which is ideally a quadrature-delayed version of CK_S. Then, the offset of CK_{SD} with respect to CK_{FD} becomes $\beta-\alpha$. ED_Q then detects the edges of CK_S to enhance the throughput.

The captured signals CS_{FI} and CS_{FQ}, and the measured counts CNT_S and CNT_F, are processed in the QOC logic block. It cancels all the offsets as shown in Fig. 2 and generates a coarse count N_S, a residual count N_F, a flag DET for the edge detection, and a signal RDY indicating the output is ready.

III. Cyclic Vernier Time-to-Digital Converter with Quad-Edge Offset Cancellation

A. Basic Concept of the Offset Cancellation

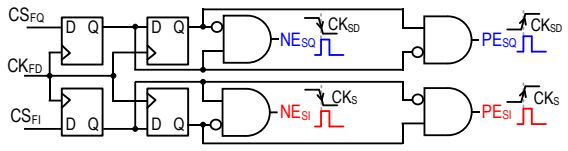

Fig. 4. A quad-edge pulse generation circuit in the QOC logic block.

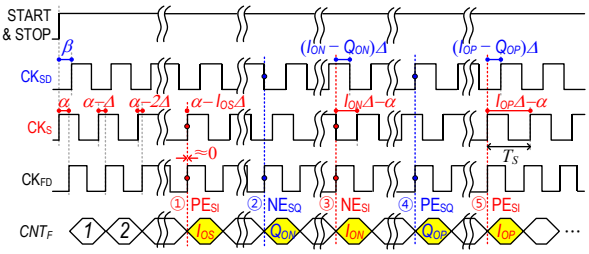

Fig. 5. Timing diagram of the offset estimations during calbration.

The proposed QOC-TDC offers precise measurements by canceling the offset α from the initial residual timing $T_{R,O}$, as shown in Fig. 3. The resolution Δ of the cyclic Vernier TDC is expressed as follows:

$$\Delta = T_S - T_F , \tag{1}$$

where T_S and T_F are the periods of CK_S and CK_F, respectively. Then, the TDC output T_{OUT} is expressed as follows:

$$T_{OUT} = T_C + T_R = (N_S - 1)T_S + N_F\Delta . \tag{2}$$

A more practical case of a non-zero offset, as shown in Fig. 3, leads to an extra offset term of α in (2) so that

$$T_{OUT,OFFSET} = T_C + T_R + \alpha . \tag{3}$$

The QOC-TDC cancels the offset α from $T_{OUT,OFFSET}$.

B. Offset Measurement Procedure during Calibration

As shown in Fig. 4, four pulses (PE_{SI}, NE_{SQ}, NE_{SI}, and PE_{SQ}) are generated by a clock-domain-crossing circuit in the QOC logic block. The pulses indicate the positive and negative edge detections of CK_S and CK_{SD}. The same signal is applied to both START and STOP for simultaneous activation of DCO_F and DCO_S during calibration, as shown in Fig. 5. Then, five offset counts (I_{OS}, Q_{ON}, I_{ON}, Q_{OP}, and I_{OP}) are sequentially captured by the pulses, as shown in Fig. 5. At the 1st PE_{SI} pulse, $\alpha \approx I_{OS}\Delta$ since $\alpha - I_{OS}\Delta \approx 0$. Similarly, we can acquire the following relationship at the 2nd PE_{SI} pulse:

$$T_S \approx (I_{OP} - I_{OS})\Delta = N_P\Delta . \tag{4}$$

Δ can be monitored by (4) if T_S is measured from CK_S.

The duty cycle skews of CK_S (τ_S) and CK_{SD} (τ_{SD}) are also included in the offset counts I_{ON} and Q_{ON}, as shown in Fig. 6 (a). I_{ON} and Q_{ON} measure the extent of such skews, and therefore the QOC scheme relaxes the duty cycle requirement of CK_S and CK_{SD}. Note that the duty cycle of CK_{FD} does not affect the offset since only the positive edges are used.

Although SLC flip-flops can be used as the edge detectors [18], their meta-stability by the setup time (T_{SU}) and the hold time (T_{HL}) is not controllable. Thus, α needs to be chosen to avoid the glitches at the start of calibration as follows:

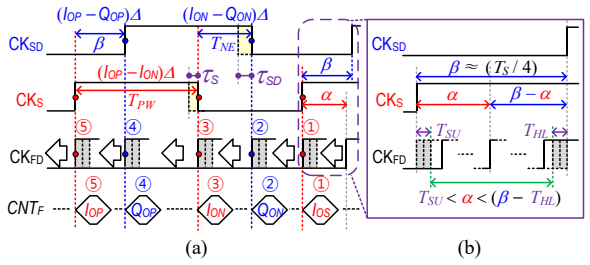

Fig. 6. Diagrams of (a) the sequence of the offset measurement and (b) indicating the valid range of delay α to avoid the setup-and-hold time violations.

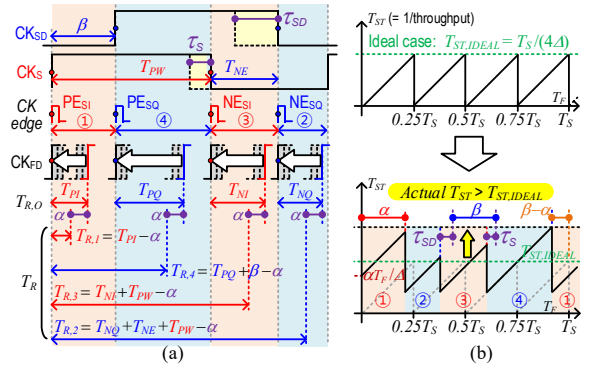

Fig. 7. Diagrams showing (a) the offset cancellation in T_F and (b) the effect of the offsets on the throughput performance.

$$T_{SU} < \alpha < (\beta - T_{HL}), \tag{5}$$

where $\alpha = \delta + \rho$, as shown in Fig. 6 (b). A correctly chosen α gives the robustness against the variation of the meta-stable region. The value of β is coarsely set to about $T_S/4$ to maximize the throughput. The values of T_{SU} and T_{HL} are process-dependent. For example, $T_{SU} \leq 73$ps and $T_{HL} \leq 32$ps at the worst PVT corners in the 28nm process used in this work. Therefore, if $T_S = 784$ps, then any value between 73ps and 123ps can be chosen as α, and the constraint on ρ is well relaxed. After calibration, the offset counts, including the setup-and-hold time offsets, are stored in the registers and used to cancel the offsets in the normal mode.

C. Offset Cancellation Procedure in the Normal Mode

The QOC-TDC measures the input timing in the normal mode and generates N_S and an initial residual count $N_{F,O}$. N_S can be directly measured from SCNT, but $N_{F,O}$ includes the offset α which is to be canceled. The initial residual timing $T_{R,O}$ is expressed as follows:

$$T_{R,O} = N_{F,O}\Delta = (N_F + I_{OS})\Delta. \tag{6}$$

Since the offsets at different edges may not be the same, four independent cancellation schemes are required.

The cancellation schemes are shown in Fig. 7 (a). For case ①, a final residual timing T_R is expressed as follows:

$$T_{R,1} = \left(N_{F,O} - I_{OS} + \left(P_{F,O} \times N_P\right)\right)\Delta, \tag{7}$$

where $P_{F,O} = Boolean$ ($N_{F,O} < I_{OS}$) to keep $T_{R,1}$ positive. In the case of ③, T_R is expressed as follows:

$$T_{R,3} = (N_{F,O} + I_{OP} - I_{ON} - I_{OS})\Delta \tag{8}$$

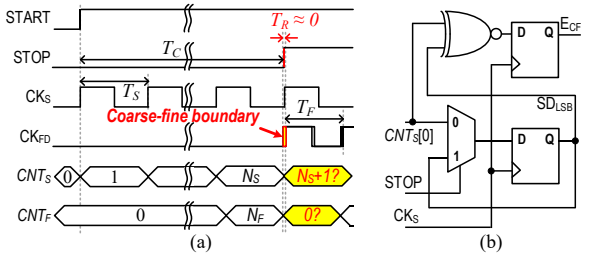

Fig. 8. (a) A coarse-fine boundary case and (b) the synchronization circuit.

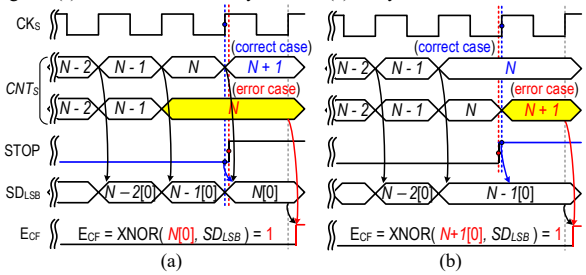

Fig. 9. Timing diagrams of the boundary cases: (a) $N_{F,O} \geq I_{OS}$ and (b) $N_{F,O} < I_{OS}$.

by (6) and T_{PW} in Fig. 6 (a). Similarly, T_R for the case ④ is expressed as follows:

$$T_{R,4} = (N_{F,O} + I_{OP} - Q_{OP} - I_{OS})\Delta \tag{9}$$

by (6) and β in Fig. 6 (a). Then, T_R for the case ② is expressed as follows:

$$T_{R,2} = (N_{F,O} + I_{OP} - Q_{ON} - I_{OS})\Delta \tag{10}$$

by (6), T_{NE}, and T_{PW} in Fig. 6 (a). The result from the earliest detected edge among (7)-(10) becomes the final residual count N_F, which enhances the throughput. In summary, the QOC scheme measures all the offsets and cancels them from N_F. Fig. 7 (b) depicts the throughput ($1/T_{ST}$) decrease due to the effects of $\alpha T_F/\Delta$, α , β, and the duty cycle skews.

D. Boundary Synchronization of Coarse-fine Counts

The cyclic Vernier TDCs may suffer from the output non-linearity at the boundaries of the coarse-fine counts since T_S and T_F are asynchronously measured, as shown in Fig. 8 (a). The boundary conditions generally occur in the case of ① in Fig. 7. A circuit in the QOC block, shown in Fig. 8 (b), verifies the sanity of N_S based on the finely measured $N_{F,O}$ and corrects the potential errors.

In the case of $N_{F,O} \geq I_{OS}$, the value of CNT_S is expected to be incremented, while it is not to be incremented in the other case of $N_{F,O} < I_{OS}$. Fig. 9 shows the correct (in blue) and erroneous (in red) operation of CNT_S for both cases. The errors in N_S are detected and corrected as follows:

$$N_{S,NEW} = CNT_S + \left(1 - 2 \times P_{F,O}\right) \times E_{CF}. \tag{11}$$

By the scheme above, the monotonicity of output is enhanced.

IV. Simulation Results

The QOC-TDC was implemented within the area of 0.011mm^2 in 28nm CMOS process, as shown in Fig. 10. The results in Fig. 11 showed that the QOC-TDC offers accurate offset estimations with robustness against the variations. It

TABLE I. COMPARISON OF RECENT FULLY-SYNTHESIZABLE TIME-TO-DIGITAL CONVERTERS

Year	2011	2015[a]	2015	2018[a]	2020	2020[a]	This work[a]
Publisher	TCAS-I [18]	NEWCAS [24]	ISSCC [1]	ISCAS [7]	ACCESS [25]	MWSCAS [22]	
Type	Cyclic Vernier	Spatial Oversampling	Stochastic Interpolation	Stochastic Interpolation	Tapped Delay-lines	Cyclic Vernier	Cyclic Vernier
Area (mm^2 @ node)	0.0060 @ 65n	0.0200 @ 65n	0.036 @ 14n	0.2210 @ 65n	0.089 @ 180n	0.0016 @ 130n	0.0109 @ 28n
Power (mW @V_{DD})	2.00 @ 1.0V	3.90 @ 1.0V	0.78 @ 0.6V	70.80 @ 0.8V	5.4 @ 1.8V	0.47 @ 1.2V	3.4 @ 1.0V
Resolution (ps)	5.5	7	1.17	0.85	111	2.8	4.5
Output range (bits)	15	11	10	14	20.6	17	19
Throughput (MS/s)	10	50	100	125	10	10.5	22
SSP (LSB)	0.78[b]	0.34	N/A	1.11	0.49	N/A	0.98
INL (LSB)	N/A	N/A	2.3	2.94	8	N/A	3.0
FoM_N[d] (pJ/step)	N/A	N/A	0.025137	0.136207	0.003058	N/A	0.001179
FoM_B[e] (pJ/step)	0.006104	0.038086	0.007617	0.034570	0.000340	0.000343	0.000295
SLC only?	Yes	Yes	Yes	Yes	Yes	No	Yes
Offset canceling?	No	No	Yes	Yes	Yes	Yes (partly)[c]	Yes

[a] Post-layout simulation results. [b] Only valid in short-range inputs within T_{IN} = 210ps (e.g. The SSP of 4.18 LSB at T_{IN} = 100ns). [c] Does not cancel the duty cycle skews (only cancels the wiring mismatch)
[d] FoM_N = Power (mW) / {2^{Nlin} × Rate (MS/s)}, where *Nlin* (effective number of linear bits) = Bits – $\log_2$(INL + 1) [26-29]. [e] FoM_B = Power (mW) / {2^{Bits} × Rate (MS/s)} [28-29].

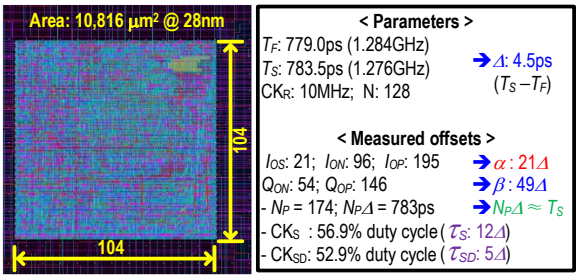

Fig. 10. Layout of QOC-TDC with the parameters and the measured offsets.

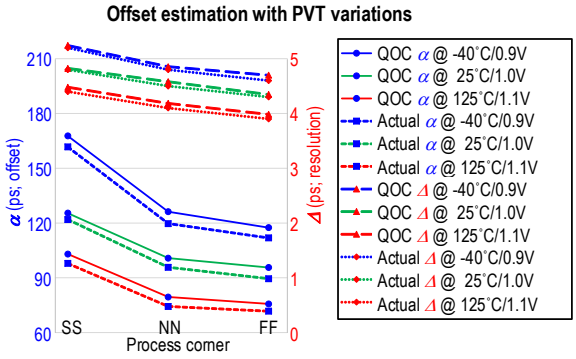

Fig. 11. Post-layout simulations of the offset measurement versus the corners.

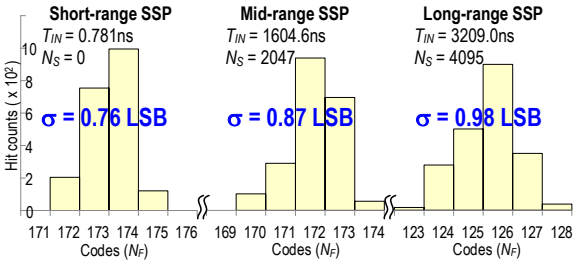

Fig. 12. Post-layout simulations of the single-shot precision (for 2,000 trials).

achieved a 19-bit range, a 4.5-ps resolution, and throughput of 22MS/s. The single-shot precision was 0.98LSB and the INL was less than 3LSBs, as shown in Figs. 12-14.

Table I summarizes the performance of recent works. Here we have chosen a popular Figure-of-Merit (FoM_N) for TDCs. We have also used FoM_B to compare the works without *Nlin*. It is shown that this work achieves the best FoM_N and FoM_B

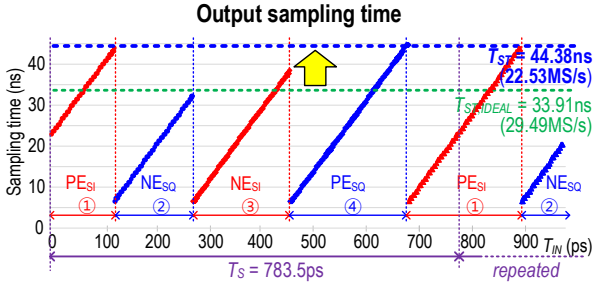

Fig. 13. Post-layout simulations of the sampling time (22MS/sec throughput).

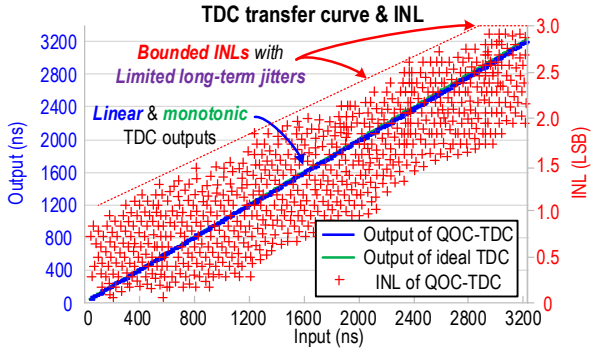

Fig. 14. Post-layout simulations of the transfer curve and the INL performance. Only the worst INLs at every 9.0ns-interval are plotted to show the distribution.

among all work listed. It is the only cyclic Vernier TDC among listed, supporting the full offset-canceling feature for superior FoMs, while it requires only SLCs for the synthesis.

V. CONCLUSION

We designed a fully-synthesizable QOC-TDC that cancels the several offsets altogether. The QOC-TDC first measured the offsets during calibration, and it canceled the offsets in the normal mode. It also synchronized the values of counter outputs at the coarse-fine boundaries to improve the output accuracy and monotonicity. It achieved a 19-bit range and a 4.5-ps resolution with a throughput of 22MS/s, while it consumed 3.4mW at the supply of 1.0V in a 28nm CMOS.

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