8.4-to-16-bit resolution, 1-to-16 kHz bandwidth ADC with programmable-gain functionality for multi-sensor applications

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A resolution-reconfigurable, bandwidth-scalable analogue-to-digital converter (ADC) with programmable-gain (PG) functionality for a multi-sensor system, which encompasses various signals such as bio-signals and battery-level, is presented. In PG and low-power mode, a PG first-order noise-shaping (NS) successive-approximation register (SAR) ADC achieves 8.4-to-10.2-bit operating up to 16 kHz while providing a gain of 1/2/4. The PG NS SAR ADC can be reconfigured as an adder and a quantiser in a delta-sigma (ΔΣ) modulator enhancing the order of the modulator for high-resolution. The third-order ΔΣ modulator achieves 16.1 bits in a bandwidth of 1 kHz. The work is implemented in a 0.18 µm CMOS process with a 1.8 V power supply.

Introduction: Analogue-to-digital converters (ADCs) in various mobile applications are required to handle signals with varying dynamic range and bandwidth [1, 2]. In this context, a reconfigurable ADC can significantly reduce the size, cost, and energy consumption of such systems. Therefore, a single reconfigurable ADC for multi-modes has been proposed [2, 3]. However, according to Yip and Chandrakasan [2], have a low resolution of 8.8 bits, and Porrazzo *et al*. [3] achieve more than 14 bits in 16 kHz but consuming excessive energy for low-resolution applications. In this Letter, we propose a reconfigurable ADC with programmable-gain (PG) functionality that achieves resolution-reconfigurable 8.4-to-16-bit and bandwidth-scalable 1–16 kHz, which includes low-resolution and low-power applications such as neural spike sorting and battery-level monitoring (up to 8.4 bits and 16 kHz bandwidth) and high-resolution applications such as ECG monitoring (16 bits and 1 kHz bandwidth).

PG noise-shaping (NS) ADC: Embedding a PG functionality in a reconfigurable ADC reduces its area, cost, and energy consumption further by possibly reducing an additional gain stage in the signal chain. Moreover, it can alleviate the noise requirements for the preceding stages of the ADC. Fig. 1 shows the half-circuit diagram of the proposed PG first-order NS SAR ADC for simplicity. A conventional NS SAR ADC [4] exploits the residual voltage on the capacitor digital-to-analogue (CDAC) array at the end of a bit-cycling phase. PG functionality can be embedded in the ADC by varying the ratio between *CA* and *CF* as long as the values of the *CF* and the residue capacitor (*CRE* or *CRO*) are equal, and charge conservation ensures that NS occurs. The timing diagram is shown in Fig. 2. PE and PO denote the even and odd phases, respectively. At the end of P1E after 4-bit cycling, the residual voltage is stored on *CRE*. During the phase P2O, the input signal, *IN*, is transferred onto the CDAC array with gain. The residual voltage on *CRE* is fed back to the input of the amplifier *XN* to perform high-pass filtering of quantisation noise. The capacitors *CRE* and *CRO* store the residual voltages in the even and odd phases, respectively. The output voltage of the amplifier, which is sampled on the CDAC array *VXN*, can be described as

$$YN[n] = \frac{CA}{CF} \cdot IN[n] - \frac{CRE}{CF} \cdot E[n-1] \tag{1}$$

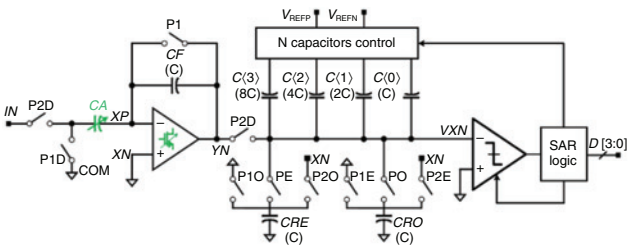

Fig. 1 *Half-circuit of PG first-order NS SAR ADC*

Since *CRE*, *CRO*, and *CF* are equal, the output the ADC can be expressed as

$$\begin{aligned} D[n] &= YN[n] + e[n] \\ &= \frac{CA}{CF} \cdot IN[n] - e[n-1] + e[n] \end{aligned} \tag{2}$$

The transfer function of the PG NS SAR ADC can be expressed as

$$D[z] = \frac{CA}{CF} \cdot IN[z] + (1 - z^{-1})E[z] \tag{3}$$

Therefore, a PG can be achieved by the ratio between *CA* and *CF* while providing first-order high-pass filtering of quantisation noise. In order to avoid implementing power-consuming two-stage amplifier for a large output swing, a folded-cascode amplifier is adopted while the reference voltage of the PG NS SAR ADC is halved. V_{REFP} is the mid-level between VDD (1.8 V) and COM (0.9 V) and V_{REFN} is the mid-level between COM and ground. The amplifier can be power-scaled for efficient power consumption of the system for various modes. For gains of 1/2/4, *CA* is set to 0.5C/1C/2C, where a unit capacitor C is 120 fF.

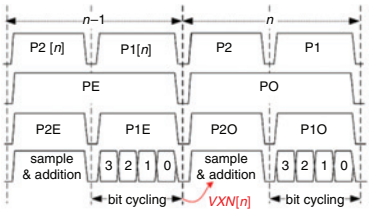

Fig. 2 *Timing diagram of ADC*

The simulation results of the proposed PG first-order NS SAR ADC with gains of 1/2/4 are shown in Fig. 3. The ADC was simulated with a sampling frequency of 2.048 MHz and an input frequency of 10.01 kHz. The power spectral densities (PSDs) of the ADC with different gain settings show that the PG functionality has been embedded successfully while achieving a first-order NS with signal-to-quantisation noise ratios higher than 69.5 dB.

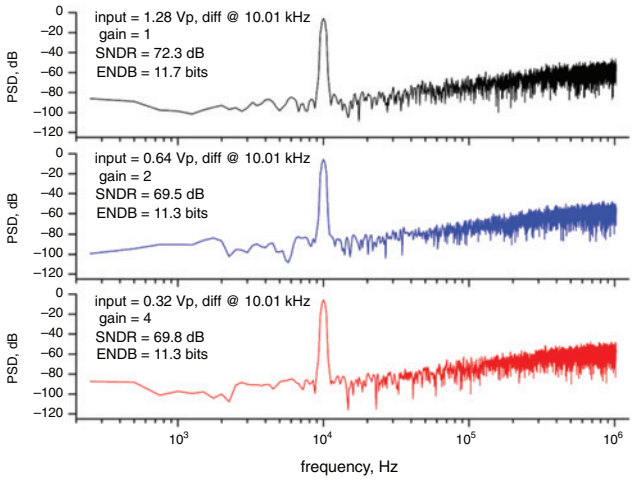

Fig. 3 *Simulation results of PG NS SAR ADC with gains of 1/2/4*

Third-order delta-sigma (ΔΣ) ADC: The first-order NS SAR ADC shown can be reconfigured as an adder and a quantiser to increase the reusability of the ADC and the order of the modulator as shown in Fig. 4. Loop-filter, binary-to-thermometer (B2T) decoder, and dynamic element matching (DEM) are enabled in this mode. B2T converts the 4-bit binary data to 15-bit thermometer codes and DEM randomises the codes to reduce the distortion caused by the DAC. *CA* is also reconfigured to realise the coefficients a1, a2, a3, and b3. The noise transfer function (NTF) can be described as

$$\mathrm{NTF} = \frac{(z-1)^3}{z(z^2 - 0.5z + 0.206)} \tag{4}$$

which is accomplished by the second-order loop filter and the first-order NS SAR ADC. This configuration avoids the need for the accurate high-speed sampling clock signal and limits the oversampling ratio (OSR) to 64, reducing current consumption of the amplifiers in the loop filter. Also, using a single comparator instead of 15 comparators found in a conventional 4-bit flash ADC reduces power consumption significantly. Besides, the quantisation noise from the previous conversion can work as a dither signal, resulting in reduced idle tones and harmonic spurs for improved linearity [5]. The input-feedforward CIFF topology allows the LF to process the quantisation noise, reducing the swing required from the amplifier [6].

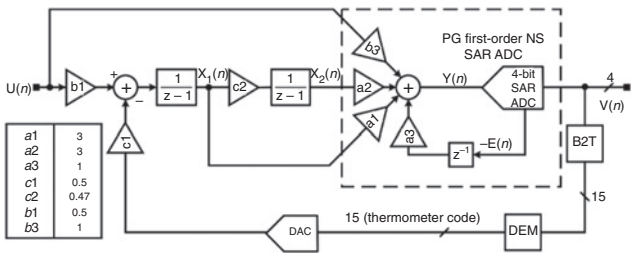

Fig. 4 *Block diagram of ΔΣ modulator incorporating PG NS SAR ADC as adder and quantiser*

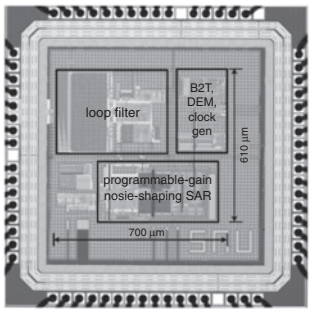

Fig. 5 *Die photograph of the prototype*

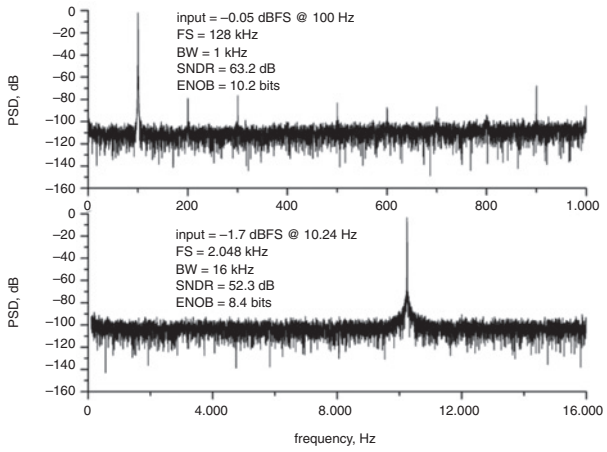

Fig. 6 *Measured PSD of first-order NS ADC at different sampling frequencies*

Experimental results: The prototype, which was fabricated in a 0.18 µm CMOS technology, is shown in Fig. 5. The ADC occupies an area of 0.42 mm^2. Fig. 6 shows the measured PSD of the digital output of the PG first-order NS SAR ADC at different sampling frequencies of 128 kHz and 2.048 MHz. The first-order modulator achieves 8.4-to-10.2-bit operating up to 16 kHz. Fig. 6 shows measured PSD of the digital output of the third-order ΔΣ modulator at a sampling frequency of 128 kHz. The third-order modulator has an SNR of 98.5 dB, and a maximum SNDR of 98.4 dB at −0.4 dBFS, while dissipating 25.5 µA with a 1.8 V supply. It achieves a Schreier figure of merit of 171.8 dB. The measured PSD (Fig. 7), attenuated with a 60 dB/decade slope, indicates that the NTF enhancement is successfully employed.

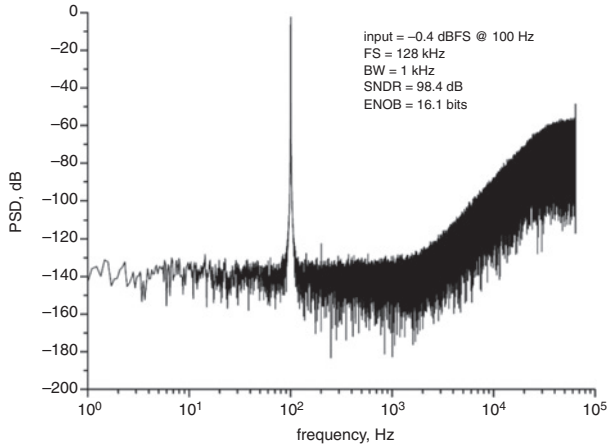

Fig. 7 *Measured PSD of third-order ΔΣ modulator*

Conclusion: A resolution-reconfigurable, bandwidth-scalable ADC for a multi-sensor system is presented. It combines the benefits of PG functionality and NS, which can operate in either a PG low-power mode or a high-resolution mode, reducing hardware, production cost, and power consumption making it suitable for multi-sensor systems.

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One or more of the Figures in this Letter are available in colour online.

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