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A 3.2 GHz Quadrature Error Corrector for DRAM Transmitters, using Replica Serializers and Pulse-Shrinking Delay Lines

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***Abstract*— For DRAM transmitters, in this letter, we propose a quadrature error corrector (QEC), in which clock signal phase errors are corrected using two replicas of the 4:1 serializer of the output stage. Pulse shrinking is used to compare and equalize the outputs of these two replica serializers. To validate the effectiveness of the QEC, a prototype quarter-rate transmitter including our QEC was fabricated in 65nm CMOS. Adopting our QEC, the experimental results show that the output phase errors of the transmitter are reduced to a residual error of 0.8ps and the output eye width and height are improved by 84% and 61% respectively, at a data-rate of 12.8Gbps.**

***Index Terms*— DRAM interface, pulse-shrinking delay line, quadrature error corrector, replica serializer.**

I. Introduction

The growing interest in big data, cloud computing, and artificial intelligence requires higher memory bandwidth. The data-rate of DDR5 and LPDDR5 memory has increased to 6.4Gbps, and the next generation of DRAM is expected to operate above 10Gbps [1]-[2].

At such a high data-rate, dividing the input clock signal and using a quarter-rate clock to drive internal circuits is advantageous in terms of timing margin [3]-[5]. However, during four-phase clock generation and distribution, factors such as process, voltage, and temperature (PVT) variations, mismatches between the clock trees of each phase, and supply and ground noise can cause quadrature phase errors. As these errors increase, the signal integrity of the transmitter (TX) output deteriorates, reducing its effective bandwidth. A data-dependent jitter (DDJ) in the output stage due to the PVT variation is another important factor for the signal integrity of a high-speed interconnection [6]. The output impedance is calibrated using external ZQ resistor [2], and considering large PVT variation in DRAM process, the distortion in the serializer (SER) should also be corrected to assure the integrity of the output signal.

A quadrature error corrector (QEC) can be implemented using analog circuits [7], but a QEC of this type is vulnerable to PVT variations, current mismatches, voltage offsets, and noise. In addition, because a DRAM is often idle, and low standby power is a key part of its specification, a digital QEC that consumes far less standby power than an analog one is more suitable for a DRAM TX. A digital QEC with reference delay line and phase detector requires iteration or locking procedure of the reference delay line, like delay-locked loop (DLL). A single shared loop filter can be used to minimize the effect of the mismatches between phase detectors [4], but it is difficult to operate at a higher frequency due to the tight internal timing margin. A time-to-digital converter (TDC) can be used to detect phase error, but counter-based TDC requires an additional clock source [8]. Alternatively, a vernier TDC architecture is widely adopted thanks to the simplicity of its design concept [9], but it consumes large area and power. On the other hand, the above QECs detect and correct phase errors in the clock trees, thus the distortion in the SER still remains.

To correct quadrature errors including distortions in the SER, we propose a QEC including two replicas of the SER of the output stage. Each replica SER converts associated clock phase difference to pulse width. Two pulse-shrinking delay lines (PSDLs) are used as a digital pulse-width comparator instead of area and power-hungry TDCs. A phase adjuster equalizes the two pulses based on the result of the comparison. As a result, the PVT variations in the SER of the output stage can be compensated during phase error correction by this QEC. A fine delay unit is added to the first stage of each PSDL to improve the accuracy of phase error detection.

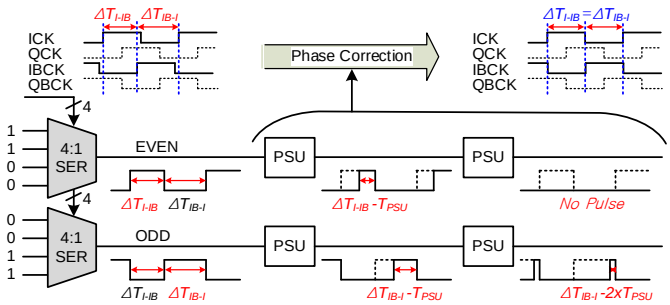

Fig. 1. Simplified block diagram of phase correction using replicated serializers and pulse-shrinking units.

II. Proposed Quadrature Error Corrector

A. Phase Correction using Replica Serializers and Pulse-Shrinking Units

Fig. 1 is a simplified block diagram of phase correction using two replicated SERs and pulse-shrinking units (PSUs). T_{PSU} is the delay of a rising edge through a PSU, the $\Delta T_{I\text{-}IB}$ is the time difference between the rising edges of ICK and IBCK, and $\Delta T_{IB\text{-}I}$ is the interval between the rising edges of IBCK and ICK. Each SER converts the clock phase differences $\Delta T_{I\text{-}IB}$ and $\Delta T_{IB\text{-}I}$ to pulses, and their widths are compared using multi-stage PSUs. As each signal passes through a PSU, its rising edge is delayed by T_{PSU}, reducing the pulse width, so that either the EVEN or the ODD pulse disappears. Using the result of this comparison, the clock phases are corrected and $\Delta T_{I\text{-}IB}$ and $\Delta T_{IB\text{-}I}$ become equal. Because the phase error is detected based on the output of the 4:1 SER, compensation includes errors caused by the PVT variations in the SER. Two SERs are used to prevent mismatches that can occur when the output of one SER is inverted for the comparison

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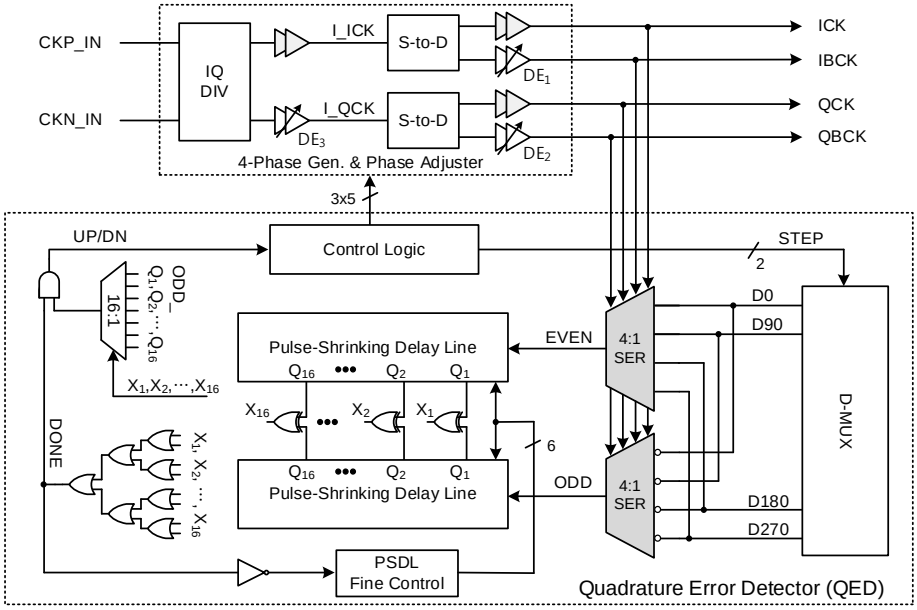

Fig. 2. Block diagram of proposed QEC.

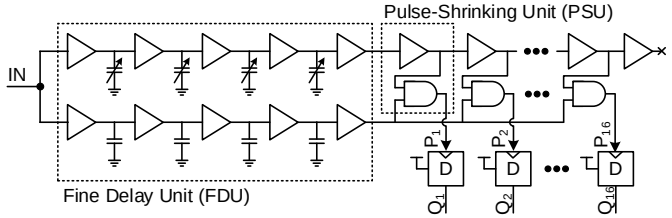

Fig. 3. Block diagram of a pulse-shrinking delay line.

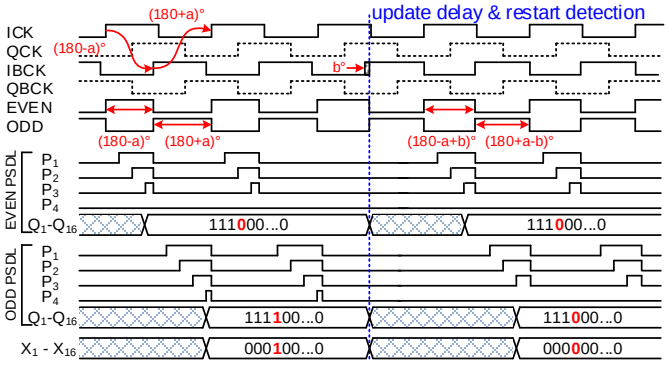

Fig. 4. Timing diagram of the QEC correcting phase between ICK and IBCK.

described above. For simplicity, Fig. 1 only shows the correction of the phase between ICK and IBCK; the other phases are corrected in the same way.

B. Overall QEC Architecture and its Operation

Fig. 2 is a block diagram of the proposed QEC, which consists of a four-phase generator, a phase adjuster, and a quadrature error detector (QED). Four quarter-rate clock signals with 90° phase separation are generated by dividing two half-rate clocks, CKP_IN and CKN_IN, and applying the divided clocks to two single-to-differential converters. The QEC corrects the quadrature errors between the four-phase clock signals in three steps without additional iteration. The 180° phase between ICK and IBCK is corrected first using a delay element DE_1, and then the 180° phase between QCK and QBCK is corrected using a delay element DE_2. Finally, the phases between ICK and QCK and between IBCK and QBCK are corrected simultaneously using delay element DE_3 by correcting the 90° phase between I_ICK and I_QCK, which are the clock signals before single-to-differential conversion. Each delay element in the phase adjuster is based on binary-weighted MOSCAP delays that provide a resolution of 1ps.

The QEC corrects the phase error by comparing and equalizing the pulse widths of an EVEN and an ODD signal, which are complementary clock patterns generated by two replicated 4:1 SERs that receive the appropriate data from the D-MUX for each step of the correction process. During the first step to correcting phases between ICK and IBCK, the inputs to the 4:1 SERs, D0, D90, D180, and D270, are 1, 1, 0, and 0 respectively, so that the data pattern of EVEN is 1100 and the data pattern of ODD is 0011. By equalizing the pulse widths of these two signals, the phase difference between ICK and IBCK becomes 180°. During the second step for correcting phases between QCK and QBCK, the four inputs to the SERs are 0, 1, 1, and 0, so that EVEN is 0110 and ODD is 1001; and during the last step, the inputs are 1, 0, 1, and 0, making EVEN 1010 and ODD 0101.

Two PSDLs are used to compare the pulse widths of the EVEN and ODD signals. A PSDL consists of a fine delay unit (FDU), together with 16 stages of PSUs and D flip-flops (DFFs). Each PSU includes a buffer and an AND gate, as shown in Fig. 3. The pulse output by each PSU is gradually shrunk by one buffer delay, T_{PSU}, and is applied to the clock input of the corresponding DFF, whose data input is tied to VDD. The true single-phase clocked (TSPC) DFFs are used to eliminate the side-effects of generating a complementary pulse from a PSU output. Because the pulse widths of the EVEN and ODD signals in the first and second step are twice the unit-interval (UI), the number of PSU stages needs to be larger than $2\times UI/T_{PSU}$.

Starting with all DFFs reset, the output of a DFF changes to 1 if the corresponding PSU output carries the pulse, whereas the output of the DFF remains 0 if the corresponding PSU output is not pulsing. The output of each PSDL, Q_1-Q_{16}, consists of a sequence of 1s followed by a sequence of 0s, i.e. of the form '111…000', and the number of consecutive 1s corresponds to the width of the pulse at the input to the PSDL. However, the exact number of 1s in the PSDL output sequence is not a concern in our QEC; the difference between the two outputs is important. To minimize mismatch, the two PSDLs are laid out as symmetrically as possible, including dummy patterns [10]. The detection offset can be monitored by the '1100' pattern output of the prototype Tx. The duty cycle error corresponds to the offset between the EVEN_PSDL and the ODD_PSDL, and this offset can be improved by adjusting the initial delays of the two PSDLs.

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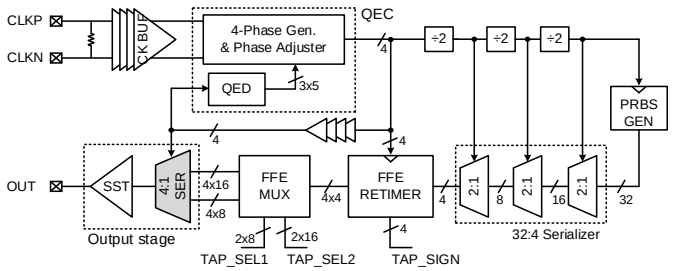

Fig. 5. Block diagram of the prototype transmitter.

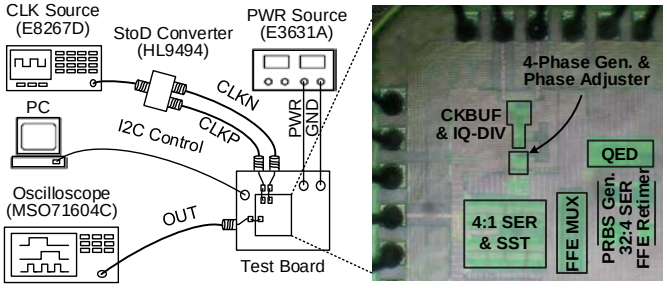

Fig. 6. Measurement setup and die micrograph.

The 16 XOR gates shown in Fig. 2 compare the outputs of the two PSDLs. When they differ, one of the XOR outputs, X_K from X_1 to X_{16}, becomes 1 and the corresponding output ODD_Q_K from the ODD PSDL indicates which of the pulse width of EVEN or ODD is larger. If ODD_Q_K is 1, the QEC increases the delay of the clock signal, and if ODD_Q_K is 0, the QEC decreases the delay.

The above comparison and update procedure is performed every 32 cycles, with a loop bandwidth of 200MHz at 12.8Gbps. To minimize the effects of input jitter and power noise, 14 pulses are cumulatively sampled and compared in the first and second steps, and 28 pulses in the third step.

Fig. 4 shows an example timing diagram for the first step to correct the phase error between ICK and IBCK. Since IBCK has been pulled by a°, the pulse widths of EVEN and ODD are (180 – a)° and (180 + a)° respectively. The output P_4 from the fourth PSU of the EVEN PSDL is low, but the ODD PSDL is still asserted. Thus the output of the corresponding DFF, EVEN_Q_4, is 0, whereas ODD_Q_4 is 1. Then X_4 is the only 1 among the XOR gate outputs X_1 to X_{16}. The 16:1 multiplexer passes ODD_Q_4, and the UP/DN signal is also 1. In response to this signal, the control logic increases the IBCK delay by an amount corresponding to b°, which is the delay control step of the phase adjuster. Now the phase error is reduced to |a – b|° and when this is smaller than one buffer delay, the pulse traveling through each PSDL is shrunk to nothing in the same position in each PSDL, and the outputs of both PSDLs can be the same.

C. *Fine Delay Unit in the PSDL*

To improve the accuracy with which phase errors are detected, a fine delay unit (FDU) is located in front of the PSU of the first stage. The FDU applies a variable delay to a shrinking edge and a fixed delay to a non-shrinking edge, as shown in Fig. 3. Four stages of 3-bit binary-weighted MOSCAP delay elements produce a total variable delay that is larger than the delay associated with one stage of a PSU. In our design, one buffer delay of a PSU is 26ps from the post-layout simulation of the typical corner. Hence the FDU is implemented in 32 steps with 1ps resolution to cover the T_{PSU}, and for all PVT corners, the delay of FDU is larger than T_{PSU}. The capacitive load is distributed across the delay elements to improve the bandwidth.

Initially, both variable and fixed delays of an FDU have the same minimum value. If the outputs of the two PSDLs are the same, then the

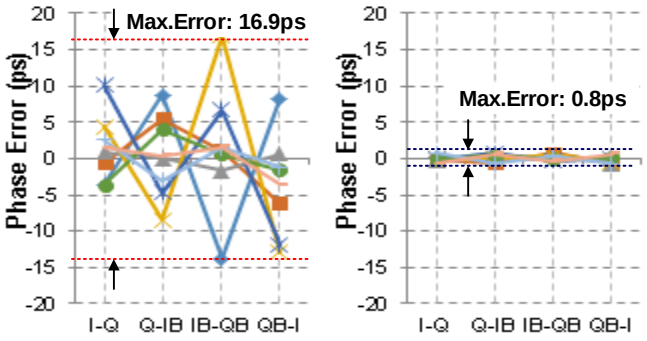

Fig. 7. Measurements of (a) uncorrected and (b) corrected output phase error.

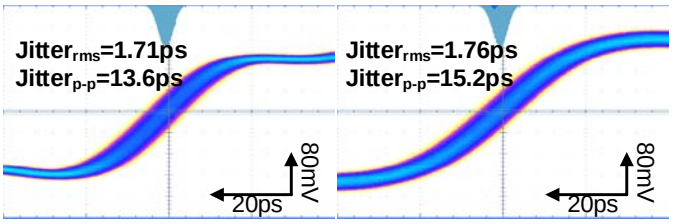

Fig. 8. Measured (a) input and (b) output clock jitter at 6.4 GHz.

XOR outputs X_1 to X_{16}, shown in Fig. 2, are all 0, and the DONE signal is not asserted. In this case, the FDUs of both PSDLs increase the variable delay and push the shrinking edges so that the shorter pulse disappears one stage earlier and the outputs of the two PSDLs differ. The QEC repeatedly updates the clock phases and adjusts the fine delay until the difference between the pulse widths of the EVEN and ODD signal is less than the resolution of the variable delay provided by the FDU. When the comparison result has changed three times, the QEC holds the corrected clock phase and advances to the next step to repeat the correction procedure for the next pair of clock signals. After all three steps are completed, the QEC enters standby state to save power and then resumes the correction procedure by an external command.

III. Implementation and Measurement Results

The prototype quarter-rate transmitter with a 4-tap feed-forward equalizer (FFE), shown in Fig. 5, was fabricated in a 65nm CMOS process to assess the proposed QEC. The clock buffer (CKBUF) receives an external differential clock input (CLKP/CLKN), and the four-phase generator generates the quarter-rate clock signals from the received clock signals. A PRBS generator is included on the chip for test purposes. It produces 32-bit parallel data, which is serialized to 4-bit sequences by a 32:4 SER. The 4-bit output of the SER is re-timed and rearranged into 4-groups of 4-bit sequences by an FFE retimer. When the TAP_SIGN signal for each FFE tap is asserted, the tap coefficient becomes negative and the output of the corresponding FFE retimer is inverted. The output stage has 40 segments, each of which is composed of a 4:1 SER and a voltage-mode source-series terminated (SST) driver. The FFE multiplexer (FFE MUX) allocates the selected FFE tap data to each of the 40 output segments under the control of the TAP_SEL1 and TAP_SEL2 signals.

Fig. 6 shows the measurement setup and a die micrograph. Half-rate differential input clock signals are applied through an external single-to-differential converter, from which four-phase quarter-rate clock signals are generated inside the chip. To evaluate the performance of the QEC, phase errors were introduced into the quarter-rate clock signals during their generation. Fig. 7 shows the measured output phase error for eight cases of quadrature clock signals

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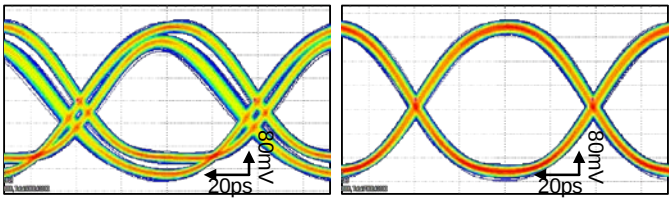
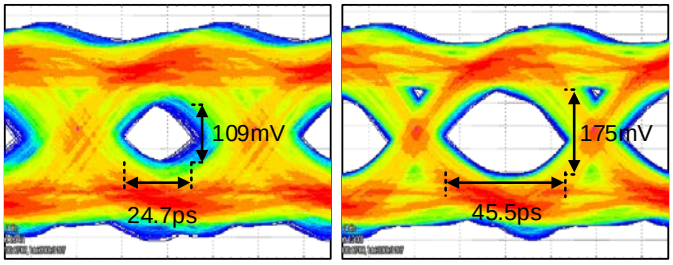


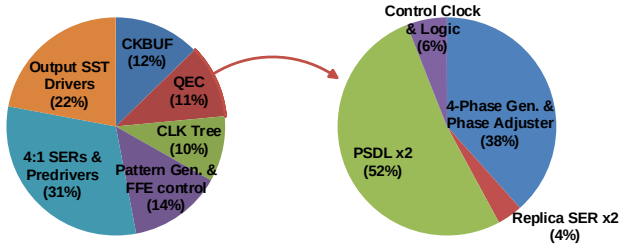
(a) (b)

Fig. 9. Measured TX output eye diagram of clock pattern at 12.8 Gbps (a) without and (b) with quadrature error correction.



(a) (b)

Fig. 10. Measured TX output eye diagram of PRBS pattern at 12.8 Gbps (a) without and (b) with quadrature error correction.



(a) (b)

Fig. 11. Power breakdown of (a) the prototype Tx and (b) the QEC

with uncorrected phase errors varying from -13.7ps to 16.9ps. The QEC corrects these phase errors to within 0.8ps.

As shown in Fig. 8, the measured jitter of the half-rate 6.4GHz input clock signal is 1.71ps$_{rms}$ or 13.6ps$_{p-p}$. The measured output jitter of the 6.4GHz clock pattern is 1.76ps$_{rms}$ or 15.2ps$_{p-p}$, and the jitters were increased slightly due to the residual phase errors between ICK and IBCK. Figs. 9 and 10 show measured eye diagrams of the output signals of the prototype TX with clock pattern and PRBS pattern, respectively, both at 12.8Gbps. The eye diagram in Fig. 9(a) shows two distinctive waveforms due to the quadrature phase skew, and the waveform of quadrature errors are corrected is shown in Fig. 9(b). In Fig. 10, 512k cycles of eyes were accumulated through the FR4 PCB channel with insertion loss of 7.8dB, and we can see that the width and height of the output eye are increased by 84% and 61% respectively after the correction of quadrature error. The power breakdowns of the prototype Tx and the QEC are shown in Fig. 11 and the total power consumption of the QEC is 6.7mW at 3.2GHz.

Table I compares the performance of other recent designs with that of our QEC, which has the lowest residual phase error with highest operating frequency. Another significant feature which distinguishes our design from the others listed in Table I is that it corrects errors in the serializer of the output stage.

IV. Conclusion

In a high data-rate DRAM interface, quarter-rate clock signals are advantageous in terms of the internal setup and hold timing margin, and overcoming the DCDL and clock-tree bandwidth limits. However, quadrature phase errors can occur during the generation and distribution of four-phase clock signals. In addition to reducing the residual quadrature phase error, signal integrity can also be improved by compensating for the distortion introduced by the output stage. We have presented a QEC for DRAM transmitter that corrects quadrature phase errors, including distortions in the serializer of the output stage. Pulse-shrinking delay lines are used to detect the phase errors, and a fine delay unit improves accuracy. A prototype quarter-rate transmitter including this QEC was fabricated in 65nm CMOS. At a data-rate of 12.8Gbps, it reduces phase errors in the transmitter to a residual error of 0.8ps. The output eye width and height are improved by 84% and 61% respectively.

TABLE I
Performance Summary and Comparison with Other QEC Designs

	[4]	[7]	[9]	[11]	This Work
Process	65nm	130nm	65nm	90nm	65nm
Supply	1.0V	1.2V	1.2V	1.0V	1.0V
Frequency	1.25GHz	2GHz	1GHz	2.7GHz	3.2GHz
Error Detector	Delay Line & BBPD	Clock Doubler & Integrator	TDC	TDC	SER & PSDL
Correction Range	10.4ps	63ps	40ps	-	16.9ps
Residual Phase Error	1.1ps	4.2ps	5ps	3.71ps	0.8ps
Jitter(rms)	2.53ps	-	2.98ps	-	1.76ps
Jitter(p-p)	15ps	-	19.4ps	-	15.2ps
Area	0.01mm^2	0.01mm^2	0.09mm^2	0.09mm^2	0.01mm^2
FoM (mW/GHz)	1.82	3.24	2.6	18.3	2.1

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