A 32-Channel Neural Recording System with a Liquid-Crystal Polymer MEA

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***Abstract*— Our integrated 32-channel recording system for *in-vivo* measurement of neural activity has 32 analog front-end (AFE) channels, a 32-to-1 time-division multiplexer, and a comparator-based cyclic ADC. Each channel has a low noise amplifier and a programmable-gain amplifier (PGA) with a tunable bandwidth. The mid-band gain of the low noise amplifier is 47dB. The total gain of the analog front-end is adjustable from 54dB to 67dB, and its input-referred noise is 11.93μV_{rms}. The low noise amplifier consumes 7.2μW per channel. The comparator-based cyclic ADC digitizes the signals at 20kS/s per channel, with a signal to distortion and noise ratio (SNDR) of 48.23dB, corresponding to an effective number of bits (ENOB) of 7.72. This system was implemented in 0.18μm CMOS technology, the average power consumption of the system is 62.5μW per channel. An *in-vivo* measurement of the electrical activity of the cerebral cortex has been demonstrated, using a flexible liquid-crystal polymer microelectrode array.**

I. INTRODUCTION

Multi-channel neural recording system is increasingly used in biomedical sensor applications. Recent research trend suggests that the neural recording system has been implanted below the skull and uses wireless data transmission to reduce the risk of infection. A neural recording system acquires neural activity, amplifies and filters it, and can also perform quantization and neural stimulation [1], [2]. It needs to be particularly small and power efficient, The heat generated must be limited to avoid tissue damage. It has been suggested that the power-to-area ratio should not exceed 80mW/cm^2 [3].

We present a low-power neural recording system that is able to measure neural action potential. Our system has been tested on the bench and *in-vivo* experiment.

The rest of this paper is organized as follows. In Section II, we describe the architecture of our 32-channel neural recording system and its components. In Section III, we provide the circuit implementation and operation. In Section IV, we present experimental results of the system performance and *in-vivo* neural recording experiment. Conclusions are drawn in Section V.

II. SYSTEM ARCHITECTURE

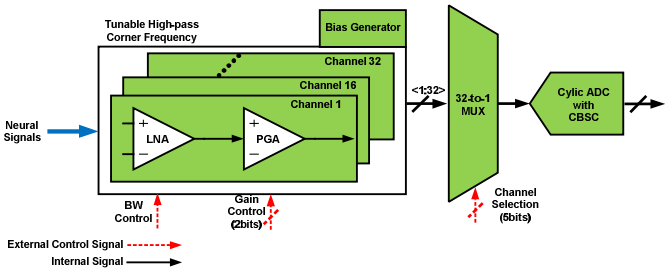

Figure 1. Block diagram of the neural recording system.

As shown in Fig.1, the neural recording system is composed of 32 analog front-end(AFE) channels, an analog 32-to-1 multiplexer, bias generators and a comparator-based cyclic analog-to-digital converter(ADC). The AFE includes a low-noise amplifier (LNA) and a programmable-gain amplifier (PGA) for each channel. Tunable pseudo-resistors in each LNA feedback path, controlled by an external voltage, can move the high-pass corner frequency. The PGA can change the overall gain of the AFE to match the input range of the ADC. An external 2-bit digital code provides four values of the AFE gain. After preamplification, the neural signals are passed through a 32-to-1 analog multiplexer, allowing each channel to be successively connected to the ADC. This ADC adopts a comparator-based switched-capacitor (CBSC) technique, and operates at 2MS/s, which is fast enough to digitize the signals from all 32 channels.

III. CIRCUIT DESIGN

A. Analog Front-End

Fig.2(a) is a schematic diagram of the LNA that acquires the neural signal. This uses the capacitor feedback topology [4] to reject the DC offset produced at the electrode-tissue interface. Using the tunable bandwidth of the AFE, the pseudo-resistors M_1-M_2 provide a high resistance R_x, of approximately 10^{10} to 10^{14} Ω which can be set by changing the gate voltage. A PMOS pseudo-resistor biased in the sub-threshold region is very sensitive to the gate voltage: the PMOS device size has to be large to control the resistance

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value by 10mV unit steps of the gate voltage. But the parasitic capacitance C_x around the pseudo-resistor affects the capacitance of the feedback path of the LNA.

The loop gain T(s) of the LNA can be approximated as follows:

$$T(s) = \frac{\alpha G_m R_{out}}{1 + sR_{out}C_{L,tot}} \quad (1)$$

$$where\ \alpha = \frac{C_I}{C_I + C_P + C_F + C_X}\ and\ C_{L,tot} = C_L + \frac{(C_F + C_X)(C_I + C_P)}{C_I + C_P + C_F + C_X}$$

C_p is the parasitic capacitance at the input of the operational transconductance amplifier (OTA) within the LNA, G_m is the transconductance of the OTA, C_L is the output load capacitance and R_{out} is the output load impedance. By nodal analysis using Kirchhoff's current law, the low-pass corner frequency is expressed as $1/(2\pi \times R_{out}C_{L,tot})$, where Assuming an adequate DC loop gain, the closed-loop transfer function H(s) of the LNA can be approximated as follows:

$$H(s) = \frac{C_I}{C_F + C_X} \times \frac{sR_X(C_F + C_X)}{1 + sR_X(C_F + C_X)} \quad (2)$$

The closed-loop gain of the amplifier is fixed at $C_I/(C_F+C_X)$. The high-pass corner frequency can be expressed as $1/\{2\pi \times R_X(C_F+C_X)\}$. The OTA within the LNA has a current mirror OTA design, as shown in Fig.2(b). The input devices of the OTA are operated in weak-inversion to minimize flicker and thermal noise, of which the latter is the dominant noise source in this circuit. The input-referred noise (IRN) of the OTA can be express as follows:

$$\overline{V_{in}^2} = \frac{8KT}{3}\frac{1}{g_{M1}}\left[2 + \frac{4g_{M3}}{g_{M1}} + \frac{2g_{M7}}{g_{M1}} + \frac{2g_{M0}}{g_{M1}}\right] \times \Delta f \quad (3)$$

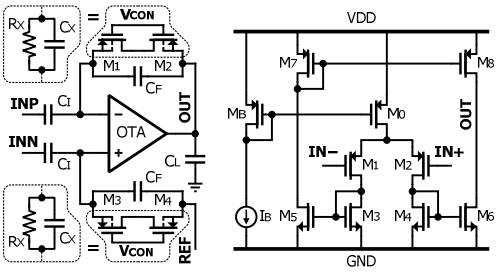

Figure 2. Schematic diagrams of (a) the LNA and (b) the OTA in the LNA.

The PGA provides a second stage of amplification for each channel, contributing to the ability of the system to accommodate the large dynamic range of the neural signal. The bandwidth of the PGA is 10Hz~30kHz, covering the full range of the LNA. The PGA structure shown in Fig.3(a) is a capacitor feedback circuit with a power efficient OTA of class AB shown in Fig.3(b) [5]. The mid-band gain of the PGA is adjusted by varying its feedback factor. A pseudo-resistor of fixed value regulates the DC biasing points of the PGA. The total mid-band gain of the AFE is 54dB, when the PGA is adjusted to a mid-band gain of 7dB.

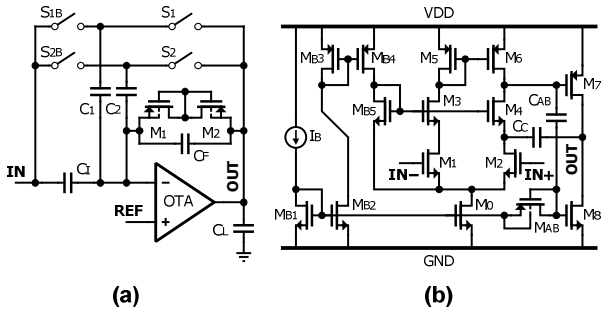

Figure 3. Schematic diagrams (a) of the PGA and (b) of the OTA in the PGA.

B. *Comparator-Based Cyclic ADC*

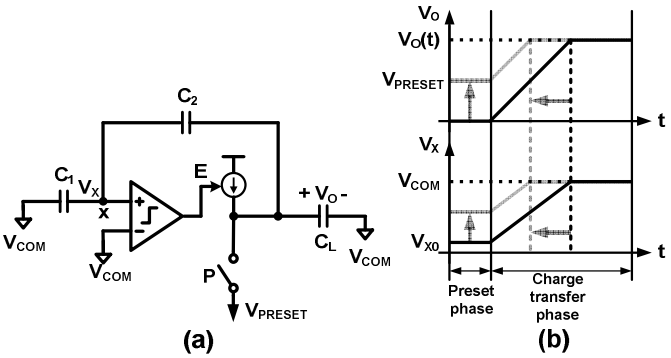

Figure 4. a) Comparator-based switched-capacitor gain stage, and (b) its transient response.

Our system uses a cyclic ADC with a comparator-based switched-capacitor (CBSC) gain stage to digitize the amplified neural signal. We use a cyclic ADC, because it provides good resolution while requiring little power and small area. The CBSC gain stage [6] shown in Fig.4(a) also consumes a little power, because it contains no op-amp; this is replaced by a comparator and a current source. A CBSC gain stage operates in three phases. In the sampling phase, the input signal is sampled on the capacitors C_1 and C_2. During the preset phase, V_{COM} is connected to C_1, V_X starts below V_{COM}, and the output of the stage is connected to the lowest voltage. This pulls V_X low and takes V_{X0} below V_{COM} over the full range of the input voltages. The preset value of the summing node voltage V_{X0} can be expressed as follows:

$$V_{X0} = \left(2 - \frac{C_2}{C_1 + C_2}\right)V_{COM} - V_{IN} \quad (4)$$

In the charge transfer phase, the current source is turned on and it charges up the capacitor network consisting of C_1, C_2 and C_L, creating the ramp waveforms V_O and V_X shown in Fig.4(b). At the end of the charge transfer phase, the voltage V_X is equal to V_{COM}.

A large charging current causes a large overshoot and hence a large offset. The nonlinearity of the output voltage is the product of the change in the ramp-rate and the overshoot voltage. This nonlinearity can be reduced by reducing the overshoot, by introducing a preset scheme.

In Fig.5, to enhance the operation speed, the output node is switched to the preset voltage V_{preset} during the preset phase. V_X starts a higher voltage than V_{X0}. In the subsequent charge transfer phase, the system obtains rough estimates of the output voltage and virtual ground condition.

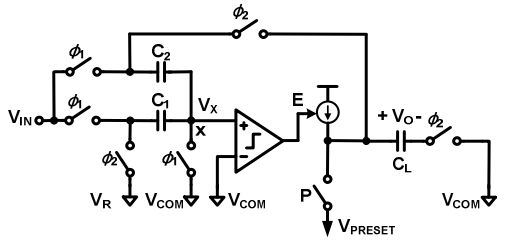

Figure 5. Operation of the CBSC with its preset scheme.

This scheme requires V_X to be calculated from the preset voltage V_{preset} applied at the output node, where V_R is one of the digital-to-analog converter (DAC) voltage levels.

$$V_{X0} = V_{com} + \frac{C_1}{C_1 + C_2} V_R - V_{IN} + \frac{C_2}{C_1 + C_2} V_{preset} \quad (5)$$

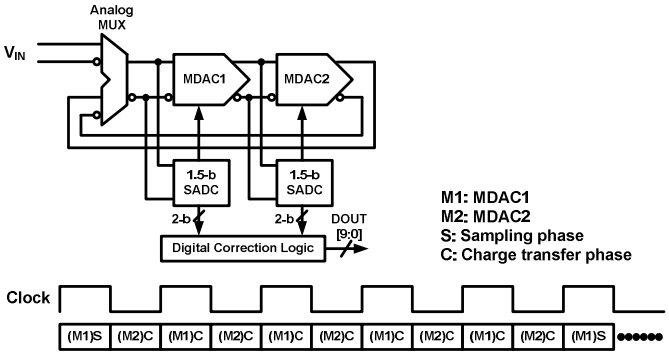

Figure 6. Block diagram and timing diagram of the cyclic ADC.

The cyclic ADC [7], shown in Fig.6, is composed of two multiplying DACs (MDACs), two 1.5-bit sub-ADCs (SADCs), digital correction logic, and a clock generator. At the first clock pulse, MDAC1 samples the analog input signal and transfers the output of MDAC1 to the input of MDAC2 for the subsequent conversion cycle. The charge transfer phase in MDAC2 occurs at the second clock pulse, and then the residual output of MDAC2 is returned to the input of MDAC1. This process is repeated iteratively 5 times. The digital logic recombines the serial output of MDAC1 and MDAC2 to 10-bit digital codes. To reduce the power consumption, a technique similar to amplifier sharing [8] is used to allow a single comparator and current source to be shared between two MDACs.

IV. Experimental Results

We fabricated our 32-channel neural recording system on a chip in 0.18µm standard CMOS with mixed-signal option. Fig.7 shows a microphotograph of the chip. The size of the 32-channel AFE is 1.3mm × 3.5mm. The size of the circuit for each channel is 400µm × 230µm, and the cyclic ADC is 610µm × 240µm. Table I summarizes the performance of the chip at a supply voltage of 1.8V.

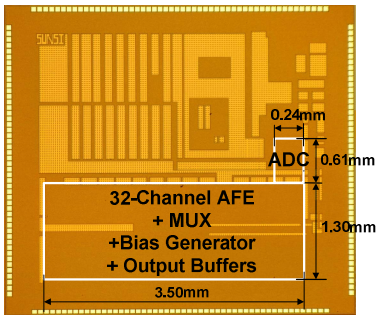

Figure 7. Microphotograph

Table 1. Performance Summary

Technology	**0.18 µm Standard CMOS**
Channels	**32**
Chip Area	**1.3mm x 3.5mm (32-channel) 0.61mm x 0.24mm (cyclic-ADC)**
Supply voltage	**1.8V**
Mid-band gain	**47dB**
Programmable gain	**54~67dB**
High-pass corner frequency	**20~200Hz**
Low-pass corner frequency	**7kHz**
Input referred noise	**11.93µV_{rms}**
Sampling rate/channel	**20kS/s**
ADC ENOB	**7.72 bits**
SNDR	**48.23dB**
SFDR	**53.99dB**
Sampling frequency (Clock frequency)	**2MHz (10MHz)**
Power(AFE+ADC)	**1.26mW+0.74mW=2mW**
Average power/channel	**62.5µW**

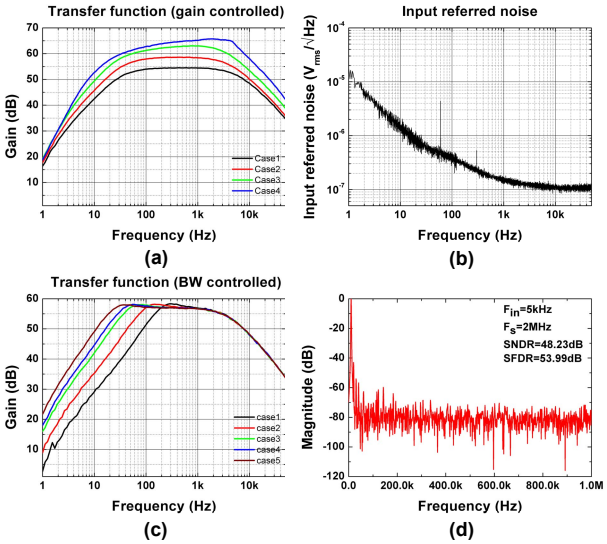

Figure 8 . (a) Transfer function with the PGA in operation, (b) Input-referred noise spectrum, (c) Transfer function with bandwidth tuning, (d)FFT of measured data for a 5kHz sine wave input.

The transfer function with different settings of the PGA is shown in Fig.8(a). The mid-band gain of the LNA is 47dB. Fig.8(b) shows the input-referred noise (IRN) measured using HP 35670A. Integrating the input-referred noise spectrum curve in Fig.8(b) results in a total IRN of 11.93µV_{rms}. Fig.8(c)

shows that the high-pass corner frequency is tunable from 20Hz to 200Hz using the control voltage. As shown in Fig. 8(d), at a conversion rate of 2MS/s, with a 5kHz sine-wave input, the measured signal-to-noise and distortion ratio(SNDR) is 48.23dB and the spurious-free dynamic-range (SFDR) is 53.99dB. The total power consumption of all 32 AFE channels is 1.26mW and the cyclic ADC consumes 0.74mW at a sampling frequency of 2MHz. The low noise amplifier consumes 7.2μW per channel.

Fig.9(a) shows the *in-vivo* recording of neural spikes from the primary somatosensory cortex of a Sprague Dawley rat. The system successfully captured the neural action potential signals shown in Fig.9(b),(c), from a commercial MEA.

We measured the local field potential with tunable bandwidth AFE by a flexible flat-plate LCP probe [9]. The results are shown in Fig.9(d). This probe offers a controllable stiffness and compatibility with the thin-film process, as well as being reliable and biocompatible. Fig.10 shows the information from a neural spike sorted by a MATLAB program. First, the program sets the threshold voltage to detect spike signals. Second, spike signals were averaged out and classified by a sorting algorithm. The program finally shows the firing rates information of the each sorted spike signals on the time domain.

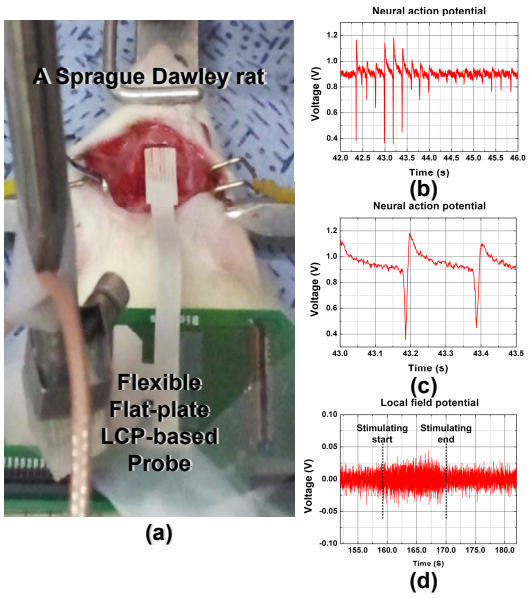

Figure 9. (a) Experimental set-up for in-vivo recording (b) A action potential recorded by a commercial MEA (c) Magnified neural spike (d) Local field potential measured using a LCP-based probe

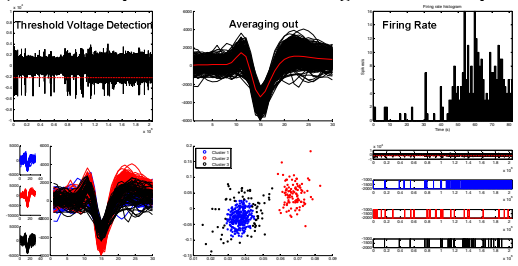

Figure 10. Neural signal sorted by a MATLAB program

V. CONCLUSION

We have presented a neural recording chip consisting of 32 AFE channels and a cyclic ADC. Each channel has tunable bandwidth to accommodate the acquisition of local field potential using a flexible flat-plate LCP probe. The recording channels also have a programmable-gain function to adapt to the large dynamic range of neural signals. The cyclic ADC achieves the necessary conversion speed to allow all the channels to be used. The system has been demonstrated in an *in-vivo* experiment with a flexible flat-plate LCP-based probe as well as with a commercial MEA.

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