INTEGRATION, the VLSI journal 45 (2012) 253–262

Contents lists available at SciVerse ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Static-switching pulse domino: A switching-aware design technique for wide fan-in dynamic multiplexers

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ARTICLE INFO

Available online 3 December 2011

Keywords:
Domino logic
Dynamic circuits
Low-power design
Switching activity
High speed
Noise immunity

ABSTRACT

In wide fan-in dynamic multiplexers, the two phase evaluate-precharge operation leads to high switching activity at the dynamic and the output nodes introducing a significant power penalty. To address this issue, the switching-aware design techniques are being explored but these existing techniques suffer from design inflexibilities. In this paper, we propose a pulse domino switching-aware technique, called SSPD, to reduce the overall power consumption of a wide fan-in dynamic gate by having static-like switching behavior at the dynamic node, and the gate input/output terminals. A conditional pulse generator is also proposed, which enables the SSPD multiplexers to be easily adapted to a wide set of noise and delay specifications. Simulation results of 8-bit and 16-bit dynamic multiplexers designed and simulated in a 1.2-V 90-nm CMOS process show that the SSPD technique can reduce the average power by up to 21% and 36%, respectively, when compared to the conventional footless domino technique.

1. Introduction

High-performance and compact dynamic circuits are frequently employed to implement wide-OR gate structures in decoders, comparators, L0 caches and register files [1–3]. These dynamic circuits employ a dual-phase domino logic style with each clock cycle divided into a precharge and an evaluate phase. This mechanism permits high-speed operation and enables the implementation of complex functions with a single NMOS evaluation network. As an example, a simple implementation of a dynamic multiplexer employed in the read port of a register file is shown in Fig. 1 [2].

Although fast and compact, wide fan-in dynamic circuits suffer from several limitations. Cumulative leakage from the parallel evaluation paths renders the gate susceptible to several charge-loss mechanisms severely compromising the gate's tolerance to input noise [4,5]. While keeper upsizing is a straightforward option for increasing robustness to noise, it is no longer considered viable due to large performance overheads [6]. Therefore, several alternative techniques for dynamic multiplexers have been proposed to improve the noise immunity [7–9]. In addition to low noise immunity, wide fan-in dynamic multiplexers also suffer from excessive power dissipation; however, this problem has not received adequate attention in literature and we introduce it briefly. It is known that static gates consume power only when a toggling event occurs at the output. In other words, the switching power of a static gate is output-switching dependent but that of dynamic gates are output state-dependent, consuming power in every clock cycle where the output is logically high during the evaluation phase [10]. In Fig. 1, we see that the output and the dynamic nodes are reset during every precharge phase even when the logical output value across two consecutive cycles are unchanged. This power penalty due to redundant switching becomes especially significant for wide fan-in gates where the dynamic node with a high capacitance (due to the large parasitic contribution from the evaluation network and the interconnect loading) has a high switching factor. Note that higher fan-in increases the probability of one of the inputs to be in the logic high state at the start of evaluation. Therefore, these considerations motivate an exploration of design techniques to mitigate the problem of redundant switching in dynamic multiplexers [11].

In this paper, we propose a switching-aware design technique for a dynamic multiplexer, which minimizes redundant switching at the dynamic and output nodes thereby achieving static-like behavior. In Section 2, we review previous switching-aware design techniques and discuss their limitations. In Section 3, we introduce and analyze the proposed static-switching pulse domino (SSPD). In Section 4, we provide the simulation results and conclude the paper in Section 5.

2. Previous works

Recently, so-called switching-aware design techniques have been proposed to remove the problem of excessive switching in

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doi:10.1016/j.vlsi.2011.11.013

dynamic domino circuits. In [12,13], a new class of logic family called the limited switch dynamic logic (LSDL) was proposed to exploit the performance and area savings of dynamic circuits while avoiding the excessive dynamic power penalty. A basic wide fan-in implementation of an LSDL gate [14] is shown in Fig. 2(a). The gate has a pull-down network similar to a footed conventional domino gate but the output inverter and the keeper transistor of domino logic, which together form a half-latch, is now replaced by a static latch structure (M3, M4). An additional gain stage (M2, M6) is added to prevent back-propagation of the latched signal to the dynamic node, which precharges every clock cycle. The insertion of the static latch eliminates redundant switching at the output but the internal dynamic node, with a large capacitive loading, still has an enhanced switching rate. Thus, LSDL fails to provide a truly static switching behavior.

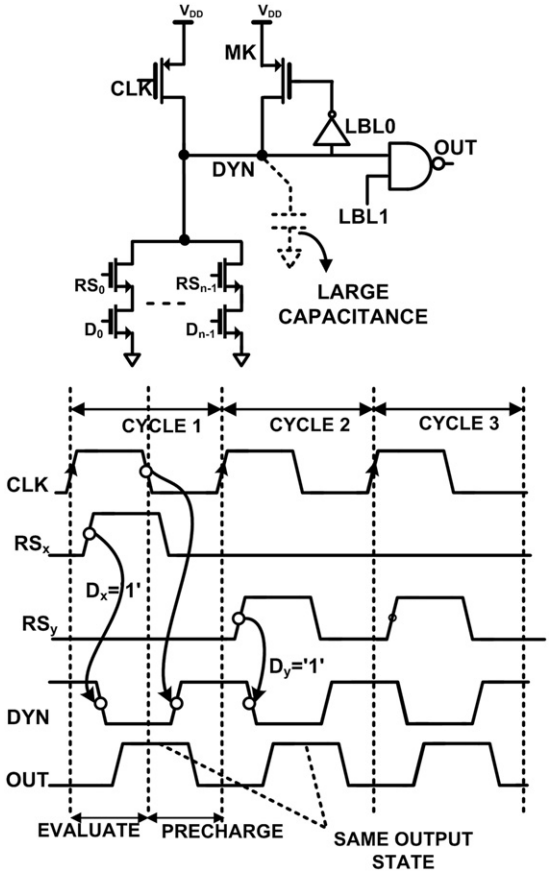

Fig. 1. Local bit-line (LBL) organization of the read port of a register file (RF) using a conventional n-bit footless dynamic multiplexer with its input and output switching waveforms. $RS_x - RS_y$ and $D_x - D_y$ are two row-select and data inputs, respectively.

To achieve static input/output characteristics, a domino technique was proposed in [10] called the single phase SP-Domino (Fig. 2(b)). Similar to clock-delayed domino [15], it uses a delayed clock requiring the latest arriving input to arrive with or before the rising edge of the delayed clock. The gate has a single phase operation as both the pull-up and pull-down of the dynamic node occurs during the evaluation phase. A pMOS transistor, M1, functions both as the keeper and the pull-up device. A pulse-generator block turns on M1 unconditionally at the start of every evaluation cycle. If the pull-down network is on, then a small contention period ensues between M1 and the pull-down network, which are both simultaneously on for the duration of the pulse P at the gate of M1 (equal to the delay of three inverters and the NAND gate of the pulse-generator block). The stronger pull-down network overpowers M1 and the dynamic node is either maintained at or transitions to the low logic state. Alternatively, if the pull-down network is off at the start of evaluation, M1 evaluates the dynamic node to the high logic state. If at the end of the pulse window, the dynamic node is in logic state '0', M3 remains turned off and P is pulled up high (see Fig. 3) by the action of M2 turning off M1. If, however, the dynamic node has been charged up enough to turn-on M3, the charging operation can continue even after the pulse window has elapsed. The logical expression for pulse P is

$$P = \overline{CLK \cdot CLK_i + DYN} \tag{1}$$

where CLK and CLK_i are, respectively, the clock signal and its delayed inverse.

However, the design of SP-Domino suffers from several limitations. Consider the lack of flexibility in sizing M1. Increasing the size of M1 increases the keeper ratio (K, defined as the ratio of the average current drivability of the keeper transistor to that of a single evaluation path of the wide pull down network [8]) and this in turn increases the low-to-high transition delay (T_{rise}) due to the increased contention while decreasing the high-to-low transition delay (T_{fall}). To have symmetric rise and fall delays, SP-Domino requires a fixed K value and the gate cannot be tuned for a specific delay or noise performance. Fig. 4 presents the

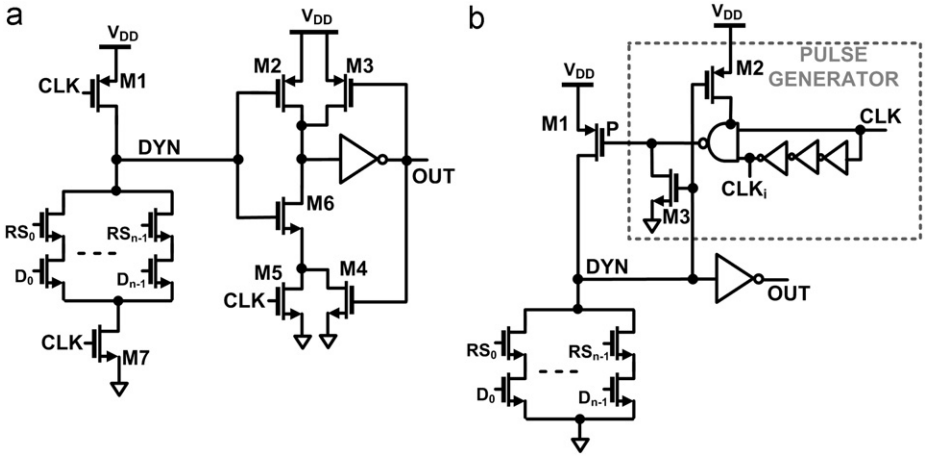

Fig. 2. Wide fan-in dynamic multiplexers using (a) Limited switch dynamic logic (LSDL) [13] and (b) Single-phase SP-Domino [10].

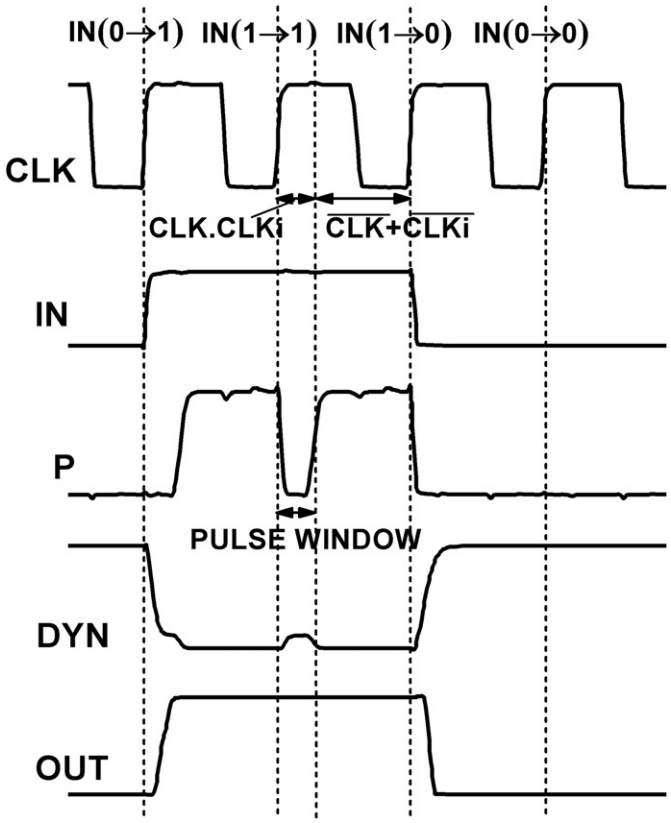

Fig. 3. Simulated waveforms of a 16-bit dynamic multiplexer in 1.2 V 90-nm industrial CMOS process using the SP-Domino technique.

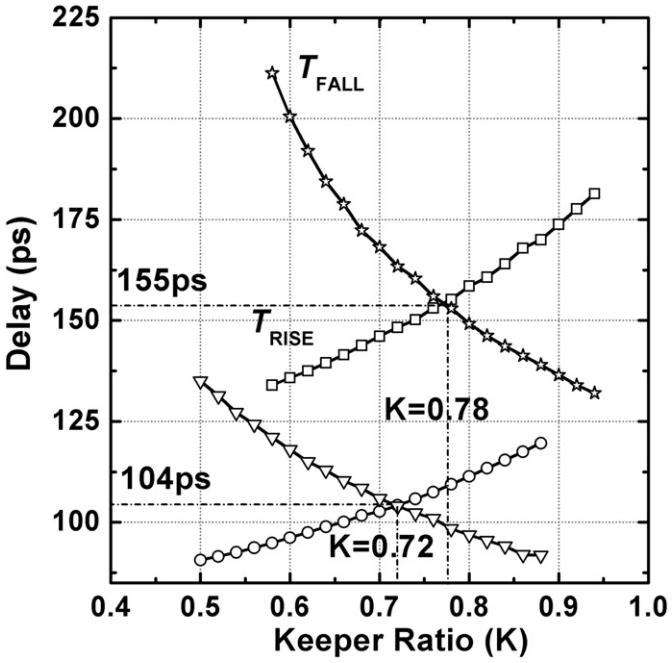

Fig. 4. Rise and fall delays of 8- and 16-bit SP-Domino dynamic multiplexers with an output load of 2 fanout-of-4 inverters (2FO4).

delays of 8-bit and 16-bit SP-Domino multiplexers. In addition, M1 should also be sized large enough to ensure that M3 turns-on before the end of the pulse window. This further restricts K to high values (0.78 for 16-bit, 0.72 for 8-bit multiplexer) and fixes the delay and noise design points at a single value.

However, reduced switching at the dynamic node and the gate output terminal saves a lot of power. This power advantage can be better understood by first considering the switching power of a conventional dynamic multiplexer [10]:

$$P_{Dyn,Conv} = P_{Switching} + P_{SC} + P_{CLK}$$
$$= P_{OUT}(1)C_{DYN}V_{DD}^2 f_{CLK} + P_{OUT}(1)I_{SC}V_{DD}f_{CLK} + P_{CLK}, \quad (2)$$

where $P_{Switching}$ is the power dissipated due to the charging and discharging of the large dynamic node capacitance C_{DYN} (Here we neglect the contribution to switching power from other node capacitances). P_{SC} is the average short-circuit current due to keeper action that flows in every cycle in which the output is in the logic high state (an event with probability $P_{OUT}(1)$). P_{CLK} is the clocking power overhead. Now, the power consumption of an SP-Domino can be written as:

$$P_{Dyn,SPDo} = P_{Mux} + P_{CPG} + P_{SC} + P_{CLK}$$
$$= \frac{1}{2}\alpha C_{DYN}V_{DD}^2 f_{clk} + P_{CPG} + P_{OUT}(1)I_{SC}V_{DD}f_{clk} + P_{CLK}. \quad (3)$$

Here, α is the switching probability of the gate output. Comparing (2) and (3), we observe that the SP-Domino gate consumes switching power only when the output switches; this limited switching at dynamic and output nodes leads to large power savings [10]. Eq. (3) further shows that the gate draws some power (due to contention) even when the output is stable at logic high state. This is because M1 is unconditionally turned on at the rising edge of every clock.

In conclusion, we see that the SP-Domino technique is heavily disadvantaged by the use of the same transistor to perform both the pull-up as well as the keeper action. While a static-like switching behavior renders it advantageous in terms of power, it is inflexible and has significant design overheads.

3. Proposed static-switching domino technique

3.1. SSPD design

In this section, we introduce the static-switching pulse domino (SSPD) technique to remove the limitations of the SP-Domino scheme imposed by its inflexible design. The schematic and the simulation waveforms of the proposed SSPD scheme applied to a 16-bit dynamic multiplexer are shown in Figs. 5 and 6, respectively. Similar to an SP-Domino gate, the SSPD technique has a clock-delayed footless operation with static input and output characteristics. However, to avoid the several design constraints imposed by the use of the same transistor (M1 in Fig. 2b) to perform both the pull-up and keeper action, SSPD employs separate transistors, M1 and M2. The use of two separate transistors is based on the simple observation that during a pull-up operation, keeper action is not required and when the keeper is required, the pull-up operation should be disabled. In the SSPD scheme, M1 and M2 are therefore never on simultaneously and during an evaluation, only M1 or only M2 are turned on with the other being off. Thus, while a SP-Domino multiplexer's rise and fall delay is affected by the size of a single transistor, SSPD allows independent tuning of rise and fall delays. M1 is on during the low-to-high transition on the dynamic node and thus affects only the multiplexer's fall delay. Similarly, M2 is on only during the high-to-low transition on the dynamic node and affects only the multiplexer's rise delay. The keeper ratio (K) still determines the multiplexer's noise

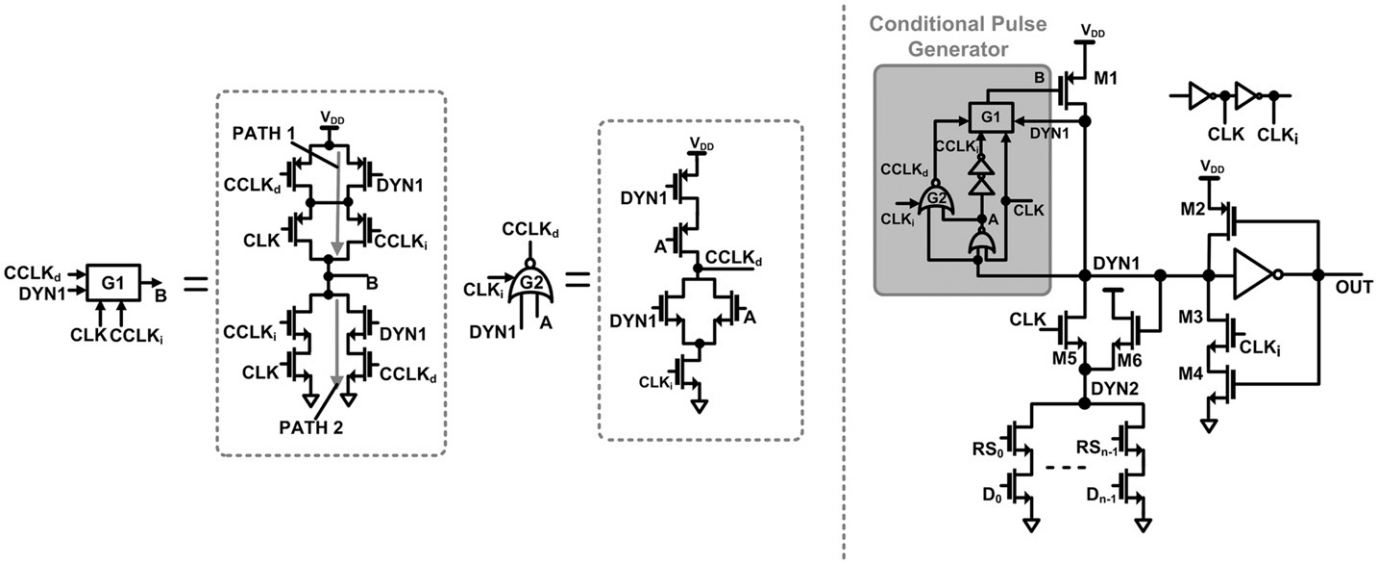

Fig. 5. Dynamic multiplexer implemented with the SSPD technique. G1 and G2 are the two gates of the pulse generator.

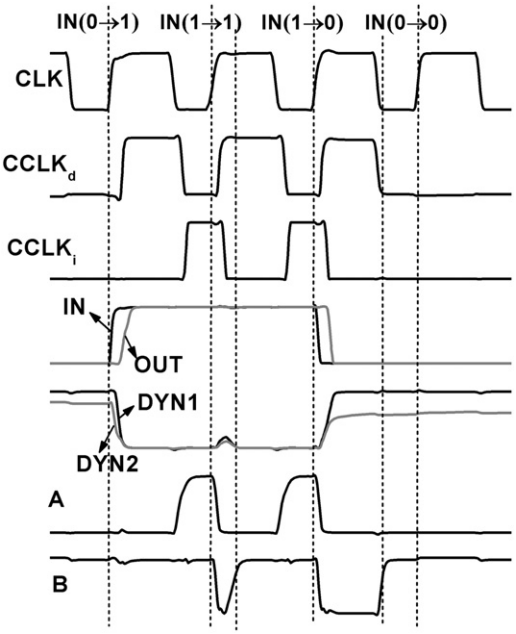

Fig. 6. Simulated waveforms of a SSPD 16-bit dynamic multiplexer.

robustness but for characterizing the delay signature, both K as well as the size of M1 requires simultaneous consideration.

As discussed previously, SP-Domino has a conventional pulse generator, which generates a pulse unconditionally at the start of every evaluation phase. This would however fail to provide the required exclusivity between the operation of M1 and M2. Therefore, the SSPD scheme employs a conditional pulse generator (CPG) shown in Fig. 5. The role of the CPG is to generate a pulse, and hence turn on M1, only when the dynamic node has been discharged or held low in the previous evaluation cycle. Notice that only in these cases, the keeper transistor M2 is off and a low-to-high evaluation is probable on the dynamic node. On the other hand, if the dynamic node has not been discharged, M1 is not turned on by the CPG. Now, if the pull-down network is on, it faces contention only from the keeper transistor M2.

To achieve the conditional mode of operation, the CPG monitors the dynamic node to internally generate two additional clock phases, $CCLK_d$ and $CCLK_i$. Their behavior in relation to the clock signal (CLK) and the dynamic node is illustrated in Fig. 6. $CCLK_d$ and $CCLK_i$ are, respectively, the conditionally generated delayed and inverse phases of the original clock signal CLK. The two phases are utilized by the gate G1 of the CPG to generate the pulse signal B, where the logical expression of G1 is

$$B = \overline{(CLK \times CCLK_i) + (DYN1 \times CCLK_d)}. \quad (4)$$

From Fig. 6, we see that the two phases behave as the delayed and delayed inverse phase of the clock only when the dynamic node is low; but, when the dynamic node is evaluated high and a pulse is not required during the next evaluation phase, both the clock phases are pulled down to the low logic state. From expression (4), we see that when both $CCLK_d$ and $CCLK_i$ are low, B remains high and no pulse is generated. This conditional behavior of the two clock phases can be easily achieved by a NOR operation between the clock signal and the voltage of the dynamic node.

The final design change is the introduction of a clocked isolation transistor M5 to separate the drain terminal of the pull-down network with large capacitive loading (DYN2) from the main dynamic node (DYN1), which is inversely coupled to the output. The purpose of the isolation transistor in the SSPD gate is to shield the large parasitic capacitance at DYN2 (due to the wide pull-down network) from M1 during a pull-up operation. Consider a situation where both DYN1 and DYN2 have been discharged to logical ground in the previous evaluation cycle (see Fig. 6). At the start of the next clock cycle, if the pull-down network is off, the pull-up transistor M1 will evaluate DYN1 to the logical high state. Contrary to the case in an SP-Domino gate where the pull-up device has to be adequately sized to charge the large capacitance on the dynamic node, most of M1's initial current drive will be utilized to quickly charge up the much smaller capacitance on DYN1 as the current drained by the isolation transistor M5 would be limited by its near-zero drain-to-source voltage. Thus, the sizing constraint on the pull-up device to

equalize the high-to-low delay of the gate with its low-to-high delay is now relaxed. In addition, the voltage swing on DYN2 is also reduced by V_{TN} (nMOS threshold voltage) leading to power savings. Note that M6 is only a weak nMOS keeper for the node DYN2; the main keeper action is provided by M2.

3.2. SSPD operation

In this sub-section, we describe in detail the four possible cases of operation in the SSPD multiplexer. The four cases correspond to changes in DYN1 during the evaluation phase where (1) during Case 1, DYN1 is evaluated low from the logic high state, (2) during Case 2, DYN1 maintains the logic low state, (3) during Case 3, it undergoes a low-to-high transition and finally, (4) during case 4, it maintains its logic high state. The waveforms of the important nodes during the four cases are represented in succession in Fig. 6.

Case 1: The dynamic nodes transition from the logic high to the logic low state during the evaluation cycle. Since DYN1 was high during previous evaluation, we see that $CCLK_i$ is zero at the start of the clock cycle and no pulse is generated. The pull-down network is on, and therefore DYN1 is evaluated to the logic low state facing contention only from the keeper transistor M2. The situation is depicted in Fig. 7. Also notice that after DYN1 goes low, both $CCLK_d$ and $CCLK_i$ resume behaving, respectively, as the delayed and the delayed inverse phases of the original clock.

When DYN1 is discharged to the logic low state, a special case of clock feedthrough arises at the high-to-low transitions of the clock. Conventionally, the keeper transistor forms only a half-latch with the output inverter. Thus, when a high-to-low transition of the clock causes the lightly-loaded dynamic node DYN1 to fall below zero (logic low state) due to the capacitive coupling from the clock input to M5, no discharge path is available from DYN1 for the injected charge. Therefore, as shown in Fig. 5, transistors M3 and M4 are added. The additional path through M3 and M4, which is activated when both DYN1 and clock are low, drains away the excessive charge, and the undesirable effects of capacitive feedthrough can thus be avoided.

Case 2: This case corresponds to the situation when the dynamic node maintains its low logic state from the previous evaluation, and is depicted in Fig. 8. At the start of evaluation, *B* goes low, turning on M1. However, since the pull-down network is also on, a small contention period, which is the sum of the delays of the NOR gate and the two inverters in the CPG of Fig. 5, ensues between M1 and the pull-down network after which *B* goes high again. Since the transistors in the pull-down network are sized to be stronger than M1, the dynamic nodes are only slightly disturbed but do not change their states. The short-circuit (or contention) power expended in this situation however imposes an upper bound on the size of M1; it should be high enough to achieve the required high-to-low delay of the multiplexer but small enough to prevent the contention power from overriding the benefits of a static switching factor. Further, for a large M1 size, the disturbance on the dynamic nodes during the contention period increases, possibly leading to an erroneous evaluation.

An analogous case for a dynamic multiplexer is when the inputs are high in two consecutive cycles. Thus, the dynamic node, which has been evaluated low in the previous cycle, will undergo a redundant evaluation in the present cycle due to the intermediate precharge phase. While the short-circuit power can be considered the overhead of the SSPD scheme, the analogous overhead for a dynamic multiplexer is the switching energy expended during the precharge-evaluation operations across consecutive cycles. Therefore, as long as the short-circuit power

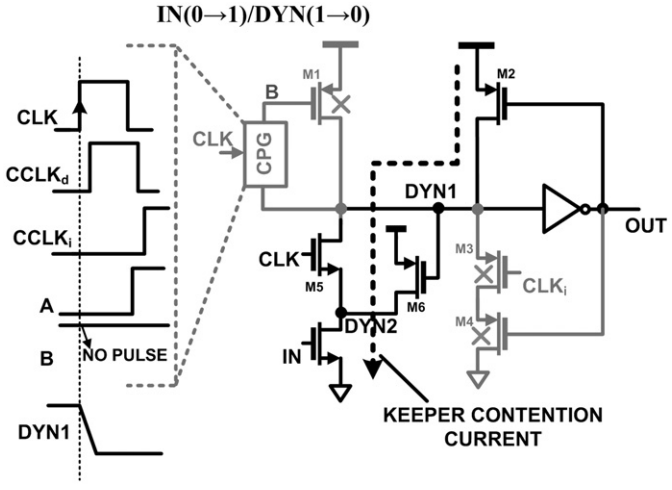

Fig. 7. Operation of the SSPD multiplexer when the dynamic nodes are evaluated from the logic high to the logic low state during the evaluation cycle. The pull-down network is represented by a single nMOS transistor.

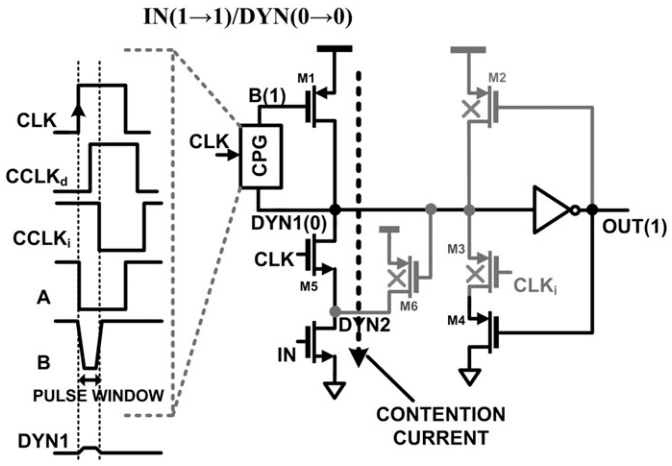

Fig. 8. Operation of the SSPD multiplexer when the dynamic nodes maintain the logic low state during the evaluation cycle.

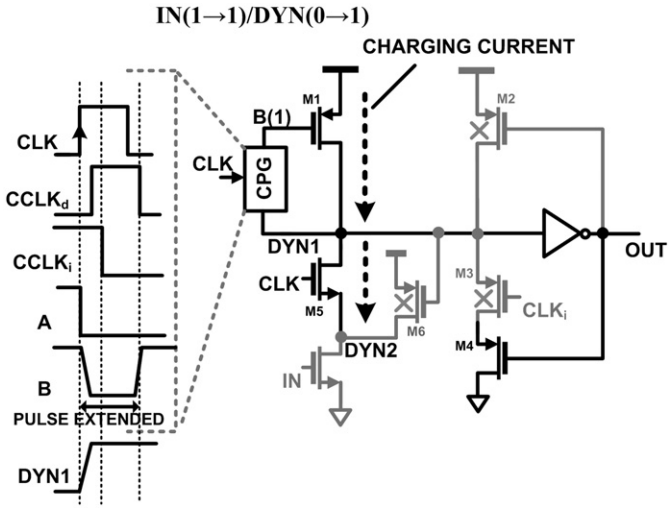

Fig. 9. Operation of the SSPD multiplexer when the dynamic nodes are evaluated from the logic low to the logic high state during the evaluation cycle.

of the SSPD multiplexer remains much smaller than the switching power of the conventional multiplexer, SSPD will always hold an advantage in power for high values of $P_{OUT}(1)$ (probability of the output, and hence the input, to be in the logic high state).

Case 3: This case, depicted in Fig. 9, corresponds to the situation when the dynamic node transitions from the logic low to the logic high state during the evaluation cycle. Notice that since M2 and the pull-down network is off, the speed of the evaluation is dependent only on M1.

During the pull-up operation, the CPG generates a pulse that is wide enough to span the on-period of the clock. This is made possible by the action of $CCLK_d$. As DYN1 is evaluated high, both $CCLK_d$ and $CCLK_i$ should be pulled low, but due to the gated pull-down path in gate G2, $CCLK_d$ transitions low only at the next negative edge of the clock. Thus, rising voltage on DYN1 turns on the discharge path 2 and turns off path 1 in gate G2 (see Fig. 5), and *B* remains low. At the next negative edge of *CLK*, as $CCLK_d$ goes low, the discharge path is deactivated and *B* is pulled high. The pulse-width extension ensures that M1 is not turned off before the pull-up operation is completed, and also relaxes its sizing requirement.

Case 4: When the dynamic node maintains the logic high state, no charging/discharging currents are present at the dynamic node. The situation is depicted in Fig. 10.

3.3. SSPD power

If we consider only the dynamic node capacitances, the switching power of an SSPD multiplexer can be written as

$$\begin{aligned} P_{Dyn,SSPD} &= P_{Mux}+P_{CPG}+P_{SC}+P_{CLK} \\ &= \left[\frac{1}{2}\alpha C_{DYN1}V_{DD}^2 f_{CLK}+\frac{1}{2}\alpha C_{DYN2}(V_{DD}-V_{TH,N})V_{DD}f_{CLK}\right] \\ &\quad +P_{CPG}+P_{Out}(1)I_{SC}V_{DD}f_{CLK}+P_{CLK}. \end{aligned} \tag{5}$$

Assuming $V_{DD}-V_{TN}\approx 0.75V_{DD}$, (5) reduces to

$$P_{Dyn,SSPD}\approx \frac{1}{2}\alpha\left[C_{DYN1}+\frac{3}{4}C_{DYN2}\right]V_{DD}^2 f_{CLK}+P_{CPG}+P_{SC}+P_{CLK}, \tag{6}$$

where P_{Mux} and P_{CPG}, respectively, are the power dissipated in the dynamic multiplexer and the pulse generator. α is the switching probability of the input and output terminals. Comparing (6) with (3), we see that the SSPD's capacitive power is different from that of SP-Domino in that the capacitive contribution from the main dynamic node (the drain terminal of the evaluation network transistors) is now reduced due to the smaller voltage swing ($V_{DD}-V_{TN}$). Additionally, P_{CPG} is now output-state dependent: when DYN1 is held high and the output is low, all nodes in the CPG remain static and do not switch. We expect the above two factors to offset the increase in power consumption of the SSPD multiplexer due to the overhead of the generation of the two additional local clock phases $CCLK_d$ and $CCLK_i$.

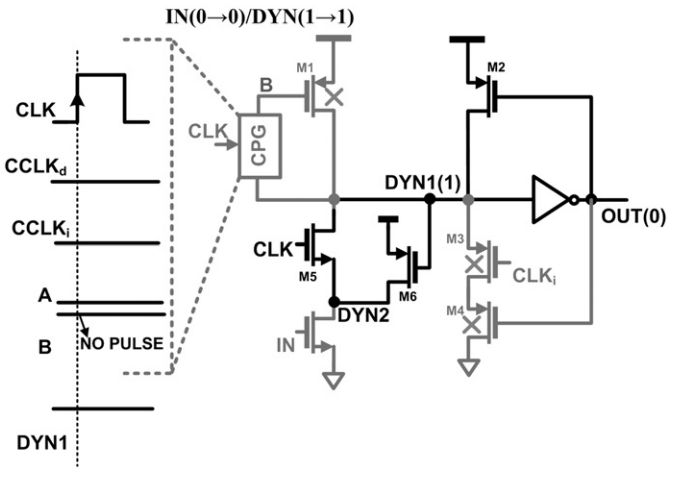

Fig. 10. Operation of the SSPD multiplexer when the dynamic nodes maintain the logic high state during the evaluation cycle.

3.4. Sizing methodology

Based on the description of the SSPD operation in the previous sub-sections, it is easy to see that the design of an SSPD multiplexer can be accomplished in two simple steps. In the first step, to meet a particular noise and delay target, the keeper transistor M2 is sized thereby achieving a particular keeper ratio. In the second step, M1 is sized to equalize the multiplexer's high-to-low transition delay with its low-to-high transition delay, determined by *K*. Note that the two steps are independent and affords the designer the flexibility of designing for a wide set of specifications. Fig. 11 shows the M1–M2 width and the delay and Unity Noise Gain (UNG) values for 8-bit and 16-bit SSPD multiplexers for keeper ratios between 0.3 and 1. UNG is defined as the amplitude of input noise, which causes the same amplitude of noise at the output [8], and is determined at the worst case-leakage corner (fast NMOS, slow PMOS at 110 °C). The noise pulse width is fixed at the approximate rise/fall time of a fanout-of-4 inverter (FO4) in 90-nm technology ($\approx$ 50 ps). The size of all transistors in the evaluation network is fixed at 2 μm.

In order to understand the effect on the SSPD multiplexer's performance of the pulse width, which is the sum of the delays of the two inverters and the NOR gate in the CPG, we carry out simulations for two pulse widths of 120 ps and 160 ps. We observe that for a smaller pulse width of 120 ps, the sizing requirement of M1 increases on an average by 12% and 25% for the 8-bit and 16-bit multiplexers, respectively. This is expected because when the pulse width is shortened, the current drive of M1 must proportionally be increased to charge up DYN1 sufficiently to turn on path 2 (refer Case 3 in Section 3.2) before the end of the pulse window.

SSPD multiplexers with very wide fan-ins, say a 32-bit multiplexer, must be implemented as two 16-bit sections each with its own pull-up transistor and pulse generator, and with a final NAND-merge at the output [16,17]. This is necessary because for multiplexers with very wide fan-in, the large dynamic node capacitance would mandate a large M1 to equalize the multiplexer's rise and fall delays. This requirement, besides increasing the disturbance on the dynamic node during case 2, can override the benefits of static behavior rendering the design unfeasible in terms of power. A large M1 is also required for 8-bit and 16-bit SSPD multiplexers with keeper ratios less than 0.4, and hence is not simulated.

4. Simulation results

We simulated 8-input and 16-input footless dynamic multiplexers in a 1.2 V 90-nm industrial CMOS process. The average power consumption for different output state probabilities of an SP-Domino multiplexer, optimized for equal rise and fall delays, is compared with the conventional footless domino and SSPD multiplexers under equal-UNG (same noise robustness) condition. To account for the overhead of clocked transistors, the power consumption of the local clock buffer is included in the power measurements. The evaluation transistors of the pull-down network and the output inverter are sized equally for all three designs. The pulse width of the SP-Domino and SSPD multiplexers

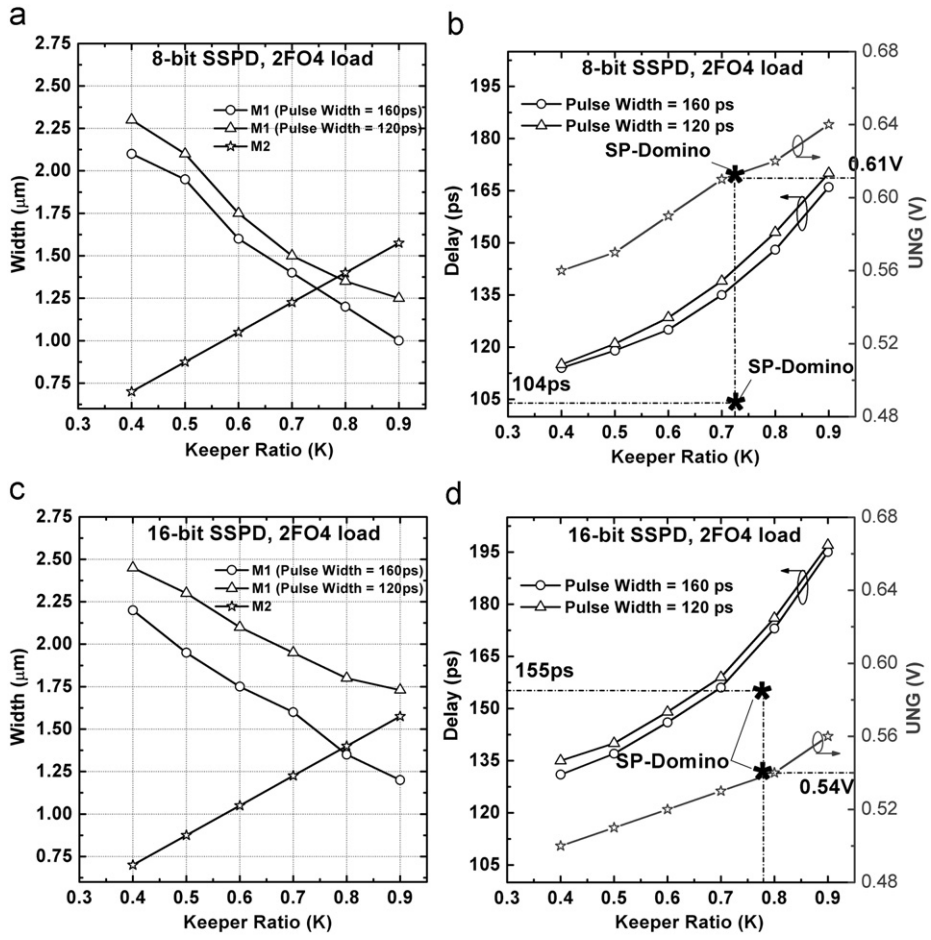

Fig. 11. (a) M1–M2 width; (b) delay and UNG of a 8-bit SSPD multiplexer (with 2FO4 load) with different keeper strengths; (c) M1–M2 width; (d) delay and UNG of a 16-bit SSPD multiplexer (with 2FO4 load) with different keeper strengths.

Table 1
Values of switching factor α for different values of $P_{OUT}(1)$.

$P_{OUT}(1)$	Switching factor	
	Conventional	SP-Domino, SSPD
0.1	0.2	0.2
0.2	0.4	0.4
0.3	0.6	0.6
0.4	0.8	0.8
0.5	1	1
0.6	1.2	0.8
0.7	1.4	0.6
0.8	1.6	0.4
0.9	1.8	0.2

is kept constant at 160 ps. All measurements are done using a 1 GHz clock with 50% duty cycle. Simulations are done by varying the output state probability $P_{OUT}(1)$ between 0.1 and 1. For each value of $P_{OUT}(1)$, the input to the dynamic multiplexer is chosen to obtain the maximum switching factor (or switching probability). As an example, for $P_{OUT}(1)$ equal to 0.5 in the SSPD and SP-Domino multiplexers, when α can assume a value of either 0.2 or 1, the input is varied to have an α value of 1. Similarly, α is 0.2 for $P_{OUT}(1)$ equal to 0.1 and 0.9, and 0.4 for $P_{OUT}(1)$ equal to 0.2 and 0.8 and so on. On the other hand, for conventional domino multiplexers, the switching factor is always double the value of $P_{OUT}(1)$. α and $P_{OUT}(1)$ values are shown in Table 1.

Fig. 12 presents the power results of 8-bit and 16-bit multiplexers with 2FO4 and 4FO4 loads. It is seen that when $P_{OUT}(1)$ is less than 0.5, the same-UNG conventional multiplexers outperforms both SSPD and SP-Domino. However, the power advantage due to the static-switching behavior becomes apparent for output state probabilities greater than 0.5. For equal noise robustness and $P_{OUT}(1)$ greater than 0.5, SSPD gate offers as much as 21% power reduction for a 2FO4 load and around 36% power reduction for a 4FO4 load when compared to the conventional domino multiplexer. Notice that when $P_{OUT}(1)$ is less than 0.5, α is greater than $P_{OUT}(1)$, but starts decreasing for larger values of $P_{OUT}(1)$. Since the capacitive power consumption of an SSPD gate is dependent on α (see (5)), this leads to a power advantage for biased output states ($P_{OUT}(1) > 0.5$). This is a significant advantage as wide fan-in multiplexers usually have high values of $P_{OUT}(1)$ [10]. Further, notice that although the α values are same for $P_{OUT}(1)$ equal to 0.2 and 0.8, the power demand of the SSPD multiplexer in the latter case is higher due to the larger power consumption by the pulse generator and contention currents, which are dependent on $P_{OUT}(1)$. From (5), we can also infer that as $P_{OUT}(1)$ increases beyond 0.5, α decreases and so does P_{Mux}, but the contribution from P_{CPG} and P_{SC} to the overall power increases. The two effects tend to offset each other resulting in nearly constant power dissipation. We also observe that due to the static switching factor, the power advantage of the SSPD scheme over the conventional design increases with larger output loads and wider fan-ins.

In Fig. 13, the variation of average power of the SSPD multiplexers against $P_{OUT}(1)$ for different keeper ratios is shown. For

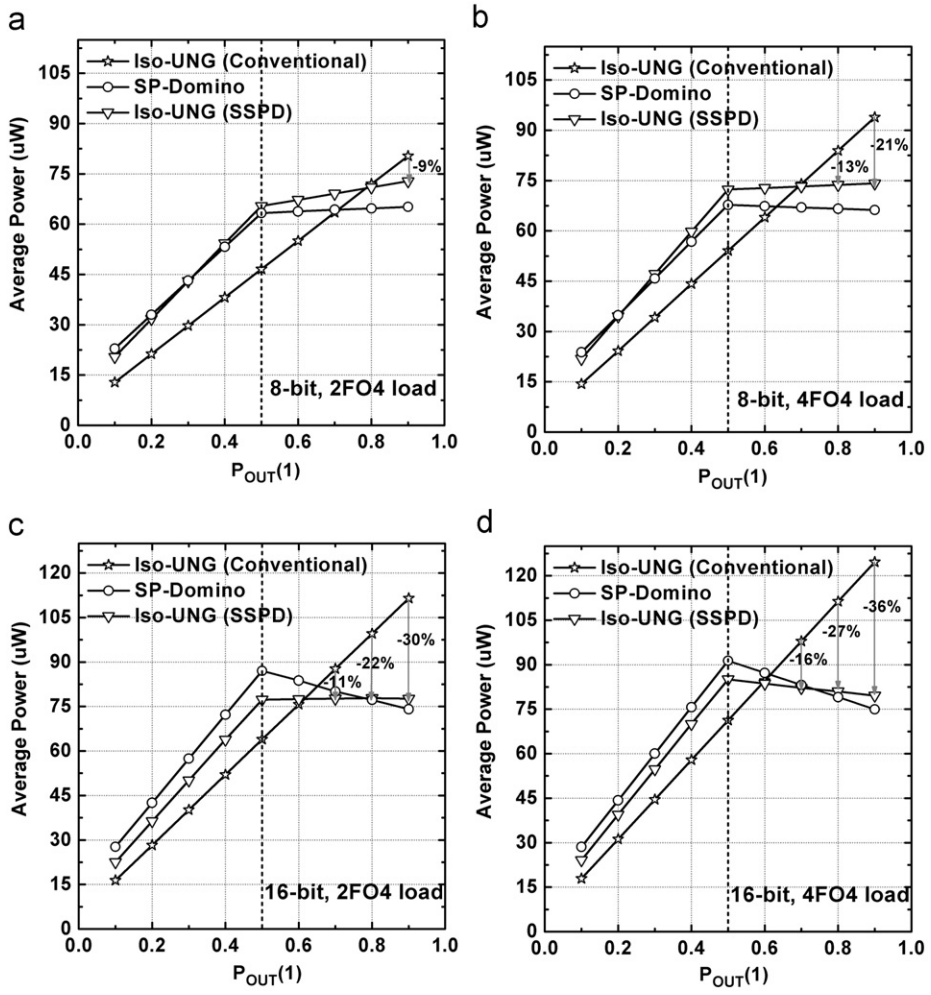

Fig. 12. Variation of average power of dynamic multiplexers against $P_{OUT}(1)$ for (a) 8-bit operation with 2FO4 inverter load, (b) 8-bit operation with 4FO4 inverter load, (c) 16-bit operation with 2FO4 inverter load and (d) 16-bit operation with 4FO4 inverter load. $P_{OUT}(1)$ is the probability of output to be in the logic high state.

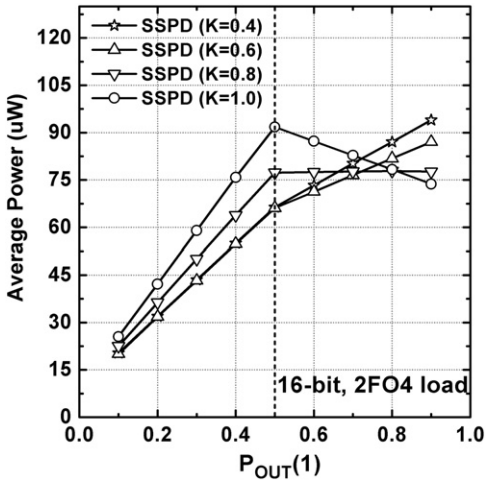

Fig. 13. Variation of average power of a 16-bit SSPD multiplexer against $P_{OUT}(1)$ for different keeper ratios.

lower output state probabilities, contention due to M2 is more dominant, and since the size of M2 increases with increasing K (see Fig. 11), the average power also follows an increasing trend. On the other hand, for higher output state probabilities, the average power is dominated by contention due to M1. This contention power at a fixed value of $P_{OUT}(1)$ is dependent only on M1's size, which, as shown in Fig. 11, decreases with increasing K. Therefore, for $P_{OUT}(1) > 0.5$, average power also follows a decreasing trend with increasing K.

The power performance of SP-Domino is marginally better ($\sim$7% with 2FO4 load and $\sim$9% with 4O4 load) than the SSPD gate for 8-bit multiplexers (see Fig. 12(a) and (b)). This can be explained by the use of a simpler pulse generator (PG) in the SP-Domino scheme. As shown in Fig. 14, SP-Domino's PG power consumption does not vary significantly for different values of $P_{OUT}(1)$. However we see that SSPD PG's power consumption increases rapidly with $P_{OUT}(1)$, consuming on an average $\sim$58% more power than the SP-Domino PG. For 16-bit multiplexers however, the SSPD and SP-Domino multiplexers have similar average power. Thus, despite the larger PG power, the SSPD and SP-Domino multiplexers have similar power performance in general; this can be attributed to the power savings from the reduced swing of the DYN2 node in the SSPD scheme.

In conclusion, analysis of the simulation results show that while both SP-Domino and SSPD techniques offer significant power reductions over the conventional domino multiplexer for biased output states ($P_{OUT}(1) > 0.5$), the design of the SSPD multiplexer has the important advantage of being easily modifiable for a particular delay or noise performance. However, these

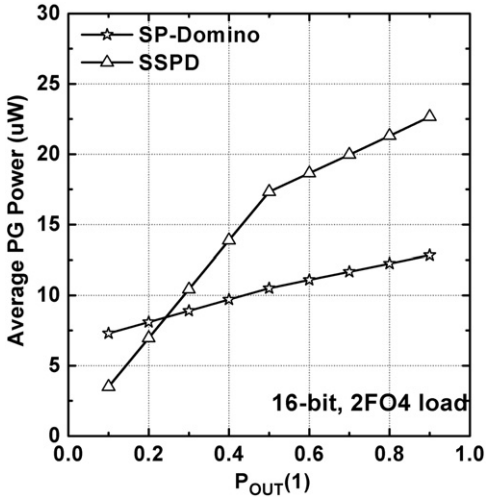

Fig. 14. Variation of average power consumed by the pulse generator block in 16-bit SPD and SP-Domino multiplexers against $P_{OUT}(1)$.

Table 2
Comparison of delay distribution and average power ($P_{OUT}(1)=0.9$) for 16-bit conventional, SP-Domino and SSPD multiplexers. T_{delay} is the average of the rise and the fall delays.

	Power (μW)	16-bit delay (T_{delay}) (Corner simulations)			16-bit delay (T_{delay}) (Monte Carlo simulations)	
		Min. [ps]	NN 27 °C [ps]	Max. [ps]	μ [ps]	σ [ps]
Conventional (Iso-UNG)	111.5	126.6	157	219.8	156.7	10.8
SP-Domino	74.1	122.7	155	219.6	155.6	10.7
SSPD (Iso-UNG)	77.6	144.2	173.5	247.1	175.3	9.8

improvements in power of the SSPD scheme come at the cost of increase in complexity and area: the SSPD multiplexer requires nearly three times the number of transistors as the conventional dynamic multiplexer (excluding the pull-down network). Further, the requirement of a clock-delayed operation, which would require additional clock delay lines, is also an additional overhead.

The three designs are also analyzed for process variations by performing simulations at three process corners (TT, FF and SS) for three different temperatures (27 °C, 55 °C and 110 °C). Robustness against random variations is tested by performing 1000-point Monte Carlo simulations using industrial-hardware calibrated transistor statistical models. The mean delay (μ) and its standard variation obtained from Monte Carlo simulations and the minimum, nominal and maximum values of the average delay obtained from corner simulations are shown in Table 2. The variation in power is found to be very small and is omitted. The maximum variations in delay of the conventional, SP-Domino and SSPD multiplexer from the nominal under process variations are 53 ps, 55 ps and 74 ps, respectively. Since both the SSPD and domino gates were designed to have a sufficiently wide pulse width to account for variations (160 ps in the present case), the delay spread of both the techniques is similar to that of the conventional scheme and the pulse generator is found to not increase the performance variability.

5. Conclusion

We have examined the significant issue of reducing the switching power of wide fan-in dynamic multiplexers. We propose a static-switching pulse domino technique that utilizes a conditional pulse generator to realize a flexible design, which also has significant power advantages from having a static-switching behavior. We demonstrate that the proposed technique can be easily applied to wide fan-in multiplexers to meet a wide range of delay and noise specifications. Further, we also show that for biased output states, we observe as much as 36% reduction in power at equal noise robustness of wide dynamic multiplexers in 90-nm CMOS technology.

Acknowledgments

This work was financially supported in part by the grant from the Industrial Source Technology Development Program (10033657, 10033812) of the Ministry of Knowledge Economy (MKE) of Korea and in part by Samsung Electronics. The authors also gratefully acknowledge the support of the IC Design Education Center (IDEC), by the provision of CAD tools, and the support of the Inter-university Semiconductor Research Center (ISRC) and Engineering Research Institute.

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