Column readout circuit with dual integration CDS for infrared imagers

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Abstract: A column readout circuit with proposed dual integration CDS for low pattern noise infrared imager is presented. By using an extra integration, the dual integration CDS effectively reduces the level of column and row noise (CN and RN) and column fixed pattern noise (CFPN) in an infrared image. In addition, a time flexible integration technique minimizes the penalty of readout time by a dual operation. Simulation of a $0.18\,\mu\text{m}$ CMOS implementation suggests that CN can be reduced by 68%, RN by 71%, and CFPN by 95% compared with a column readout circuit with conventional CDS.

Keywords: noise, correlated double sampling, column readout circuit, infrared imager

Classification: Integrated circuits

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1   Introduction

Uncooled infrared microbolometer sensors are now used in a wide range of industries such as traditional military market, security, and environment monitoring [1, 2]. Image quality determined by various factors including column noise (CN), column fixed pattern noise (CFPN), row noise (RN), row fixed pattern noise (RFPN), and pixel noise (PN). Pattern noise such as CN, CFPN, RN, and RFPN is more visible than PN and therefore its noise level must be significantly less than that of PN [3]. An infrared imager is more vulnerable to noise than others such as CMOS imager and charge-coupled devices (CCDs) because the column readout circuit needs a considerable gain to amplify the microscopic sensing current and this gain also amplifies the noise.

To reduce the pattern noise, various structures have been proposed. The fully differential structure from a pixel unit is effective to cope with RN and RFPN caused by the noise sources such as power-rail fluctuation, but it cannot reduce CN, CFPN caused by $1/f$ noise and device mismatching at a column readout circuit respectively [4]. Correlated double sampling (CDS) has been a popular solution in especially the CMOS imager and CCDs where the CDS function is essential for reducing $1/f$ noise of source follower and reset noise in a pixel unit [3, 5, 6]. However, it cannot be directly utilized in an infrared imager due to the different structure at the pixel unit and column readout circuit. The CDS function for infrared imager was discussed in [7, 8], but it only reduces $1/f$ noise of an amplifier for integrator that is a part of CN and CFPN. In this paper, we propose a dual integration CDS in order to address all the components of pattern noise in an infrared image. In addition, we analyze contributions of different types of noise considered the characteristics in two-dimensional visual artifact and compare the effectiveness of our circuit with a column readout circuit with a conventional CDS.

2   Types of noise

The generic readout architecture for an infrared imager consists of microbolometer focal plane array (FPA) to detect infrared lights, column readout circuits to convert the change of microbolometer resistance in pixel unit into a voltage level, analog to digital converter (ADC) to convert the voltage level into digital signals, and digital processor to control the readout operation as shown in Fig. 1 [9].

The column readout circuits are the dominant source of pattern noise since they have to be simultaneously performed at a row readout time and placed as column units. In Fig. 2 [7, 8, 9, 10], the sensing current (I_{INT}) is generated by the active microbolometer with a resistance of R_S, blind microbolometers with resistances R_B and R_C. The R_B provides the zero point of I_{INT} through I_B. The R_C with DAC and digital processor calibrates thermally changed resistance R_S other than infrared light
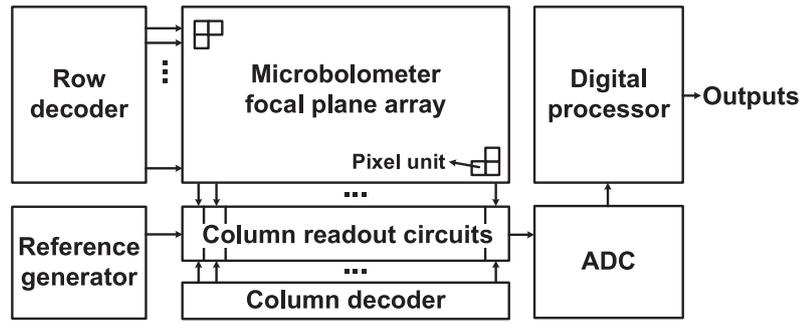
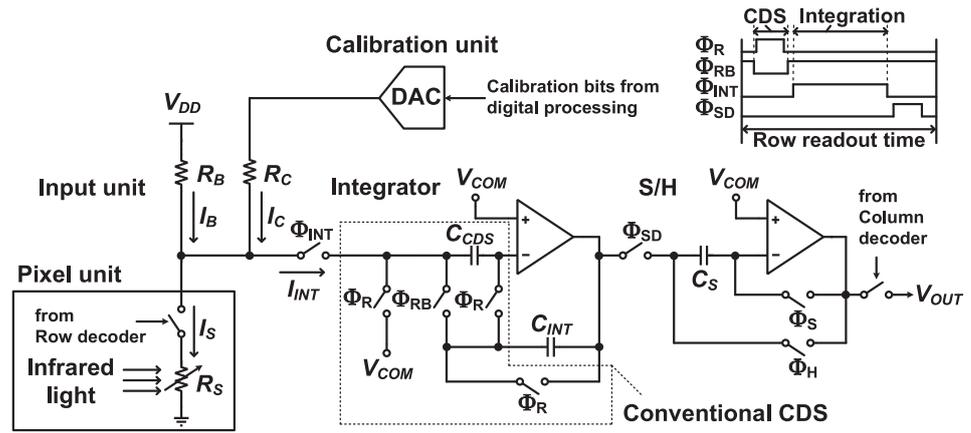Fig. 1. Generic readout architecture for an infrared imager.

Fig. 2. Column readout circuit with conventional CDS.

and mismatching effect of R_S in FPA through I_C. The current entering the integrator, I_{INT}, can now be expressed in terms of the currents I_B, I_S, and I_C, as follows:

$$I_{INT} = I_B - I_S + I_C = \frac{V_{DD} - V_{COM}}{R_B} - \frac{V_{COM}}{R_S} + \frac{V_{DAC} - V_{COM}}{R_C} \qquad (1)$$

where V_{DD} is a supply voltage, V_{COM} is a common-mode voltage, and V_{DAC} is a voltage output by the DAC.

I_{INT} is then amplified by the integration gain, G_{INT}:

$$V_{OUT} = I_{INT}G_{INT} = -I_{INT}\frac{T_{INT}}{C_{INT}} \qquad (2)$$

where T_{INT} is an integration time and C_{INT} is an integration capacitor.

The pattern noise contributions can be related to the variables in these equations. Noise in V_{DD} and V_{COM} contaminates all I_{INT} at a row readout time. This noise appears in the image as RN if its frequency is lower than the row readout frequency or as PN if its frequency is higher than the readout frequency. In terms of intrinsic noise of device, the $1/f$ noise is the dominant source of pattern noise when considering its low noise frequency range. Therefore, the individual contributions of RN without CDS are expressed as follows:

$$\overline{I_{INT.RN}^2} = \frac{\overline{V_{DD.1/f}^2}}{R_B^2} + \left(\frac{1}{R_B} + \frac{1}{R_S} + \frac{1}{R_C}\right)^2 \overline{V_{COM.1/f}^2} \qquad (3)$$

The noise in the integrator amplifier, V_{AMP}, and V_{DAC} are sources of CN because they operate as a column unit. The individual contributions of CN without CDS are expressed as follows:

$$\overline{I_{INT.CN}^2} = \frac{\overline{V_{DAC.1/f}^2}}{R_C^2} + \left(\frac{1}{R_B} + \frac{1}{R_S} + \frac{1}{R_C}\right)^2 \overline{V_{AMP.1/f}^2} \tag{4}$$

Thermal noise and kTC noise are the dominant source of PN. The individual contributions of PN are expressed as follows:

$$\overline{I_{INT.PN}^2} = \left(\begin{array}{c} \dfrac{4kT}{R_B} + \dfrac{\overline{V_{DD.t}^2} + \overline{V_{AMP.t}^2} + \overline{V_{COM.t}^2}}{R_B} + \dfrac{4kT}{R_S} + \dfrac{\overline{V_{AMP.t}^2} + \overline{V_{COM.t}^2}}{R_S} \\[3mm] + \dfrac{4kT}{R_C} + \dfrac{\overline{V_{AMP.t}^2} + \overline{V_{COM.t}^2} + \overline{V_{DAC.t}^2}}{R_B} + \dfrac{kT}{C_{INT}}\dfrac{1}{R_{RST}^2} \end{array} \right) \tag{5}$$

where the subscript, t, means thermal noise and R_{RST} is the resistance of reset transistor in integrator.

The noise produced by the sample-and-hold (S/H) and the analog-to-digital converter (ADC) can be ignored in practice because the gain of the integrator is not considered. The CFPN and RFPN are regarded as frequency independent noise. CFPN is mainly caused by device mismatching and RFPN can be caused by extrinsic noise sources such as a crosstalk between a row-wise internal node and a system clock. Therefore, the total noise (TN) considered frequency dependent noise is expressed as follows:

$$\overline{V_{TN}^2} = (\overline{I_{INT.RN}^2} + \overline{I_{INT.CN}^2} + \overline{I_{INT.PN}^2})G_{INT}^2 = \overline{V_{RN}^2} + \overline{V_{CN}^2} + \overline{V_{PN}^2} \tag{6}$$

Conventional CDS reduces the noise in V_{AMP} by using C_{CDS} that stores the noise before the integration starts, but this cannot reduce the noise in V_{DD}, V_{COM}, and V_{DAC} in equations of (3) and (4). In addition, this increases the RN and PN compared with those without CDS because the noise in V_{COM} becomes uncorrelated by C_{CDS}, decoupling negative input node of the integrator amp from I_{INT}. The proposed dual integration CDS can be an effective way of reducing the pattern noise from all these sources at the cost of introducing a third blind microbolometer and some additional switches.

3 Dual integration CDS

A column readout circuit for an infrared imager that uses the dual integration CDS is shown in Fig. 3. The concept of dual integration CDS individually readouts the level of extra blind microbolometer R_{CDS}, which we calls it reference integration, and active microbolometer R_S, which we call it signal integration, along with the operation of thermal calibration that needs a bit pattern and a DAC, and then their difference uses. Since the dual operation in front of integrator, the amplified pattern noise by G_{INT} can be correlated. In the input unit, two switches between the R_S and the extra R_{CDS} reduce the RN and CN caused by the noise in V_{DD}, V_{COM}, and V_{AMP}. In the calibration unit, the input to the DAC is switched between a bit pattern from digital processing unit and an extra hardwired bit pattern corresponding to V_{COM} in order to reduce the CN caused by the noise in V_{DAC}. As a result, the pattern noise is cancelled when considering entirely low noise frequency region, and the PN

increases because this correlation is lost at higher noise frequencies. The TN with dual integration CDS is expressed as follows:

$$\overline{V_{TN}^2} \approx (\overline{V_{REF.PN}^2} + \overline{V_{SIG.PN}^2}) \approx 2\overline{V_{PN}^2} \tag{7}$$

Operation of the dual integration CDS needs additional reference integration, and this might be expected to double the readout time. However, a time-flexible integration technique using C_{INT} separates two capacitors, C_1 and C_2 in the integrator minimizes this penalty. The time required for reference integration is T_{INT}/N, where N is expressed as (8), but this does not affect G_{INT}.

$$N = 1 + \frac{C_1}{C_2} \tag{8}$$

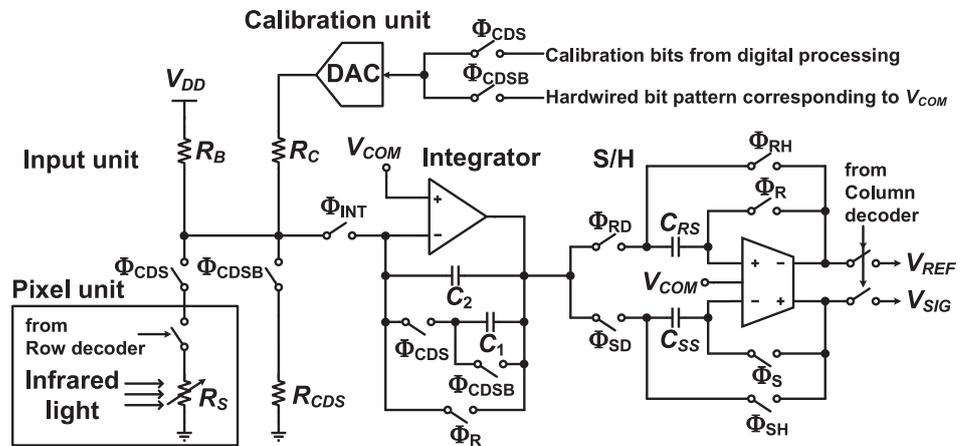The operating sequence explained by the timing diagram of Fig. 4 is as follows:

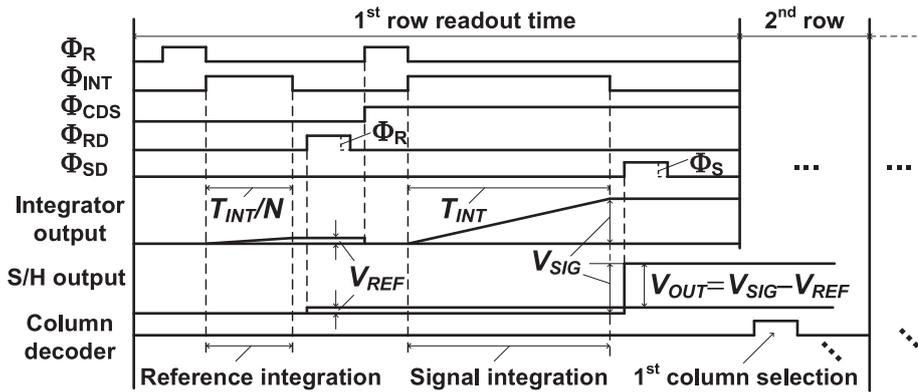**Fig. 3.** Column readout circuit with proposed dual integration CDS.

Fig. 4. Timing of dual integration CDS operation.

After the integrator has been reset, it begins to capture the pattern noise. After reference integration, the voltage V_{REF}, including amplified noise, is sampled by C_{RS} when Φ_{RD} is high. Φ_R is for bottom-plate sampling to remove the effect of charge injection. After Φ_{CDS} is high, I_{INT} is transferred into the integrator for the signal integration. And then, the V_{SIG} including the amplified noise and signal is sampled by C_{SS}. The hold signals generated by V_{REF} and V_{SIG} in the S/H circuit are

sent to the ADC by column decoder. This procedure is repeated for every row. The pattern noise is reduced by subtracting of V_{REF} and V_{SIG} which include amplified components of the RN, CN, RFPN, and CFPN.

4 Simulation results

In order to determine the effect of our dual integration CDS on noise, we used a transient noise simulation with a $0.18\,\mu m$ CMOS technology. It facilitates observing the noise behavior with non-ideal effects at transient response and selecting the noise bandwidth (NBW) that determines the noise type compared to AC noise simulation. Table I exhibits the circuit configurations and elements' values, which was implemented for this simulation.

Table I. Circuit configurations and elements' values

Process	$0.18\,\mu m$ technology
Supply voltage, V_{DD}	3.3 V
Common-mode voltage, V_{COM}	1.65 V
Default values of R_S, R_B, R_C, R_{CDS}	150 kΩ
R_S by infrared radiation except an environment temperature	145 kΩ
Sampling capacitors for S/H, C_{SS} and C_{RS}	2 pF
CDS capacitor, C_{CDS} for conventional CDS	2 pF
Integration capacitors, C_{INT} for conventional CDS, C_1 and C_2 for dual integration CDS	$C_{INT} = 3\,pF$ $C_1 = 3\,pF$, $C_2 = 0\,pF$ @ $N = 1$ $C_1 = 1.5\,pF$, $C_2 = 1.5\,pF$ @ $N = 2$ $C_1 = 2.25\,pF$, $C_2 = 0.75\,pF$ @ $N = 4$ $C_1 = 2.625\,pF$, $C_2 = 0.375\,pF$ @ $N = 8$
Integration time, T_{INT}	8 us
Integrator reset and S/H time	2 us
Circuits for voltage	Line-drop output for 3.3 V and voltage reference generator for 1.65 V with 10 uF load capacitor respectively
Internal amp type for integrator, S/H, and the output stage of DAC	2-stage amp

Table II exhibits simulation conditions in order to assess the each noise performance about RN, CN, PN, TN, and CFPN. Some ideal components provided by HSPICE were used to separate noise types along with the NBW. We note that the RFPN that is dominant at an extrinsic noise was excluded because the noise sources of this sort would be dependent on layout and test environment, and are beyond the scope of this paper. In RN, a noise frequency of 25 kHz approximately corresponds to the readout time for one row that can be visible to RN in the image.

Table II. Simulation conditions to separate noise types

RN	NBW of 50 Hz~25 kHz with ideal amp and switch to exclude the CN and PN
CN	NBW of 50 Hz~5 kHz with ideal V_{DD} and V_{COM} to exclude the RN and PN
PN	NBW of 25 kHz~100 MHz without ideal components to exclude the RN and CN
TN	NBW of 50 Hz~100 MHz without ideal components
CFPN	Monte-Carlo simulation with 100 samples

In CN, a noise frequency of 5 kHz approximately corresponds to the readout time for 5 rows that can be visible to CN in the image. In PN, the NBW includes the noise frequency above that of RN with all circuit components. The TN includes the CN, RN, and PN. The noise frequency of 50 Hz in the RN, CN, and TN was constrained by an acceptable simulation time. Monte-Carlo simulation was used to evaluate the effect of device mismatching.

Fig. 5 shows transient waveform at the output of integrator under the simulation condition of CN. The intrinsic noise gradually changes the output voltage of integrator with the course of time, which causes the column-wised pattern noise in an image. From the histograms that express the signal variation, our dual integration CDS reduces CN to 0.56 mV from 4.80 mV and 5.20 mV at standard deviation through the subtraction of V_{REF} and V_{SIG}.

Fig. 6 compares results from the column readout circuit with and without CDS corresponding to the prior works of [7, 8] and [9, 10] respectively with these from the dual integration CDS which significantly reduces the levels of all types of pattern noise. When compared with those without CDS, the conventional CDS reduces 67% and 52% of the CN and CFPN respectively, but increases 31%, 205%, and 80% of RN, PN, and TN respectively. Meanwhile, the dual integration CDS at $N = 1$ reduces 89%, 62%, 52% of CN, RN, and CFPN respectively with minimizing the increment of PN that is 36%. When compared with conventional CDS, the
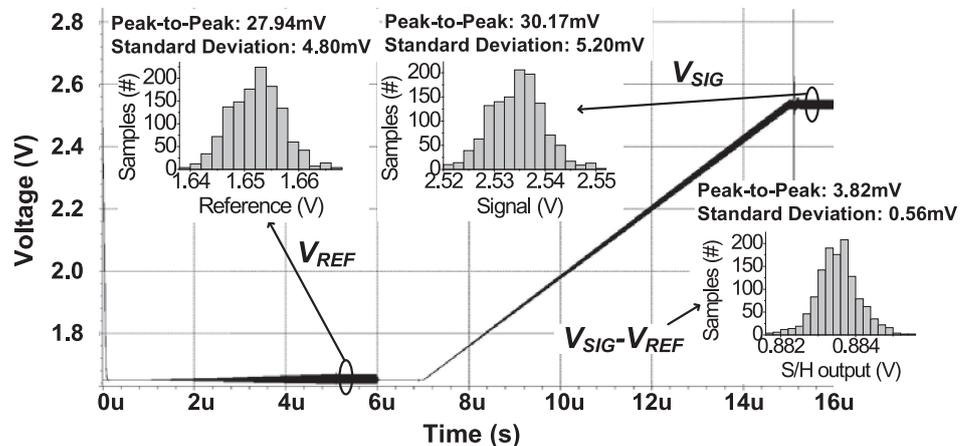

Fig. 5. Simulated waveform of dual integration CDS at $N = 2$. This waveform is accumulated from 0 ms to 20 ms.

dual integration CDS reduces 68%, 71%, 55%, 55%, and 95% of CN, RN, PN, TN, and CFPN respectively. The time-flexible integration technique reduces the readout time by increasing N, but this at least requires additional time for integrator reset and S/H at the reference integration. In terms of noise performance, the CFPN and CN increase due to the deterioration in the matching characteristic caused by reducing C_2 and the change of the noise in the integrator due to the asymmetry of reference and signal integration. Nevertheless, this technique still reforms better than conventional structure.
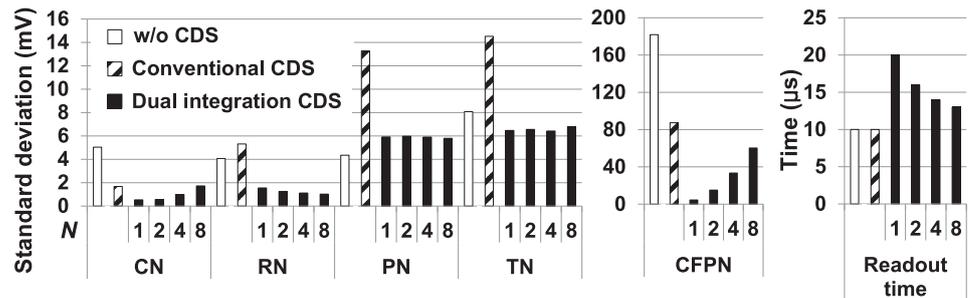

Fig. 6. Performance summary.

5 Conclusion

The effectiveness of CDS in an infrared imager is enhanced by dual integration method. The extra readout time that this requires is offset by time-flexible integration technique. We would expect the dual integration CDS to be effective in reducing not only intrinsic noise that we simulated, but also extrinsic noise from sources such as power-rail voltage fluctuation and crosstalk that depend on the overall design of the system.

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