Energy-Efficient Read-Out IC for High-Precision DC Measurement System with Instrumentation Amplifier Power Reduction Technique

Sangmin Shin, Minsung Kim, Junyoung Park, Hyunjoong Lee and Suhwan Kim
Department of Electrical and Computer Engineering
Seoul National University
Seoul 08826, Republic of Korea
E-mail: sangmin.shin@analog.snu.ac.kr, suhwan@snu.ac.kr

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***Abstract*—A high-precision DC measurement read-out integrated circuit (ROIC) is implemented from a low-noise capacitively-coupled chopper instrumentation amplifier (CCIA) followed by a high-resolution incremental discrete-time delta-sigma modulator (DTΔΣM) analog-to-digital converter (ADC). In this paper, a doubled sampling-time (DST) incremental DTΔΣM is proposed to reduce CCIA's bandwidth. Through the proposed technique, the power consumption of the traditionally power-hungry IA is halved, while the desired system specifications such as output data rate (ODR) and effective resolution (ER) are maintained. Implemented in a standard 0.13-µm CMOS process, the ROIC's effective resolution is 21.0 bit at gain 1 and that of 19.8 bit at gain 64. The analog part draws only 114.4 µA from 3-V supply.**

Keywords—Capacitively-coupled chopper instrumentation amplifier (CCIA), incremental discrete-time delta-sigma modulator (DTΔΣM), doubled sampling-time incremental DTΔΣM, analog-to-digital converter (ADC), differential difference amplifier (DDA), noise aliasing

I. Introduction

Wheatstone bridge is widely used in DC measurement systems such as pressure, temperature, humidity and etc [1]–[3]. As the sensor advances, the demand of high resolution read-out integrated circuit (ROIC) is increased, and energy-efficiency of ROIC becomes crucial for use in small applications such as mobile phones and wearable devices.

A high-precision DC measurement ROIC generally consists of a low-noise instrumentation amplifier (IA) and a high-resolution analog-to-digital converter (ADC) as shown in Fig. 1. The three-opamp IA, current feedback IA (CFIA) and capacitively-coupled chopper instrumentation amplifier (CCIA) are the three most commonly used IA topologies in high-precision DC measurement ROICs [2], [3]. The CCIA is being researched most actively in recent years due to its high power efficiency [3]–[7]. The noise of a CCIA is determined by one amplifier [3], [7], so that the energy efficiency is higher than the three-opamp IA and CFIA.

The reason why research is active despite high energy efficiency is because the CCIA still suffers from several drawbacks such as low input impedance, output ripples, and output spikes at its chopping transitions [3],[6]. The output spikes of CCIA at chopping transitions should not be sampled by ADC because it is nonlinear function of the input signal and the chopping frequency is forced to $2f_s$ [6], [7],

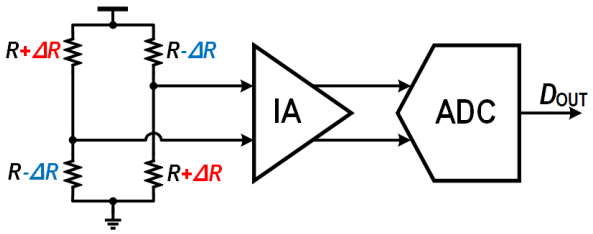


Fig. 1. Typical block diagram of a bridge-to-digital converter.

where f_s is ADC's sampling frequency. Then, the bandwidth is determined by ADC's sampling frequency. For complete settling, the CCIA's bandwidth needs to be wide enough or additional buffer is required, which increases noise aliasing and degrades ROIC's energy efficiency [6]–[8].

The [6] reduces CCIA's bandwidth by using continuous-time delta-sigma modulator (CTΔΣM) instead of using discrete-time delta-sigma modulator (DTΔΣM) which is mostly used in previous papers. The input is connected to common-mode voltage when CCIA's output generates spikes. However, CTΔΣM has an inherent disadvantage of being more sensitive to clock jitter and accuracy [9] than DTΔΣM. Also, in [8], pre-charging buffer and dynamic filter are introduced to increase energy efficiency by reducing noise aliasing, but this increases design complexity and introduces the need for an additional filter.

In this paper, we describe an energy-efficient high-precision DC measurement ROIC. We propose a CCIA's bandwidth reduction scheme by using a doubled sampling-time (DST) incremental DTΔΣM. For high gain DC measurement ROIC, to lower the input referred noise of the system, the IA consumes the majority of power in DC measurement ROIC, thus determining the energy-efficiency of the system. Using the proposed technique, the current consumption of the power-hungry CCIA is reduced to half compared to that of an IA followed by a conventional DTΔΣM. The sampling time of the proposed DTΔΣM is effectively doubled, while the output data rate is maintained. As the bandwidth of the CCIA is cut in half, it reduces noise aliasing generated from sampling of the ADC, which compensates for any degradation in system effective resolution and increase the energy-efficiency. In other words, the proposed technique relaxes the power-consumption burden of the IA and it can be applied to any other types of IAs in the DC measurement system.

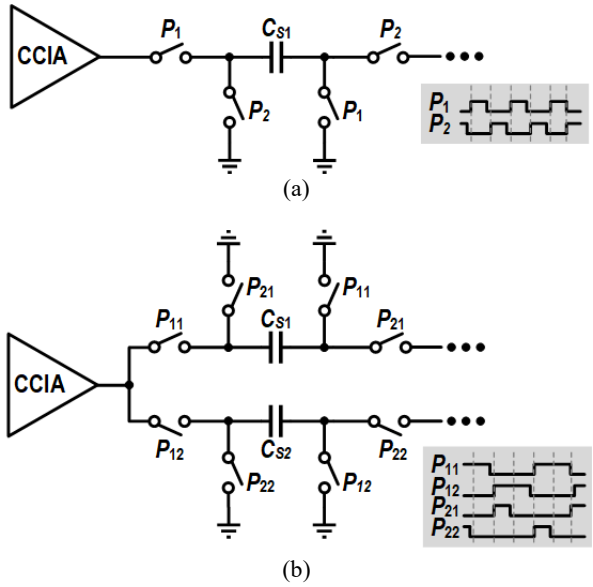


Fig. 2. Simplified block diagram of sampling and integrating operation of (a) a conventional DTΔΣM (b) a proposed doubled sampling-time DTΔΣM (single-ended circuit is assumed).

II. System Overview

A. Operation

A conventional DTΔΣM operates in two phases which are sampling and integration. The Fig. 2 (a) shows the simplified sampling and integrating operation of a conventional DTΔΣM and single-ended circuit is assumed. In the P_1 phase, C_{S1} samples the output of the IA; afterwards, in the P_2 phase, the first integrator integrates. Typically, bottom-plate sampling is employed, and P_1 and P_2 are switched using non-overlapping clocks to minimize circuit nonlinearities.

Fig. 2 (b) shows a simplified sampling and integrating operation of the DST incremental DTΔΣM. The switched-capacitor shows the sampling capacitors of a first integrator in proposed DTΔΣM. If the circuit is assumed as a single-ended circuit, in phase one, when P_{11} and P_{22} are high, C_{S1} does sampling and C_{S2} does integrating simultaneously. In phase two, when P_{11} is high and P_{22} is low, C_{S1} keeps sampling and C_{S2} is at rest. In phase three, when P_{12} and P_{21} are high, C_{S1} starts integrating and C_{S2} starts sampling. In phase four, P_{12} is high and P_{21} is low, the C_{S1} stops integrating and C_{S2} keeps sampling. The four-phase operation is continuously repeated until the conversion is ended when the incremental DTΔΣM's reset is high.

B. Analysis of the proposed system

If the DTΔΣM performs sampling and integrating with the sequences shown in Fig. 2 (b), the sampling time is effectively doubled comparing to that of a conventional DTΔΣM while maintaining the same output data rate. Assuming that CCIA is a single pole system without slew rate limitations, the doubled sampling time halves the bandwidth BW of the CCIA, as shown in equation (1) [6], [10]

$$BW \geq 2 \cdot (m+1) f_s \cdot \ln 2 \qquad (1)$$

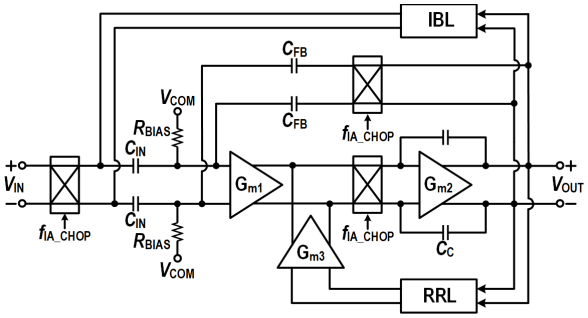


Fig. 3. Simplified block diagram of CCIA.

where f_s is the sampling frequency of the DTΔΣM and m is the target resolution. The noise within $\pi/2 \cdot BW$ folds back and it increases the CCIA's in-band noise power density [6]. Then, the ROIC's energy-efficiency decreases significantly [7]. By the DST incremental DTΔΣM, the bandwidth and the power of a CCIA are reduced to half, so that the lower noise-aliasing and higher energy-efficiency effects can be obtained.

In order to implement the proposed DST DTΔΣM design, additional area is required to add the extra sampling capacitor. However, in the perspective of a system, the area of a CCIA's main amplifier can be halved, effectively compensating for the additional area of the capacitor. Also, considering the kT/C noise and the half over sampling ratio (OSR) applied to each capacitor, the RMS noise of the proposed DST DTΔΣM is nearly doubled comparing with a conventional DTΔΣM. However, in the perspective of a system, the increased noise of the DTΔΣM is negligible because the input referred noise of a system is strongly determined by the gain of a CCIA as shown in equation (2)

$$V_{n,input-referred} = \sqrt{V_{n,IA}^{\ 2} + \frac{V_{n,ADC}^{\ 2}}{Gain^2}} \qquad (2)$$

where $V_{n,IA}$ is the input referred noise of IA and $V_{n,ADC}$ is the input referred noise of ADC. Finally, the mismatch of two sampling capacitors is not a concern in regards to the performance of the system. Because in the proposed system, the incremental DTΔΣM is used and the system is designed for DC signals. Therefore, the modulator's output will be averaged out accordingly.

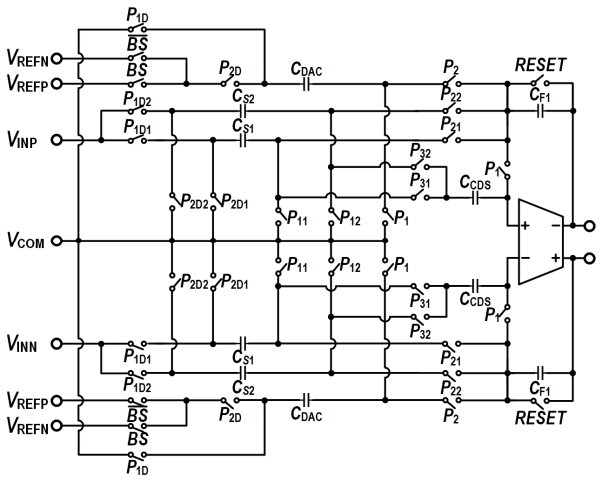
III. Circuit Implementation

A. CCIA Implementation

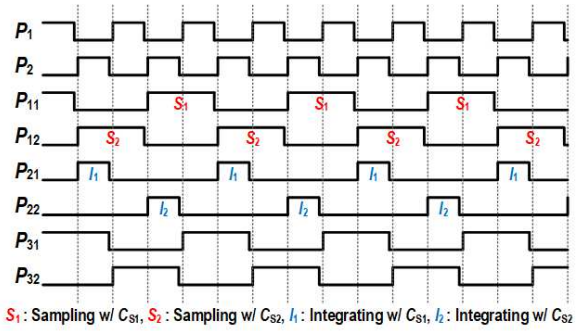
Fig. 3 shows the simplified schematic of the CCIA. The closed-loop gain G is determined by C_{IN}/C_{FB}. Given that C_{IN} = 16pF and C_{FB} = 1, 0.5, 0.33, and 0.25 pF to produce a closed-loop gain G of 16, 32, 48 and 64, respectively. When designing CCIA, the noise gain is the one that we need to consider. The equation (3) shows the noise factor calculated by signal gain, G, and noise gain, NG, [2]

$$\frac{G}{NG} = \frac{C_{IN} + C_P + C_{FB}}{C_{IN}} \qquad (3)$$

where C_P is the parasitic capacitance of the input stage. C_{IN} is chosen to have a relatively big capacitance to achieve a low noise factor.



(a)



(b)

Fig. 4. (a) Proposed 1st integrator of the DST DTΔΣM and (b) clock distribution.

To reduce the offset and flicker noise, a chopping modulator and demodulator are applied [4], [5]. The chopping frequency, f_{IA_CHOP}, is set to 30.72 kHz, which is set by $f_S/2$ and f_{IA_CHOP} is higher than $1/f$ corner frequency to reduce flicker noise appropriately.

Although, the CCIA has many advantages compared to other IAs such as rail-to-rail sensing capability, high energy-efficiency, and high gain accuracy [3], some drawbacks exist. The first drawback is limited input impedance and the second drawback is chopping ripple caused by the up-modulated offset and $1/f$ noise of G_{m1}. To solve these drawbacks, the impedance boosting loop (IBL) [3], [7] and the ripple reduction loop (RRL) [7], [11] are used as shown in Fig. 3. To apply RRL, a two-stage differential difference amplifier (DDA) is designed as a main amplifier in CCIA [7].

B. ΔΣ Modulator Implementation

An incremental DTΔΣM ADC is designed in this paper to digitize the output of the CCIA. Before applying the proposed idea, the conventional structure of the DTΔΣM was a second-order cascade of integrators with a feedforward (CIFF) as shown in Fig. 5. A separate sampling capacitor structure is used to suppress input-dependent current from the reference voltages and this structure is required to implement the proposed idea. 6 pF is used as a sampling capacitor C_S and 61.44 kHz is used for sampling frequency f_S and the output data rate is 5 Hz.

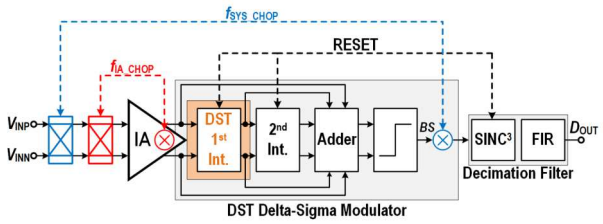


Fig. 5. Block diagram of the system

The Fig. 4 (a) shows the proposed first integrator in incremental DTΔΣM. The dual capacitors, C_{S1} and C_{S2}, are used as sampling capacitors to double the sampling time. P_1 and P_2 are 61.44kHz sampling and integrating clocks in the conventional DTΔΣM, respectively. Fig. 4 (b) shows the clock timing of the proposed first integrator. In the proposed scheme, the clocks P_{11} and P_{12} act as sampling clocks for C_{S1} and C_{S2}, respectively, which are 30.72 kHz. The clocks P_{21} and P_{22} are integrating clocks for C_{S1} and C_{S2}, respectively. The f_{IA_CHOP} transition occurs right after either P_{11} or P_{12} finishes sampling.

One thing to note here is that the reset and integrating time of the C_{DAC} in proposed DST DTΔΣM is same as those of the C_{DAC} in conventional DTΔΣM, which are P_1 and P_2. In the DTΔΣM, either V_{REFP} or V_{REFN} as an input to C_{DAC} is determined by the comparator's output bit-stream, *BS*, with feedback and it is not a concern with DC input in the proposed scheme. Accordingly, the C_{DAC}'s operation is exactly same as the conventional DTΔΣM.

In many cases, to reduce the $1/f$ noise of the amplifier and the offset, the correlated double sampling (CDS) technique is applied to the first integrator in DTΔΣM [12]. In the conventional first integrator, the offset-storage capacitor C_{CDS} stores the offset in the sampling phase and then stored offset is cancelled out in the integrating phase. However, in the proposed first integrator, there is a phase when the sampling and integrating occurs simultaneously. Because the absence of the CDS technique significantly degrades the DTΔΣM's performance, a modified CDS technique for the first integrator of the proposed DST DTΔΣM is implemented, and the effects of the modified CDS are confirmed through simulations. When P_1 is high, the bottom plate of the C_{CDS} is connected to the feedback capacitor, C_{F1}, and input of the amplifier, and the top plate is connected to either C_{S1} or C_{S2} to store the offset. When P_1 is low, bottom plate of the C_{CDS} is disconnected from C_{F1} and used for integration. The clocks P_{31} and P_{32} connect the top plate of C_{CDS} to C_{S1} and C_{S2}, alternatively. They are 1/4 delayed clocks of P_{11} and P_{12}.

C. System

Fig. 5 shows the block diagram of the entire system. It consists of a second-order system chopper, a CCIA, a DTΔΣM, and a decimation filter. The decimation filter consists of a $sinc^3$ filter followed by a finite impulse response (FIR) filter. Also, to reduce remaining $1/f$ noise and offset, a second-order system-level chopping is applied. The four consecutive outputs of $sinc^3$ are combined through a moving-average FIR filter [7]. The output data rate (ODR) is 5 samples per second (SPS).

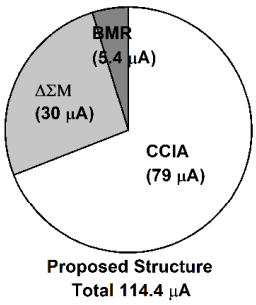


Fig. 6. Power distribution of the proposed ROIC.

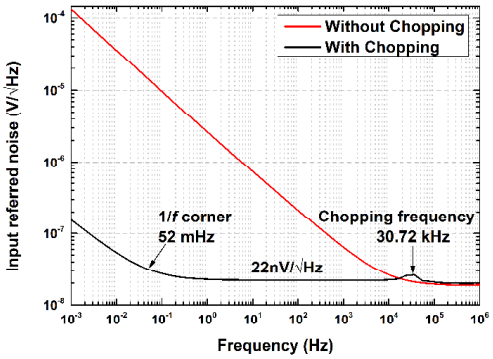


Fig. 7. Simulated CCIA's input-referred noise PSD.

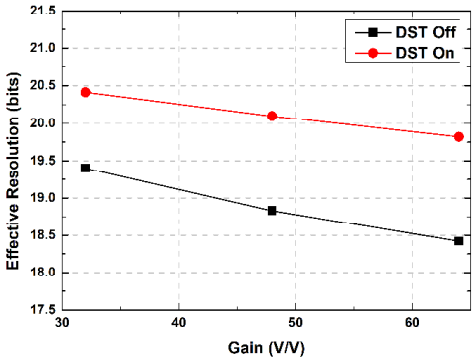


Fig. 8. Simulated effective resolution versus gain

IV. Simulation Results

In the high gain DC measurement system, the input-referred noise is dominated by an IA's main amplifier. Accordingly, the IA takes up most of the power in the system. Fig. 6 shows the power distribution of the proposed structure. The system draws only 114.4 μA from 3-V supply. If the system's IA is followed by a conventional DTΔΣM [7], [11] instead of the DST DTΔΣM, the current consumption of the IA will be increased by a factor of two, raising the total current consumption to approximately 193.4 μA.

Fig. 7 shows the input-referred noise density of the op-amp and chopped CCIA. The offset and 1/*f* noise of G_{m1} is mitigated by chopping, and G_{m2} noise is mitigated by open-loop gain of G_{m1} from Fig. 3. As shown in Fig. 7, 1/*f* noise is sufficiently suppressed by chopping with 30.72 kHz chopping frequency and 1/*f* corner is 52 mHz. The 1/*f* corner is further decreased through second-order system level chopping. Also, the simulation shows that the CCIA achieves an input-referred noise density of 22 nV/√Hz.

Fig. 8 shows the effective resolution (ER) of the proposed system. To prove the effects of the proposed DST DTΔΣM, we have designed a conventional DTΔΣM (DST off) and have applied the DST technique to the conventional DTΔΣM (DST on). The ERs of the DST off mode are 19.4, 18.8, and 18.4 bits at the gains of 32, 48, and 64, respectively. The ERs of the DST off mode are 20.4, 20.1, and 19.8 bits at the gains of 32, 48, and 64, respectively. In the DST off mode, the unit gain bandwidth of the CCIA is 7 MHz while that of the DST on mode is 3.5 MHz. As we have explained in section II, at the gain of 1, the ER of the DST off mode is nearly 1 bit higher than that of the DST on mode. However, in the perspective of the system, with half current consumption of the CCIA, the ERs are even higher at the high gains in the DST on mode due to the lower noise-aliasing. The table I shows that the proposed system shows outstanding performance in the system figure of merit (FOM).

TABLE I. Performance Summary and Comparison

	This work	**[7] JSSC' 19**	**[13] ISSCC' 18**	**[6] JSSC' 19**
Architecture	CCIA+ DTΔΣM	CCIA+ DTΔΣM	CCIA+ DTΔΣM	CCIA+ CTΔΣM
Technology (μm)	0.13	0.13	0.13	0.18
Supply voltage (V)	3.0	3.0	3.0	1.8
Supply current (μA)	114.4	142	326	1200
Conversion time (ms)	200	200	200	0.5
Gain range	1 ~ 64	1 ~ 128	1 ~ 128	100
+/- Input range (V)	2.8	2.8	2.8	0.01
ER (bits)	19.8 (gain 64)	19.6 (gain 64)	19.0 (gain 64)	15.4 (gain 100)
NEF of IA	7.4	6.6	10.5	4.5
FOM (dB) of read-out IC*	160 (gain 64)	157 (gain 64)	150 (gain 64)	155.5 (gain 100)

*FOM (dB)=SNR+10log(1/(2×Power×Conversion time))

V. Conclusion

An energy-efficient ROIC for a high-precision DC measurement system has been proposed. Energy-efficiency of the ROIC is one of the most important factors in high-precision DC measurement systems. Although, the CCIA is the most energy-efficient structure out of all IA topologies, its bandwidth is still determined by DTΔΣM's sampling frequency, and is prone to larger noise aliasing. Then, it lead to degraded energy-efficiency of the CCIA. To maximize energy-efficiency, DST DTΔΣM technique is proposed to cut the CCIA's bandwidth in half. As a result of the lower bandwidth, the noise-aliasing is reduced and higher energy-efficiency is achieved. The proposed technique is more effective at high gain system.

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