A 10.4-Gb/s 1-Tap Decision Feedback Equalizer With Different Pull-Up and Pull-Down Tap Weights for Asymmetric Memory Interfaces

Joo-Hyung Chae, *Member, IEEE*, Minchang Kim, Sungphil Choi, *Student Member, IEEE*, and Suhwan Kim, *Senior Member, IEEE*

***Abstract*—In asymmetric memory systems, the pull-up and pull-down data from the channel can have different amounts of inter-symbol interference (ISI), so they cannot be fully corrected by an equalizer which uses a single tap weight. We introduce a receiver-side single-ended 1-tap asymmetric decision-feedback equalizer (DFE) with a weight selection multiplexer, which allows the application of a different weight to each direction of data value transition. Implemented in a 55-nm CMOS technology, our DFE compensated for asymmetric ISI in a 10.4-Gb/s signal from a channel with an insertion loss of −8.3 dB, leading to a 50% wider horizontal margin at a bit-error-rate of 10^{-12} than symmetric correction. The energy efficiency is 0.16 pJ/bit.**

***Index Terms*—Quarter-rate receiver, decision feedback equalizer (DFE), memory interface, asymmetric equalization.**

I. Introduction

With the emerging interest in virtual reality, artificial intelligence, Internet of Things, and autonomous vehicles, there is increasing demand for higher data-bandwidth in memories such as double data-rate (DDR), low-power DDR (LPDDR), and graphics DDR (GDDR) [1]; thus, a higher data-rate per pin should be supported in memory interfaces [2]. This increases inter-symbol interference (ISI), because the insertion loss of the channel is frequency-dependent.

One way to compensate for an increased channel loss is to use an equalization technique. If the pull-up and pull-down ISI is identical, equalization can use the same tap weight for the pull-up and pull-down data [3]. However, memory interfaces use the single-ended signaling with the asymmetric termination [4], and the characteristics of the pull-up and pull-down output drivers are also asymmetric [5]–[8]. Thus rising and falling edge responses are likely to differ [9], so that pull-up and pull-down data have different amounts of ISI.

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J.-H. Chae and M. Kim were with the Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea. They are now with DRAM Design, SK hynix, Icheon-si 17336, South Korea.

S. Choi and S. Kim are with the Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea, and also with the Inter-University Semiconductor Research Center, Seoul National University, Seoul 08826, South Korea (e-mail: suhwan@snu.ac.kr).

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To compensate for the asymmetric response of the output driver, asymmetric feed-forward equalization (FFE) [10], [11] has been used to provide different amounts of emphasis pulses to the pull-up and pull-down data. However, transmitter-side equalization techniques require a large number of unit drivers in the output driver to obtain the asymmetric tap weights correctly. This makes impedance matching difficult and increases the pre-driver complexity and power consumption; this situation becomes worse if the number of taps is increased [12]. Since more current is consumed by the output driver when equalization is performed, the signaling and switching power increased, leading to a lot of simultaneous switching noise (SSN) that is one of the limiting factors in the performance of single-ended signaling.

To alleviate the above issues, we present a receiver-side single-ended 1-tap DFE, which can reduce ISI without significantly increasing noise or power consumption, with independently controlled pull-up and pull-down tap weights for asymmetric memory interfaces. This accounts for the asymmetric 1st post-tap ISI of the pull-up and pull-down data, by assigning a different DFE tap weight to each direction of data transition, thus producing more accurate equalization.

The rest of this brief is organized as follows: in Section II we describe the design considerations for asymmetric memory interfaces; in Section III we introduce our 1-tap asymmetric DFE; in Section IV we show how this DFE has been implemented; in Section V we present experimental results; and in Section VI we draw conclusions.

II. Design Considerations for Asymmetric Memory Interfaces

A. LPDDR4/4X Memory Interface

Fig. 1(a) shows an LPDDR4 memory interface with a low-voltage swing terminated logic (LVSTL) driver and a V_{SSQ} termination. The LVSTL driver is configured as an N-over-N driver that uses NMOS in both its pull-up and pull-down drivers. The pull-down driver operates in the linear region, while the non-linear pull-up driver operates in the saturation region [5]. If channel length modulation is not considered, the currents flowing the pull-up and pull-down driver can be expressed as follows:

$$I_{PU,LPDDR4} \approx {}^1\!/_2 \cdot \beta \cdot (V_{DDQ} - V_{RX} - V_{TH})^2 \quad (1)$$

and

$$I_{PD,LPDDR4} \approx {}^1\!/_2 \cdot \beta \cdot [2 \cdot (V_{DDQ} - V_{TH}) \cdot V_{RX} + V_{RX}^2], \quad (2)$$

where β is $\mu_n \cdot C_{ox}$·(W/L), μ_n is electron mobility, C_{ox} is the gate oxide capacitance per unit area, and V_{TH} is a threshold

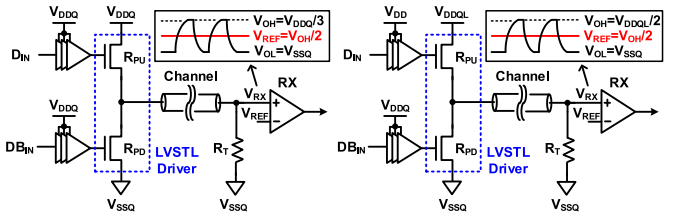


Fig. 1. (a) LPDDR4 and (b) LPDDR4X memory interfaces with an LVSTL driver and a V_{SSQ} termination.

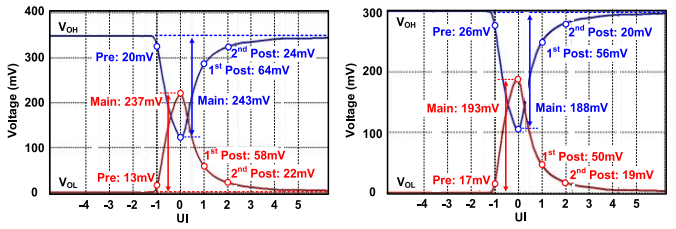


Fig. 2. Simulated single-bit responses of V_{RX} at 10Gb/s, for (a) the LPDDR4 and (b) the LPDDR4X memory interface of Fig. 1.

voltage. Since the current characteristics according to the voltage of the pull-up and the pull-down driver are different, the pull-up and pull-down drivers are not symmetric [5], [6].

Fig. 1(b) shows an LPDDR4X memory interface in which the output driver uses an isolated supply voltage V_{DDQL}, which is lower than the supply voltage V_{DD} of the pre-driver [7]. The introduction of V_{DDQL} allows both pull-up and pull-down drivers to operate in the linear region. The currents flowing the pull-up and pull-down drivers become [7]:

$$I_{PU,LPDDR4X} \approx {}^1\!/_2 \cdot \beta \cdot [2 \cdot (V_{DD} - V_{TH}) \cdot (V_{DDQL} - V_{RX}) + (V_{DDQL} - V_{RX})^2] \quad (3)$$

and

$$I_{PD,LPDDR4X} \approx {}^1\!/_2 \cdot \beta \cdot [2 \cdot (V_{DD} - V_{TH}) \cdot V_{RX} + V_{RX}^2]. \quad (4)$$

Asymmetric pull-up and pull-down signals can be generated by varying the amount of current flowing to each driver, which is controlled by V_{RX}.

We simulated the single-bit response of pull-up and pull-down data transmission to the LPDDR4 and LPDDR4X memory, with V_{DDQ} set to 1.1V in the LPDDR4 interface, and V_{DD} and V_{DDQL} set to 1.1V and 0.6V respectively in the LPDDR4X interface. The simulated channel loss was −9.5dB at 5.0GHz. Fig. 2(a) and (b) show their simulated results at 10Gb/s. The asymmetry of these interfaces is apparent, as the pre-tap, 1st post-tap, and 2nd post-tap ISIs of the pull-up and pull-down data signal are different.

B. GDDR6/DDR4 Memory Interface

Fig. 3 shows a GDDR6 and DDR4 memory interface, consisting of a pseudo open drain (POD) driver [13], in which both pull-up and pull-down drivers operate in the linear region, and a V_{DDQ} termination. The GDDR6 memory interface adopts the unmatched on-resistances of 60Ω and 40Ω in the pull-up and pull-down drivers, and the V_{DDQ} termination of 60Ω [8]. The corresponding values are matched in

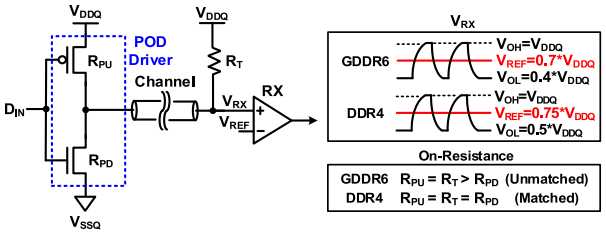


Fig. 3. GDDR6 and DDR4 memory interface.

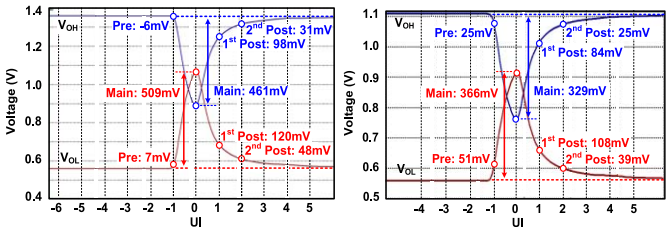


Fig. 4. (a) Simulated single-bit response of V_{RX} in the GDDR6 memory interface at 12Gb/s, and (b) in the DDR4 memory interface at 10Gb/s.

the DDR4 memory interface, but the strength of the pull-up driver differs from that of the pull-down driver, due to the different characteristics of PMOS and NMOS. Furthermore, asymmetric V_{DDQ} termination can increase the asymmetry of the transmitted signal in these interfaces [4].

We performed single-bit response simulations of these interfaces, with a V_{DDQ} of 1.35V and 1.1V in the GDDR6 and DDR4 memory interfaces. The channel loss is −9.5dB at a Nyquist frequency. Fig. 4(a) and (b) show simulated single-bit responses of the GDDR6 and DDR4 memory interfaces at a data-rate of 12Gb/s and 10Gb/s. The 1st post-tap ISIs of the pull-up and pull-down data signal are different, and the pre-tap and 2nd post-tap ISIs of the pull-up and pull-down signal are also asymmetric. These results demonstrate that the different characteristics of the pull-up and pull-down drivers cause the asymmetrical ISI, which requires asymmetric equalization.

C. Asymmetry According to Channel Loss

To verify the relationship between the channel loss and the asymmetry of the tap weight, we performed the above simulation again for several channel losses in each interface. Fig. 5 shows the simulated difference between the pull-up and pull-down tap weights, according to channel loss. The asymmetry increases with the channel loss.

III. 1-Tap DFE With Different Pull-Up and Pull-Down Tap Weights

Fig. 6 shows a block diagram of a 1-tap asymmetric DFE, which consists of a weight selection multiplexer (WMUX), a summer, and a sampler. This figure also shows that the pull-up and pull-down data results in different post-tap ISI in the waveforms passing through the channel. The asymmetric DFE can correct this imbalance by applying a weight W_{PU} to the pull-up data and a weight W_{PD} to the pull-down data.

Both symmetric and asymmetric DFE based on data-state improves the data eye by compensating for post-tap ISI when there is a data transition, but it reduces the height of the data eye when there is no transition [14]. We define the data eye as an AC data eye when there is a data transition

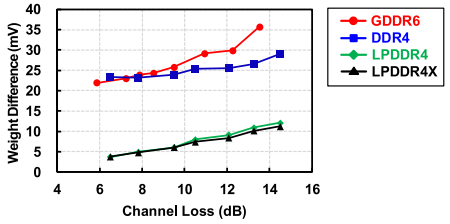


Fig. 5. Simulated difference between the pull-up and pull-down weights.

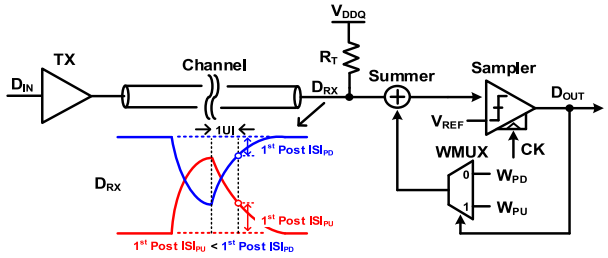


Fig. 6. Block diagram of the 1-tap DFE with the different pull-up and pull-down tap weights.

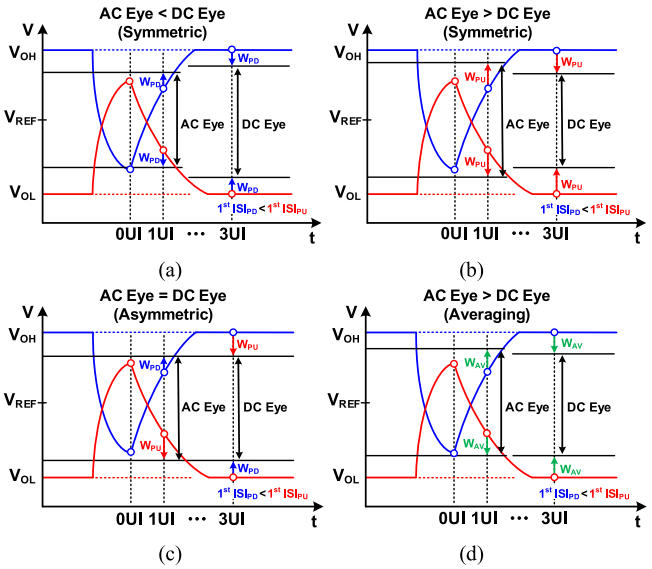


Fig. 7. (a) Less-equalization and (b) over-equalization, resulting from equal pull-up and pull-down tap weights, (c) improved equalization by an asymmetric DFE, and (d) equalization by an average of asymmetric weights.

and the DC data eye when there is no data transition. To demonstrate the concept of our DFE, Fig. 7 shows how symmetric and asymmetric DFEs remove ISI from a single-bit response [14], [15]. Fig. 7(a) and (b) show waveforms that the same tap weight is applied to both pull-up and pull-down data when 1st post-tap ISI of the pull-up data is larger than that of the pull-down data. Applying a weight W_{PD} appropriate for the 1st post-tap ISI of the pull-down data to the pull-up data as well, results in less-equalization. Conversely, if the DFE applies a weight W_{PU} based on the 1st post-tap ISI of the pull-up data to the pull-down data as well, there is over-equalization. Data eyes of equal heights are only obtained when different pull-up and pull-down weights W_{PU} and W_{PD} are applied by the DFE to each direction of the data transition, as shown in Fig. 7(c). When an average weight W_{AV} of pull-up and pull-down weights W_{PU} and W_{PD} in Fig. 7(c) is applied, the AC and DC data eyes are still different, as shown in Fig. 7(d).

IV. Implementation

A. Architecture

To assess the effectiveness of asymmetric equalization, we designed the receiver shown in Fig. 8, which has a 1-tap DFE with different pull-up and pull-down tap weights. This receiver has a quarter-rate architecture to ensure a relaxed timing margin on the direct feedback path of the DFE [2], [16].

Quadrature clock signals CK_0, CK_{90}, CK_{180}, and CK_{270} are generated from the incoming differential clock signals CK and CKB in the clock path. Three resistor ladders generate the reference voltage V_{REF} and the pull-up and pull-down tap weights W_{PU} and W_{PD}, as specified by the selection signals $SEL_{VREF}<5:0>$, $SEL_{WPU}<3:0>$, and $SEL_{WPD}<3:0>$.

The quarter-rate DFE consists of four units DFE_0, DFE_{90}, DFE_{180}, and DFE_{270}, each of which contains a WMUX, a summer, a sampler, and a latch. This DFE compensates for the 1st post-tap ISI of the asymmetric input data signal D_{RX} by assigning different pull-up and pull-down tap weights, and this compensated data signal are demuxed into four quarter-rate data signals $D_{OUT,0}$, $D_{OUT,90}$, $D_{OUT,180}$, and $D_{OUT,270}$ by the quadrature clock signals. In the test setup, we monitored $D_{OUT,0}$ to measure the bit-error-rate (BER).

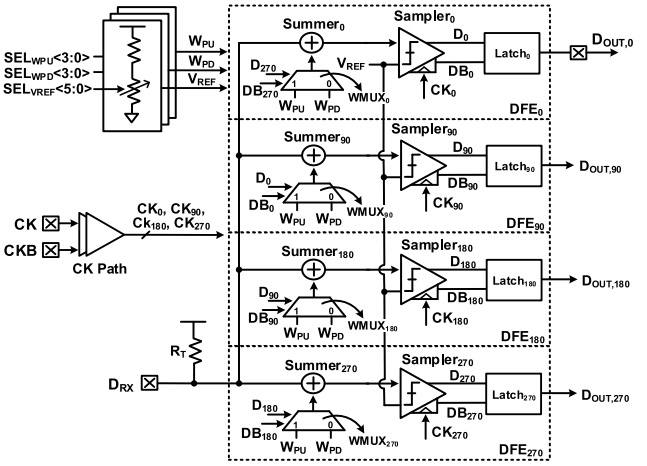


Fig. 8. Block diagram of a quarter-rate receiver with a DFE with the different pull-up and pull-down tap weights.

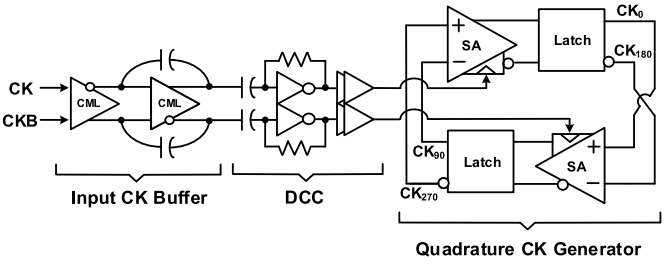


Fig. 9. Block diagram of the clock path.

B. Clock Path

The clock path contains an input clock buffer, a duty-cycle corrector (DCC), and a quadrature clock generator, as shown in Fig. 9. The differential clock signals CK and CKB are amplified in 2-stage input clock buffers based on a current-mode logic (CML) amplifier, with a negative capacitance circuit to

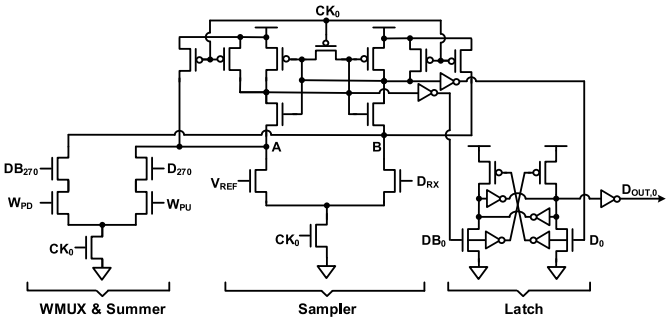
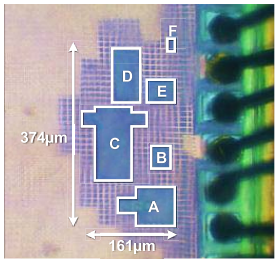


Fig. 10. Circuit diagram of one of the four DFE units (DFE_0).



	Block Description
A	Input Clock Buffer & Duty-Cycle Corrector
B	IQ Generator
C	Resistor Ladder for W_{PU} and W_{PD}
D	Resistor Ladder for V_{REF}
E	Four Samplers, Weight Selection MUXs, Summers, and Latches
F	Output Data Buffer

Fig. 11. Die micrograph and block description.

increase its bandwidth. The duty-cycle corrector increases the signal bandwidth, corrects duty-cycle errors, and changes the level of the clock signals to CMOS voltage. These signals pass to the quadrature clock generator, consisting of two sense amplifiers (SAs) and two latches, which converts them to the quadrature clock signals CK_0, CK_{90}, CK_{180}, and CK_{270}, which then enter the DFE.

C. Decision Feedback Equalizer

Fig. 10 is the circuit diagram of one of the DFE units (DFE_0), which consists of a WMUX, a summer, a sampler, and a latch. To reduce the offset mismatch, MOS devices of sufficiently large size are used. When the clock signal CK_0 goes low, all the circuits in the DFE_0 reset. The WMUX selects either W_{PU} or W_{PD}, depending on the value of the previous data bits D_{270} and DB_{270}, and this tap weight is subtracted from the voltage at the node A or B of the sampler through the summer when CK_0 goes high; thus, the selected tap weight is reflected in the current data bit. When CK_0 goes high, current data D_0 and DB_0 are determined, depending on the difference between the voltages of nodes A and B. The latch holds the value of the current data bit, and outputs $D_{OUT,0}$. In the post-layout simulation, the feedback loop delay, which limits the maximum data-rate, of our DFE is 78ps and 99.8ps in typical and slow process corners with a supply voltage of 1.3V.

V. Measurement Results

A prototype chip was implemented in a 55nm CMOS technology with a supply voltage of 1.3V. Fig. 11 shows a micrograph of the die, which has a total area of 0.06 mm^2, including the decoupling capacitor. The resistor ladders which generate W_{PU}, W_{PD}, and V_{REF} are the largest block, but they can be shared by several DQ paths.

Fig. 12(a) shows our measurement setup. The differential clock signals CK and CKB and the data signal D_{RX} are generated in the pattern generator of the signal quality analyzer (Anritsu MP1800A), and transmitted to the chip. The BER was

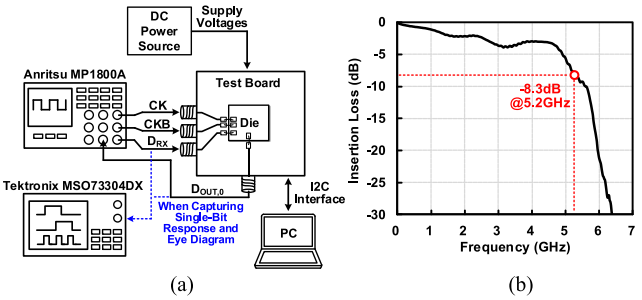


Fig. 12. (a) Measurement setup and (b) the measured channel loss of the D_{RX} path.

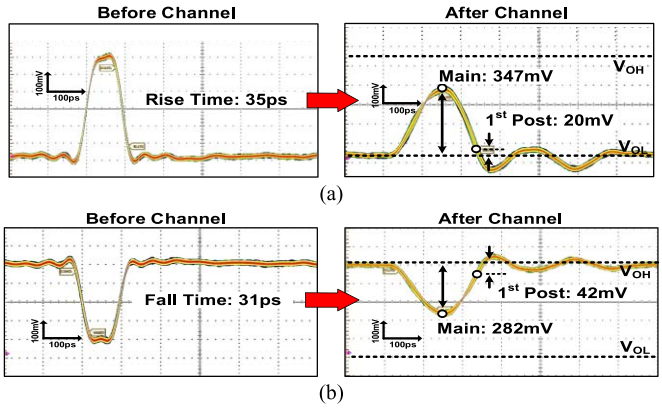


Fig. 13. Measured single-bit responses of (a) pull-up and (b) pull-down data before and after the channel, at 10.4Gb/s.

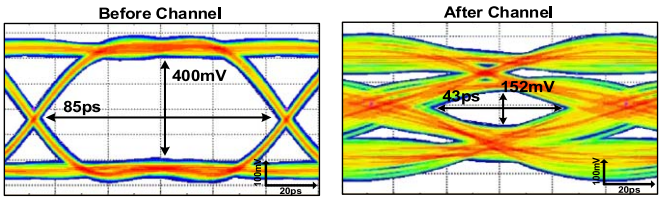


Fig. 14. Measured eye diagrams of the receiver data input D_{RX} before and after the channel, at 10.4Gb/s with the PRBS7 pattern.

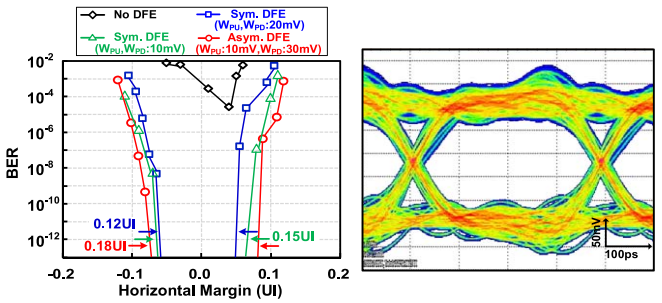
found using the error detector in the signal quality analyzer, and the eye diagrams of the input data signal D_{RX} and the output data signal $D_{OUT,0}$ were displayed on an oscilloscope (Tektronix MSO73304DX). The measured channel loss of the D_{RX} path, which consists of an SMA cable, an SMA connector, and an FR4 trace, is shown in Fig. 12(b): the insertion channel loss is −8.3dB at the Nyquist frequency of 5.2GHz.

The single-bit response was measured at 10.4Gb/s, before and after the signal goes through the channel of the D_{RX} path to verify that the pull-up and pull-down data exhibit different characteristics in the asymmetric interface. Fig. 13(a) shows the single-bit response of the pull-up data: it has a rise time of 35ps before passing through the channel, and a main-tap of 347mV and a 1st post-tap of 20mV after passing through the channel. Fig. 13(b) shows pull-down data, which has a fall time of 31ps before passing through the channel, and a main-tap of 282 mV and a 1st post-tap of 42 mV after passing through the channel. The difference between the 1st post-tap voltages of the pull-up and pull-down data justify an asymmetric equalization. There are some ISI after the 1st post-tap due to several discontinuity points in the measurement setup.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER DFE DESIGNS

	[3]	[16]	[17]	[18]	This Work
Technology	65nm	40nm	130nm	65nm	55nm
Supply	1.2V	1.0V	1.2V	0.8V	1.3V
Data-Rate	6.4Gb/s	20Gb/s	3.4Gb/s	12.5Gb/s	10.4Gb/s
Architecture	Half-rate	Quarter -rate	Quarter -rate	Quarter -rate	Quarter -rate
Signaling	Differential	Differential	Single -ended	Single -ended	Single -ended
Equalization	1-tap DFE	1-tap DFE +2 IIR filter	2-tap DFE	2-tap DFE	1-tap DFE (asymmetric)
Channel Loss	-11.96dB	-18.3dB	N/A	-14dB	-8.3dB
Timing Margin @BER	0.56UI @10^{-11}	0.20UI @10^{-12}	0.20UI @10^{-12}	[b] 0.35UI @10^{-12}	0.18UI @10^{-12}
[a] Power	1.13mW	6.2mW	3.03mW	2.75mW	1.71mW
[a] Energy Efficiency	0.17pJ/bit	0.31pJ/bit	0.89pJ/bit	0.22pJ/bit	0.16pJ/bit
[a] FoM (pJ/bit/dB)	0.014	0.017	N/A	0.016	0.019
[a] Area	N/A	0.005mm^2	0.002 mm^2	N/A	0.001mm^2

[a] DFE core only [b] Uses PRBS31 pattern



(a) (b)

Fig. 15. (a) Measured bathtub curves at 10.4Gb/s, with no DFE, with the symmetric DFE, and with the asymmetric DFE, and (b) measured eye diagram of the 1:4 demuxed output data $D_{OUT,0}$.

Fig. 14 shows the eye diagram of a PRBS7 pattern before and after passing through the channel to the receiver. Before passing through the channel, the eye has a width of 85ps and a height of 400mV. After passing through the channel, it has a width of 43ps and a height of 152mV. Due to pad capacitances of the test board and the chip, the bonding wire, and the input capacitance of the receiver, the eye opening of the receiver data input D_{RX} is more closed in the real operation.

The BER performance was measured by applying the same PRBS7 pattern through the channel of the D_{RX} path. Fig. 15(a) shows measured bathtub curves at a data-rate of 10.4Gb/s, without the DFE, with the symmetric DFE, and with the asymmetric DFE. Operation at 10.4Gb/s is feasible with the 1-tap symmetric DFE, which increases the width of the previously closed eye to a timing margin of 0.15UI and 0.12UI, at a BER of 10^{-12} with the same pull-up and pull-down weights of 10mV and 20mV. The width of the horizontal margin is further increased by the asymmetric 1-tap DFE, to a timing margin of 0.18UI at a BER of 10^{-12}. When symmetric and asymmetric weights are applied, their power consumptions are approximately equal, which is about 1.71mW. Therefore, the asymmetric DFE achieves better equalization effect than the symmetric DFE, without power and area overhead. Fig. 15(b) shows the eye diagram of the 1:4 demuxed data output $D_{OUT,0}$ when the asymmetric DFE is in operation.

The performance of our DFE is summarized and compared with previous designs [3], [16]–[18] in Table I.

VI. CONCLUSION

We have presented a receiver-side single-ended 1-tap DFE for asymmetric memory interfaces. It uses asymmetric pull-up and pull-down tap weights, determined from data transition direction to eliminate different amounts of ISI in the pull-up and pull-down data. Fabricated in a 55nm CMOS technology, our DFE compensated for asymmetric ISI at a data-rate of 10.4Gb/s in a channel with an insertion loss of −8.3dB. The energy efficiency of the DFE is 0.16pJ/bit.

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