A CMOS Analog Front-End for Driving a High-Speed SAR ADC in Low-Power Ultrasound Imaging Systems

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***Abstract*— In recent studies of ultrasound imaging systems, successive approximation register (SAR) analog-to-digital converters (ADCs) are suggested as an alternative architecture for low-power ultrasound receiver integrated circuits. However, the sampling period of a high-speed SAR ADC is very short - less than a few nanoseconds. This results in the need of a very wide unity-gain bandwidth of the amplifier in the anti-aliasing filter (AAF), and it also causes more serious kick-back noise. In this paper, a single-channel analog front-end (AFE) with a RC filter for a high-speed SAR ADC is presented. The RC filter relaxes the bandwidth requirement of the amplifier in the AAF by 16% and reduces kick-back noise coming from the ADC input. The proposed AFE is fabricated in 0.18μm CMOS process. The design achieves 5.05nV/√Hz input-referred noise density and the voltage gain is controlled in the range of [-3.02, 30.6] dB in a linear-in-dB scale with 16 steps by a 4-bit digital code. Our AFE circuit consumes 30mA from a 1.8V supply.**

Keywords—Ultrasound imaging systems; analog front-end (AFE); low-noise amplifier (LNA); variable-gain amplifier (VGA); anti-aliasing filter (AAF); analog-to-digital converter (ADC); kick-back noise

I. INTRODUCTION

Ultrasound imaging has been one of the most popular medical methods because it is harmless to human body, cost-effective, and real-time capability. In an ultrasound imaging system, the front-end receiver is the key in determining the overall system performance such as signal-to-noise ratio (SNR), dynamic range (DR), and frame rate. Ultrasound receiver circuit consists of a low-noise amplifier (LNA), variable-gain amplifier (VGA), anti-aliasing filter (AAF), and analog-to-digital converter (ADC) [1].

CMOS implementation of the front-end receiver circuit is essential for high-integration and low-cost in consumer electronics [2]. The previous work has presented the amplifier path that consists of a LNA and VGA in 0.18μm CMOS process [3]. However, it does not include an AAF which drives a following ADC as well as preventing aliasing.

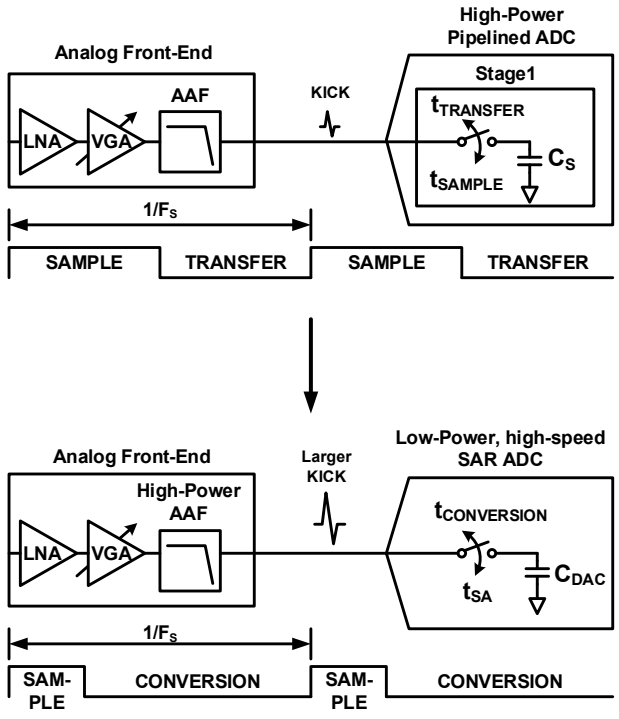

Fig. 1. Problems caused by employing the SAR ADC instead of the pipelined ADC in ultrasound receiver.

Considering the recent trend of studies, the design of an AAF as an ADC driver becomes increasingly important. Because many studies [4-8] pay attention to a successive approximation register (SAR) ADC as an alternative to a pipelined ADC that is employed as a conventional ultrasound receiver [9]. The SAR ADC itself has an advantage of low-power consumption and compatibility with technology scaling, however, another burden is added to the AAF while driving the ADC as shown in Fig. 1. Typically, the sampling period of SAR ADC is below 25% of the whole ADC throughput period [4], [6], and [7].

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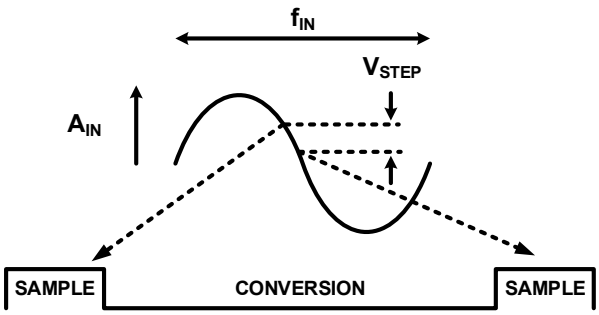

Fig. 2. Typical timing diagram of SAR ADC.

Comparing with the pipelined ADC, the sampling period is reduced more than two times, while the conversion period gets longer. This means that the change of the AFE's output voltage increases during the conversion period. Then, the kick-back noise between the AAF and the ADC becomes larger, while the time for settling back to the correct input value of the ADC is reduced. It requires that the bandwidth of the amplifier in the AAF has to be extended to prevent degradation of the overall performance. Consequently, the higher-power consuming AAF is demanded.

In this paper, to overcome the larger kick-back noise problem, we propose a single-channel analog front-end (AFE) with including a RC filter. The RC filter is added to attenuate the kick-back noise from the capacitor digital-to-analog converter (CDAC) in the SAR ADC and relaxes the bandwidth requirement of the amplifier in the AAF. Such modification of the AFE is essential to benefit the low-power and high-speed SAR ADCs in the ultrasound imaging system. The proposed chip consists of the LNA, VGA, AAF and RC filter and is fabricated in 0.18μm CMOS process.

The remainder of this paper is organized as follows: Section II addresses the design consideration of an on-chip first-order RC filter to reduce the kick-back noise. The architecture of the proposed analog front-end and the circuit implementation are presented in Section III. Section IV verifies the design with the measurement data. Finally, this paper is concluded in Section V.

II. On-Chip RC Filter For Kick-Back Noise Reduction

Fig. 2 shows the typical timing diagram of a high-speed SAR ADC. In the sampling period, the capacitors in the internal CDAC of the ADC is connected to the output of the AAF. The output signal of the AAF is captured on the capacitors of the SAR ADC. Then the sampling switch opens and disconnects the output signal of the AAF from the rest of the ADC. The conversion process occurs for this stored voltage, by redistributing charge from the capacitor to other capacitors.

When the ADC is ready to take another sample, the sampling switch closes again, reconnecting the output of the

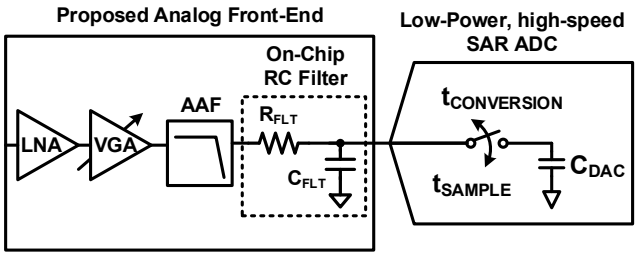

Fig. 3. Proposed analog front-end for a low-power and high-speed SAR ADC including on-chip RC filter.

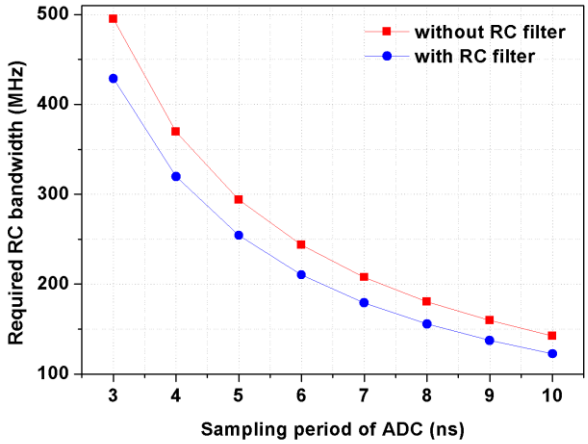

Fig. 4. Required RC bandwidth against sampling period of ADC.

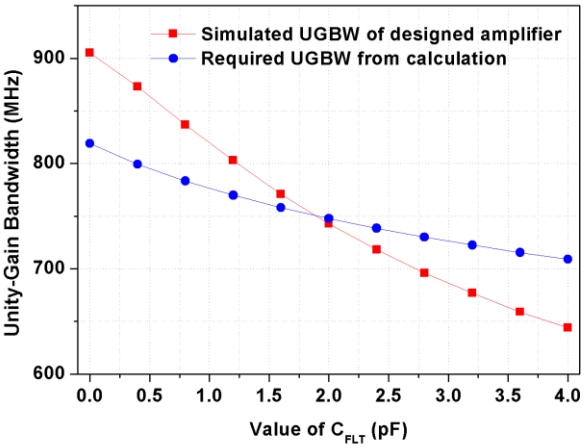

Fig. 5. Unity-gain bandwidth of the amplifier in the AAF against the value of C_{FLT}.

AAF to the capacitors in the CDAC. At this moment, the residual charge on these capacitors will have only one place to go back out the output of the AAF. Because of this phenomenon, during the sampling phase, undesirable spikes, which is also called as kick-back noise, can be observed between the AAF and the SAR ADC. Although these spikes

TABLE I. SAR ADC PARAMETERS USED IN THE SIMULATION

Parameters	Value	Unit
Resolution	12	bit
Maximum input frequency	20	MHz
Input amplitude	0.8	V
Throughput period	25	ns
Sampling period	3.35	ns
Sampling capacitor	1.6	pF
Power consumption	5.69	mW

themselves are not bad for the ADC, if they do not settle back to the correct input value within the sampling time, then this may cause the degradation of the performance.

However, employing the high-speed SAR ADC for the ultrasound imaging system forces the sampling time to be reduced to below 5ns. Therefore the spikes present very demanding load to the AAF. The RC filter, which is inserted between the AAF and the SAR ADC as shown in Fig. 3, can minimize the kick-back noise and nonlinearities from the spikes. The values of R_{FLT} and C_{FLT} are selected by taking into account of the properties of the following SAR ADC [10]. Major considerations are the input frequency, the input range, the throughput period, the percentage of sampling period and resolution. To choose a decent RC filter, we have to calculate the RC bandwidth in the following manner.

For a sine wave signal with given input frequency f_{IN} and amplitude A_{IN}, the maximum undistorted rate of change can be expressed as

$$2\pi f_{IN} A_{IN} . \quad (1)$$

The maximum amount of the AAF output, has changed during the conversion time $t_{CONVERSION}$, can be calculated as

$$2\pi f_{IN} A_{IN} t_{CONVERSION} . \quad (2)$$

This is the maximum voltage step that is seen by the CDAC when it is switched back to the sampling mode. This step is attenuated by the parallel combination of the C_{DAC} and C_{FLT}. The step size, V_{STEP} that needs to be settled is given by

$$V_{STEP} = 2\pi f_{IN} A_{IN} t_{CONVERSION} C_{DAC} / (C_{DAC} + C_{FLT}) . \quad (3)$$

Then, the time constant to settle the AAF output to 0.5LSB during the sampling time of the ADC can be calculated. The required RC time constant τ is

$$\tau = t_{SAMPLE} / N_{TC} \quad (4)$$

where t_{SAMPLE} is the sampling time and N_{TC} is the number of time constants required to settle. From the natural logarithm of

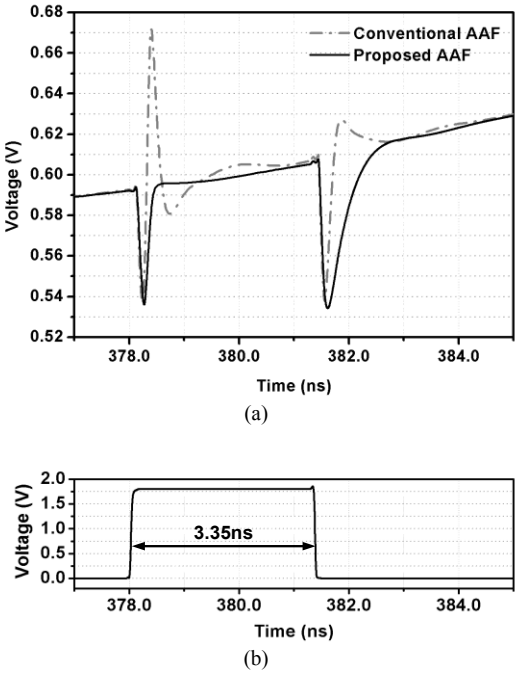

Fig. 6. (a) Signal behavior of the AFE output both with RC filter and without RC filter (b) Sampling signal of the ADC.

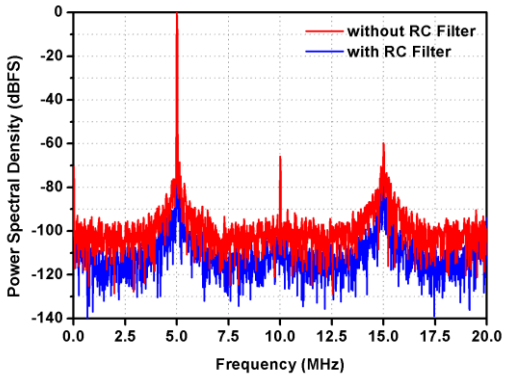

Fig. 7. FFT spectrum of the AFE output both with RC filter and without RC filter.

the ratio of the step size V_{STEP} to the settling error, the required number of time constants N_{TC} can be calculated as

$$N_{TC} = \ln(V_{STEP} / (V_{REF} / 2^{N+1})) . \quad (5)$$

Thus, R_{FLT} can be expressed as

$$R_{FLT} = \tau / (C_{FLT} + C_{DAC}) . \quad (6)$$

In this work, the high-speed SAR ADC, having the parameters in Table I, is used to obtain the values of R_{FLT} and

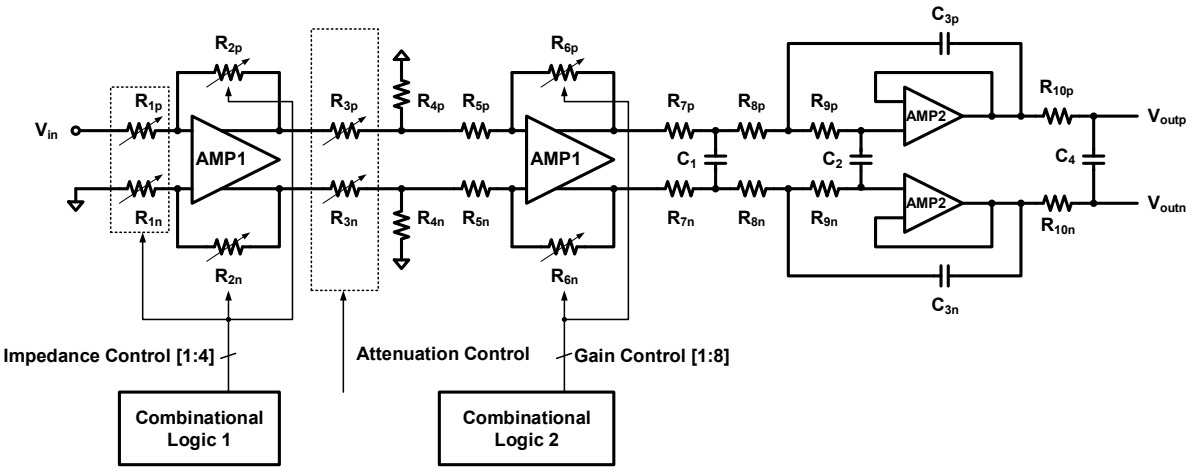

Fig. 8. Top-level block diagram of the proposed AFE.

C_{FLT} of the RC filter. Fig. 4 shows the required RC bandwidth against the sampling period of the ADC and compares between the cases of without and with the on-chip RC filter. As the sampling period of the ADC decreases, required RC bandwidth increases drastically. The unity-gain bandwidth of the amplifier, which is placed in the AAF, can be decided by this graph. It is generally known that the unity-gain bandwidth of the amplifier in the AAF should be at least two times larger than the RC bandwidth. By inserting the on-chip RC filter, the required RC bandwidth can be reduced to about 84%.

Fig. 5 shows the unity-gain bandwidth (UGBW) of the amplifier in the AAF against the value of the C_{FLT} when the sampling period of the ADC is 3.35ns. The designed amplifier has 905MHz of the unity-gain bandwidth when the RC filter is excluded. In the respect of reducing the kick-back noise, the value of the C_{FLT} must be maximized. However, 2pF is selected for C_{FLT} because the simulated unity-gain bandwidth of the designed amplifier becomes smaller than the required unity-gain bandwidth obtained by calculation.

To verify the kick-back noise reducing effect of the on-chip first-order RC filter, the transient simulation has been performed including the proposed AFE and SAR ADC. We have applied a sine wave with the amplitude of $0.25V_{PP}$ and the frequency of 5MHz to the AFE. The calculated equivalent RC bandwidth is 404MHz and the value of R_{FLT} is 109Ω. Fig. 6 shows the signal behavior of the AFE output of both with and without RC filter. Without RC filter, the kick-back noise causes the AFE output to be unstable during the sampling period. We can observe that the kick-back noise is suppressed by the inserted RC filter and the AFE output settles back to the correct input value within sampling period.

Fig. 7 compares the FFT spectrum of the AFE output (4096 FFT-points). We can also observe that the noise floor is reduced by exploiting the RC filter. The SNR of the AFE output, which is obtained from the simulation without RC filter, was 60.2dB. On the other hand, the SNR with RC filter is 72dB. Not only the noise floor, but also the 3rd-order harmonic distortion is suppressed by 5dB.

III. System Design

Fig. 8 shows the top-level block diagram of the proposed AFE. It consists of five blocks: a low-noise amplifier (LNA), attenuator, variable-gain amplifier (VGA), anti-aliasing filter (AAF), and first-order RC filter.

A systematic noise model illustrated in [1] has been used to estimate the DR of the AFE. We assume that a full-scale range of an input signal is $0.25V_{PP}$ with the 5-nV/√Hz input-referred noise density and 20-MHz bandwidth with 0.18-μm CMOS process. An input DR of 71.9dB can be achieved with a noise floor of 22.4μV. According to the systematic noise model, the gain of the LNA have to be maximized to achieve higher SNR. Hence, the LNA provides differential output voltages as high as $1.6V_{PP}$ and its differential gain sets the maximum input signal before saturation. The corresponding gain of the LNA is 15.6dB. Impedance control optimizes SNR for applications that benefit from input impedance matching. In this work, the LNA is designed to be driven from a single-ended signal source and supports different source resistance values of 200, 400, 800, and 1600Ω.

The time gain compensation (TGC) is another important function of the AFE in this application. To decide the gain range of the AFE, two different scenarios related to the reflection distance and penetration depth have to be considered [9]. When the received echo signal is reflected from the surface of the tissues, the input signal of the LNA is relatively large. In this case, the AFE has to support low gain to avoid saturation considering the input range of the ADC. On the other hand, if the received echo signal is reflected from the deep layer of tissues, the input signal of the LNA becomes very weak. Thus the AFE must guarantee high sensitivity and

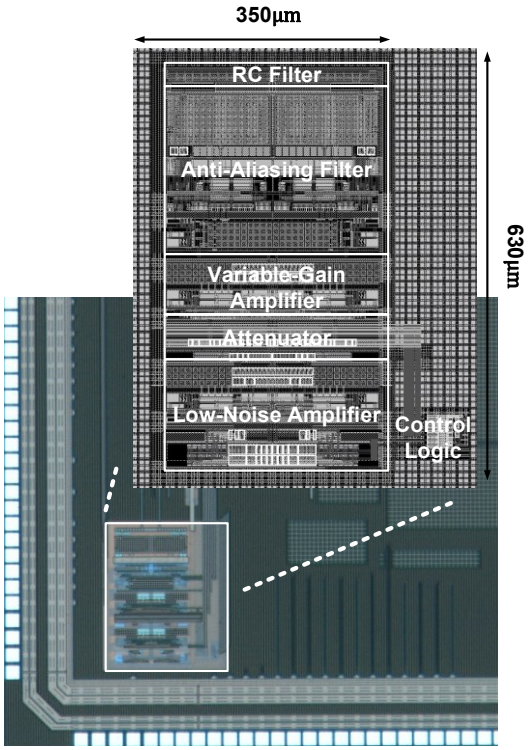

Fig. 9. Die micrograph and layout of proposed AFE.

is expected to operate with much higher gain. The output noise of the AFE should be adjusted to be lower than the ADC's noise in order to avoid SNR degradation.

In this work, the following SAR ADC has 68dB SNR and $1.6V_{PP}$ full-scale input range. The input-referred noise floor of ADC is 226µV. As a result, the gain of our AFE can be adjusted in the range -12dB to 16.125dB with a 1-bit digital controlled attenuator and a 3-bit digital controlled VGA. The total gain of the AFE including fixed gain of the LNA varies from 3.6dB to 31.725dB.

The amplifier used in both LNA and VGA consists of native-input, folded-cascode input stage and class-A output stage and each stage has continuous common-mode feedback (CMFB) circuit to maintain proper output common-mode level.

The AAF which has third-order Sallen-Key configuration drives the off-chip load or the SAR ADC. The folded-cascode Class-AB amplifier is adopted for the AAF. Both NMOS and PMOS devices are used to allow a rail-to-rail input swing. The output stage is a class-AB stage with cascode devices biasing the floating current sources. This way, high impedance is maintained at the first stage output. Higher impedance at this node indirectly implies a higher unity-gain bandwidth because the smaller compensation capacitor is required to maintain stability.

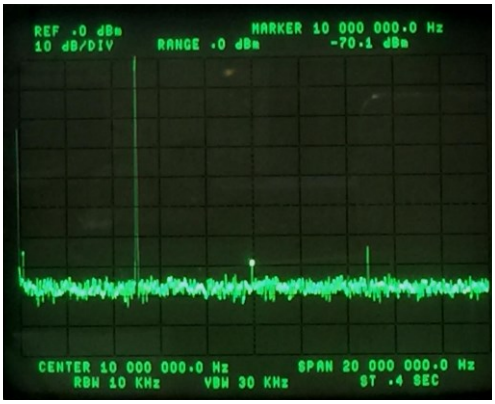

Fig. 10. Measured frequency spectrum of AFE output.

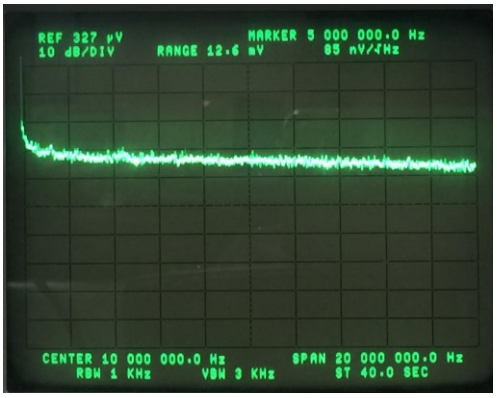

Fig. 11. Measured output-referred noise power spectrum.

IV. Experiment Results

The design has been implemented and measured in 0.18µm CMOS process. Fig. 9 shows the die micrograph and the layout of the proposed AFE. The active area is $0.22mm^2$.

Fig. 10 shows the measured frequency spectrum of the AFE's output, with a carrier frequency of 5 MHz, at the gain step of 9. The 2nd and 3rd harmonic distortion are -70.1 dB and -65.1 dB, respectively. Fig. 11 shows the measured output-referred noise spectrum under 200Ω input impedance configuration and the gain step of 15. The output-referred noise density and the noise figure measured at 5MHz are 85nV/√Hz and 9.6dB, respectively. As a result, the input-referred noise density of the AFE is 5.05nV/√Hz. A linear-in-dB gain range of [3.02, 30.6] dB was acquired with a gain error less than 1.3 dB, as shown in Fig. 12. The magnitude frequency responses measured at the gain steps of 0, 6, and 15 are shown in Fig. 13. The total current consumption of the proposed AFE is 30mA from a 1.8V supply when providing a $1.38V_{PP}$ differential signal swing. Table II shows the performance comparison between the proposed work and

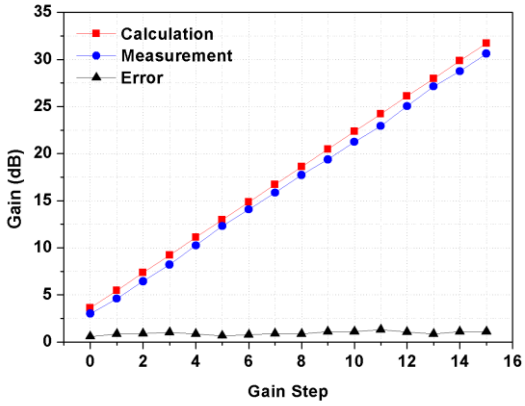

Fig. 12. Calculated and measured voltage gain of AFE versus gain step with gain error.

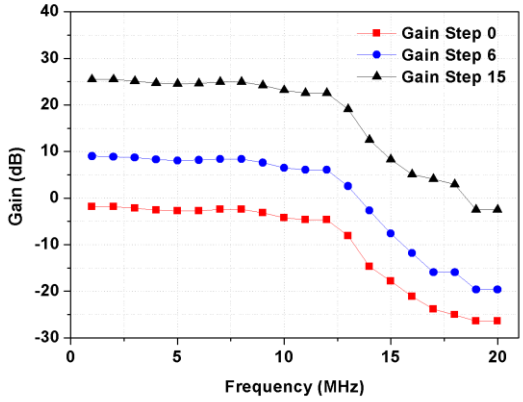

Fig. 13. Measured frequency responses of AFE.

related works available in the literature. The AD9271 employs the pipeline ADC and consumes 150mW/channel [9]. Our AFE is suitable for adopting the SAR ADCs presented in [4-8]. Because the amplifier in the AAF has a relatively wide unity-gain bandwidth and the RC filter suppresses the kick-back noise which is larger with the SAR ADC than the pipeline ADC. If our AFE and the SAR ADC are used together, the power consumption could be reduced to less than half.

V. Conclusion

The CMOS AFE for employing the low-power and high-speed SAR ADC in ultrasound imaging systems has been presented. The proposed AFE adopts a RC filter, which relaxes the bandwidth requirement of the amplifier in the AAF and reduces the kick-back noise coming from the ADC input. With the combination of our AFE and the SAR ADC, the power consumption of the ultrasound receiver can be reduced less than half. The AFE is fabricated in a 0.18µm CMOS process. In the measurement, the input-referred noise density of 5.05nV/√Hz and 28dB with less than 1.3dB gain error are achieved. The AAF has the third-order Sallen-Key configuration and the cut-off frequency is 13MHz. The AFE consumes 30mA of current from a 1.8V supply and occupies an active area of 0.22mm^2.

TABLE II. Performance Comparison with Related Works

Specifications	[3]	[9]	This work
Technology	0.18µm CMOS	N/A	0.18µm CMOS
Power (mW) / Supply (V)	56 / 1.8	150[a] / N/A	54 / 1.8
IRN (nV/√Hz)	N/A	1.4	5.05
Noise figure (dB)	15.6	4.4	9.6
Impedance control	50, 100, 200, 1000	50, 100, 200	200, 400, 800, 1600
Gain range (dB)	48.9	30	28
Number of gain step	16	Continuous gain control	16
AAF bandwidth (MHz)	Not implemented	8 to 18	13
Active Area (mm^2)	0.68	N/A	0.22

[a] ADC power consumption is included.

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