Low Noise Output Stage for Oversampling Audio DAC

Yujin Park, Han Yang, Hyunjong Kim, Jun Soo Cho, and Suhwan Kim

Electrical and Computer Engineering and Inter-university Semiconductor Research Center
Seoul National University, Seoul, 151-744, Korea
Email: suhwan@snu.ac.kr

***Abstract*—This paper presents a low noise output stage of oversampling audio digital-to-analog converter (DAC). The proposed glitchless switched capacitor DAC (GSC-DAC) eliminates the penalty of a constrained signal range and a signal distortion caused by return-to-zero signals in SC-DAC that is an essential part in order to convert the digital signal into the analog signal. By using a track and hold circuit and deglitching method in GSC-DAC, the low noise is efficiently achieved. The results of post layout simulation show the noise performance improvements of 21dB on average of SNR, SNDR, SFDR and THD in comparison with the absence of the proposed techniques.**

Keywords—audio DAC, analog output stage, track and hold circuit, switched capacitor DAC

I. INTRODUCTION

High-quality sound is the driving force for modern digital audio devices such as professional and general consumer audio applications. The high-resolution audio digital-to-analog converter (DAC) over 20bit is a current trend to support a complete stereo solution with a highly integrated chip. To meet the demands, the oversampling technique has been a popular solution because it is a cost effective alternative compared to Nyquist-rate data converters [2]. The oversampling audio DAC generally consists of digital signal processing (DSP) and output stages as shown in Fig. 1. The DSP stage produces several times oversampling ratio (OSR) to achieve higher bit-resolution. The interpolation performs a multi-step up-sampling to OSR and a low-pass filtering. The Σ-Δ modulator is a noise shaper. The binary-to-thermometer decoder provides the suitable digital signals to the internal DAC. The output stage comprises internal DAC and analog filter. The internal DAC transforms output signals of DSP stage into analog output. The analog filter drives it to the outside of the chip with filtering the audible frequency.

The output stage determines an upper limit of overall noise performance [7], [8]. There are a number of considerations for negligible in-band noise. In terms of circuit implementation, one of the most important things is what kind of internal DAC is used, and how to combine it with an analog filter. Current steering and switched capacitor (SC) topology are commonly used for internal DAC. Current steering DAC has an advantage of high speed and low power on account of a small voltage step of non-return-to-zero (NRZ) compared to a large voltage step of return-to-zero (RZ) in SC-DAC. On the other hand, SC-DAC provides low noise with medium speed since the output waveform of RZ is free at inter-symbol-interference (ISI) which makes signal distortion. In addition, the noise performance of capacitor units that is the basic element in SC-DAC is fundamentally superior to that of transistor units in current steering DAC in terms of flicker noise. Despite these noise merits of SC-DAC, when connected to an analog filter, the large voltage step of RZ signals causes the signal distortion and the limitation of output range reduced by a factor of 2 at the final output, results in performance degradation. Dual RZ method [1] is an alternative way to eliminate this problem, where two RZ signals having different phases are summed. However, the approach requires additional power dissipation for a summing circuitry and more careful implementation in order to match the phase difference which can create a glitch between original phase and copied phase.

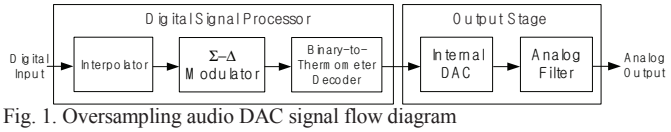

Fig. 1. Oversampling audio DAC signal flow diagram

In this paper, we present an output stage with glitchless SC-DAC (GSC-DAC) which uses a track and hold (T/H) circuit and deglitch method. It decreases the problems caused by the RZ signals while maintaining its advantages. By utilizing a T/H circuit, a glitch phenomenon comes into a major noise source. We also introduce a deglitching method in the following sections. As a result, the GSC-DAC leads to performance improvements of 21dB on average in post layout simulation.

II. ARCHITECTURE OF GSC-DAC

Generally, a T/H circuit has been used in current steering DAC to isolate switching glitches for low distortion and ISI [3], [4]. Unlike the current steering DAC, the T/H circuit is adopted at SC-DAC in our design. This approach provides design simplicity and mismatch tolerance compared to dual RZ method [1] because it only needs one switch and one hold capacitor.

The direct connection between SC-DAC and analog filter is not effective since it works a bottleneck of the overall performance of Σ-Δ audio DAC. Fig. 2 shows the conceptual output waveforms when T/H circuit is not included (a) and included (b). The output of SC-DAC repeats a conversion signal

This research was supported by IC Design Education Center (IDEC) and the IT R&D program of MOTIE/KEIT [10044497, Development of BCDMOS Technology Process & IPs based on AEC-Q100 for Automotive Applications; 10048843, Automotive ECU SoC and Embedded SW for Multi-domain Integration].

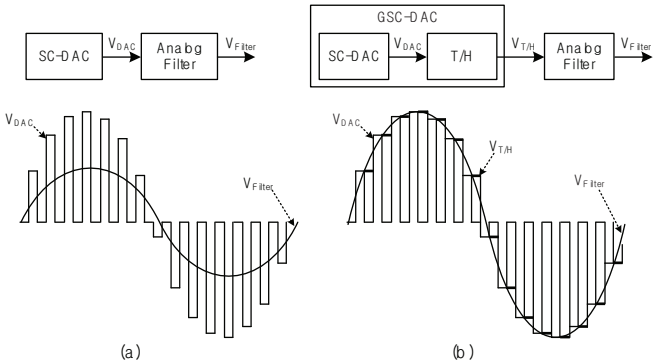

Fig. 2. Conceptual waveforms without (a) and with (b) a T/H circuit. The bold lines in the waveform of (b) represent the hold mode at T/H circuit.

in a half-cycle and a common-mode voltage signal in the rest of the half-cycle. These well-known waveforms serve to improve the noise performance because of the operation of SC-DAC with non-overlapped clock, which is less sensitive at clock jitter and the mismatching of current cell than that of current steering DAC [7]. As shown in Fig. 2 (a), however, the final output (V_{Filter}) has a limitation of targeted full scale by filtering V_{DAC} in analog filter, which results in signal loss of 6dB. Furthermore, the large voltage step of RZ signals causes a signal distortion by spurious tones and a power dissipation to secure a signal swing range. On the other hand, the GSC-DAC could be an effective alternative as shown in Fig.2 (b). It converts a large step waveform of the RZ signals of SC-DAC into a small step waveform as if a hold mode at T/H conceals a reset state. At least, it provides an improved SNR of 6dB and solves the limited signal swing of V_{Filter}.

However, the T/H circuit with SC-DAC produces a serious glitch that is different from that of the current steering DAC in which the glitch occurs at the crossing point of active current cells. Whereas, the glitch in SC-DAC occurs at a track mode as shown in Fig. 3(a). The output of the thermometer-decoded Σ-Δ modulator is sampled in the reset state of the SC-DAC clock. After the signal sampling is finished, SC-DAC starts converting digital signal into analog signal at a conversion state. At the same time, the output ($V_{T/H}$) of the T/H circuit follows the targeted analog voltage (V_{DAC}). Consequently, the glitch occurs during V_{DAC} arrives at steady-state.

To avoid the glitch phenomenon, we propose a deglitching period suitable to RZ signals. It is easily implemented by the timing adjustment of the T/H clock. Fig. 3(b) shows the timing diagram about the deglitching period. The track mode waits until the output of SC-DAC, V_{DAC}, is stabilized, and then the T/H circuit receives that. Therefore, this simple deglitching approach enables the noise performance of the GSC-DAC to be maximized.

III. CIRCUIT IMPLEMENTATIONS

Our output stage consists of a GSC-DAC and two analog filters as shown in Fig. 4. The fully differential SC-DAC in GSC-DAC is applied to direct-charge-transfer (DCT) technique where the outputs of the DSP stage are directly stored in capacitor

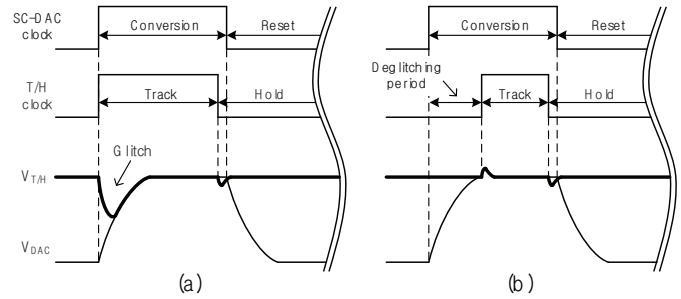

Fig. 3. Timing diagram and output waveforms without (a) and with (b) deglitching period.

arrays of the SC-DAC without additional sample-and-holder [5], [6]. The capacitor array consists of 30 unit capacitors and logic gates in order to synchronize and sample the output of the DSP stage along with a SC-DAC clock, P1 and P2. It operates at non-overlapped clock with 6.144MHz. P1D and P2D are the delayed phase at falling edge of Pl and P2 as a role of bottom plate sampling to remove an offset by charge injection. The input data is sampled during P1, and then transferred during P2. The deglitching period is applied at P3. The capacitors of C1 and C2 are about 628fF and 22.6pF respectively. A fully differential folded cascode amplifier that is commonly used is adopted with a switched capacitor common-mode feedback circuit.

The T/H circuit uses a half dummy switch to minimize the effect of charge injection of P3, not depicted in Fig. 4. It does not include a unit-gain buffer that generates additional intrinsic noise. Therefore, the drivability of the amplifier in SC-DAC includes the T/H circuit and analog filter. The sampling capacitor C3 is 6pF. It is enough because a KT/C noise is reduced by the effects of OSR. In addition, the noise contribution is not dominant at track mode, but at hold mode. In other words, the signal at track mode is approximately equal to the output of internal DAC. On

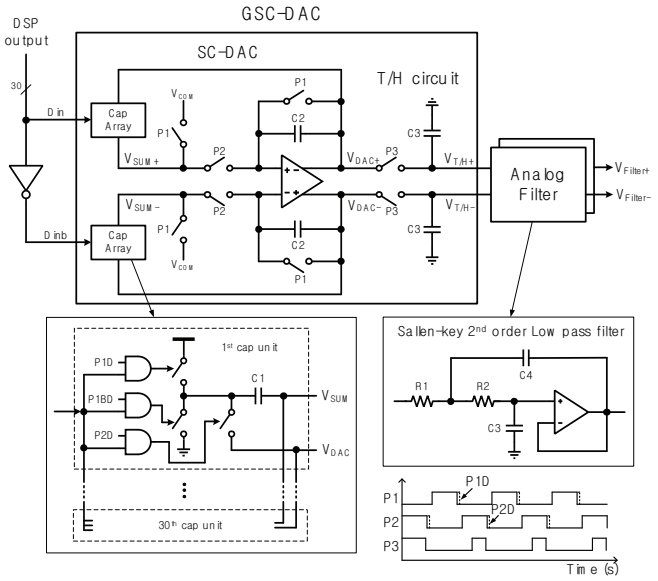

Fig. 4. Output stage circuit

the other hand, the signal at hold mode includes the KT/C noise. As a result, the noise by T/H is averaged at the analog filter stage.

Second-order Sallen-Key LPF is used in the analog filter. This reconstructs the output signal of the T/H circuit to a continuous analog signal by reducing high frequency noise components which are over audio band from 20Hz to 20kHz. The cut-off bandwidth meets the requirement of audio band. The values of R1, R2, C3 and C4 for the bandwidth are settable to counteract the effect of process variation. The default value is 20kΩ, 20kΩ, 20pF and 20pF, respectively. The op-amp is adopted in a typical current mirror topology that features a rail-to-rail output swing to reduce the distortion by limited slew-rate. The full scale swing range is 1.414V at a single-ended output. It drives a 20kΩ and 5pF grounded load at the outside the chip.

IV. Simulation Results

The proposed output stage has been implemented in a 1-poly 5-metal 0.13um CMOS technology with 3.3V supply voltage. The layout of the output stage section is shown in Fig. 5. The total area is 0.86mm^2 except the bypass capacitors and pads. The size of SC-DAC, T/H circuit and analog filter is 0.59mm^2, 0.02mm^2, 0.25mm^2, respectively. The T/H circuit occupies only 2.5% of the total area. The non-overlapped clock unit within SC-DAC includes the deglitching method whose area is negligible.

To evaluate the effects of GSC-DAC, we have performed a transient noise simulation using Spectre®. This simulation covers every possible aspect of noise sources such as intrinsic noises at passive- and active-devices, and the adverse effects of the clock feedthrough, the charge injection, the slew limit and signal coupling by parasitic RC at transient activation. In addition, the digital inputs of SC-DAC are the noise-shaped outputs of the DSP stage that are included in our simulation for more realistic values. The remaining difference between extracted absolute values in this paper and expected silicon values would be dependent on matching quality of the noise model parameters which is used in our design.

An agreeable change of each waveform by the T/H circuit and the deglitching method is depicted in Fig. 6. As mentioned above, a conventional structure without the T/H circuit and the deglitching method limits the output swing range as shown in Fig.

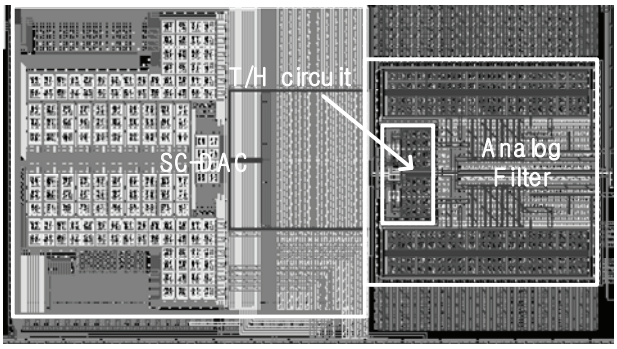

Fig. 5. Layout of the output stage section for a Σ-Δ audio DAC

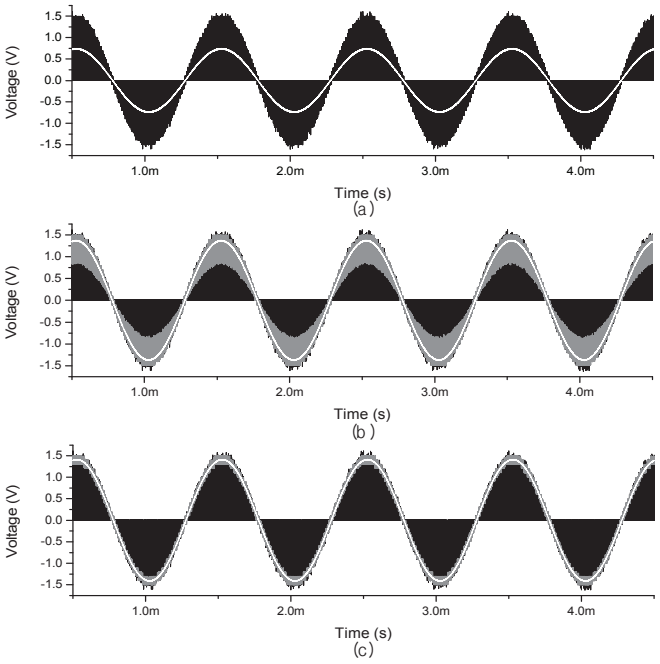

Fig. 6. Simulated transient waveforms without a T/H circuit (a), with a T/H circuit and without deglitching method (b), and with both (c). The black line is the output (V_{DAC}) of SC-DAC. The gray line is the output ($V_{T/H}$) of the T/H circuit. The white line is the output (V_{Filter}) of the analog filter. The outputs are plotted to a differential type, V_{OUTP}-V_{OUTN}.

6(a), results in a signal loss and distortion. These noise performance degradations after passing through the analog filter is over 30% in comparing between V_{DAC} and V_{Filter} as shown in Fig. 7, where key performance indexes are signal-to-noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR)

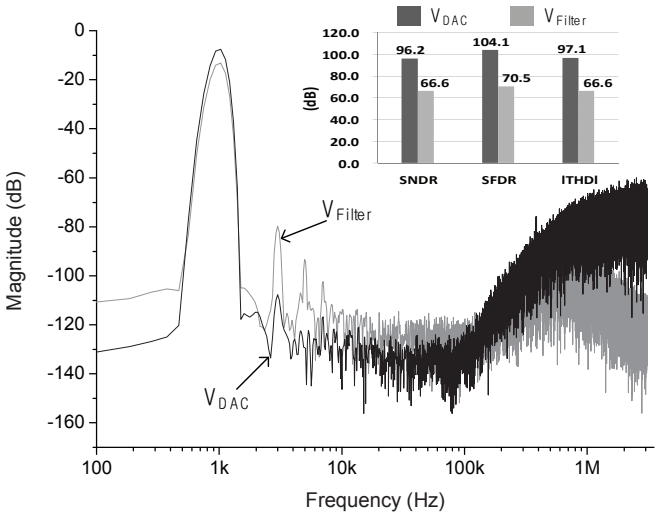

Fig. 7. Simulated FFT response of internal nodes when without a T/H circuit. The sampling rate and input frequency are 6.144 MHz and 1 kHz respectively. The band-limit is 24 kHz to calculate SNDR, SFDR and THD in full scale tone.

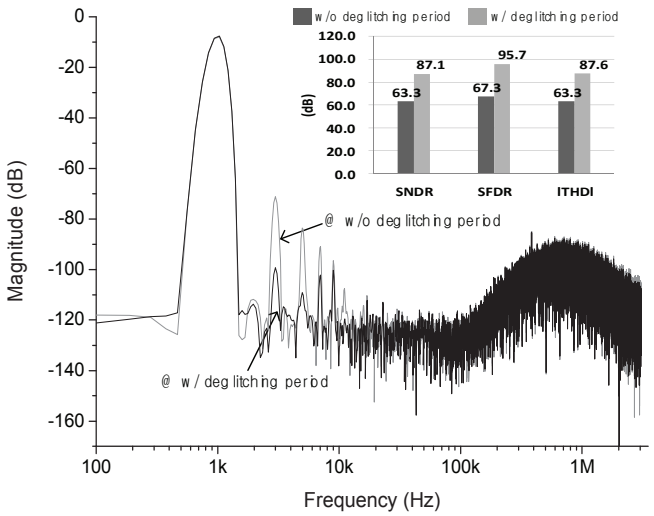

Fig. 8. Simulated FFT response of output waveforms of analog filter when the deglitching period is applied (black line) and not applied (gray line). The simulation condition is the same as Fig. 7.

and total harmonic distortion (THD). The simulation results do not include the T/H circuit.

While using the T/H circuit to overcome the problem, it generates a serious glitch at the output of the T/H circuit in Fig. 6(b), which deteriorates the harmonic performance especially. In other words, there can be better noise performances when the T/H circuit is not in use, if the deglitching period is not applied. For example, the SNDR of 63.3dB where the T/H circuit is used and the deglitching period is not applied as shown in Fig. 8, is slightly worse than the SNDR of 66.6dB where the T/H circuit is not used as shown in Fig. 7. Namely, the adverse effect by the glitch in the T/H operation of RZ signals is critical.

The deglitching method eliminates the glitch phenomenon as shown in Fig. 6(c), which maximizes the effects of utilizing the T/H circuit for RZ signals. In Fig. 8, the FFT response shows that applying the deglitching period significantly alleviates the spurious tone. The improvement ratio is about 30% at all simulated performance indexes. The performance comparisons with and without proposed techniques is depicted in Fig. 9. The results are the summary of FFT response in Fig. 7 and Fig. 8. Table I is the design summary of the proposed output stage.

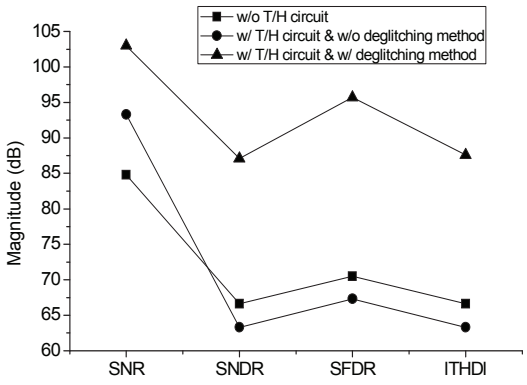

Fig. 9. Comparisons with and without proposed techniques. The performance is the result at the output of analog filter including external loads of 20kΩ and 5pF.

TABLE I. DESIGN SUMMARY

Process	0.13um CMOS
Supply	3.3 V
Differential output swing	2.828 V_{PP}
Clock frequency	6.144 MHz
Power dissipation	12.54 mW (GSC-DAC: 7.26mW, Analog Filter: 5.28mW)
Size	0.86mm^2 (GSC-DAC: 0.61mm^2, Analog Filter: 0.25mm^2)

V. CONCULUSION

A GSC-DAC for oversampling audio DAC based on the T/H circuit and deglitch method was proposed in this paper. The design approaches make it attractive for the output stage with a SC-DAC to achieve low noise performance. The T/H circuit is useful as a first filter in between SC-DAC and analog filter for a continuous-time reconstruction, and its effectiveness can be realized through deglitching method. In other words, the utilization of the T/H circuit is useless if the deglitching method is no considered. The waveforms at each internal node were also introduced. The proposed techniques have been validated by the rigorous simulation with a 0.13um CMOS technology. The results show the improvements of SNR, SNDR, SFDR and THD by 18.2dB, 20.5dB, 24.5dB and 21.0dB, respectively.

REFERENCES

[1] R. Adams and K. Nguyen, "A 113 dB SNR oversampling DAC with segmented noise-shaped scrambling," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 1871–1878, Dec. 1998.

[2] D. Su, "Oversampling Digital-to-Analog Conversion," Ph.D. dissertation, Stanford Univ., Aug. 1994.

[3] W. Kester, The Data Conversion Handbook, Burlington, MA: Newnes, 2004.

[4] K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, and P. Baginski, "A 108 dB SNR 1.1 mW oversampling audio DAC with a three-level DEM technique," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2592–2600, Dec. 2008.

[5] I. Fujimori, A. Nogi, and T. Sugimoto, "A multibit delta-sigma audio DAC with 120-dB dynamic range," IEEE J. Solid-State Circuits, vol. 35, no. 8, pp. 1066–1073, Aug. 2000.

[6] J. A. C. Bingham, "Applications of a direct-transfer SC intergrator," IEEE Trans. Circuits Syst., vol. CAS-31, pp. 419-420, Apr. 1984.

[7] I. Fujimori and T. Sugimoto, "A 1.5-V 4.1-mW dual-channel audio delta-sigma D/A converter," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 1879–1886, Dec. 1998.

[8] Y. Liu, J. Gao, and X. Yang, "24-bit low power low cost digital audio sigma-Delta DAC", Tsinghua science and technology, VOL 16, NO. 1, February 2011.