A 9-bit, 110-MS/s Pipelined-SAR ADC Using Time-Interleaved Technique with Shared Comparator

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***Abstract*— A 9-bit 110-MS/s pipelined-SAR ADC is proposed. To alleviate the design tradeoff between conversion rate and power consumption, the design adopts a voltage-mode open-loop amplifier and a time-interleaved SAR architecture with comparator sharing. The ADC simulated in a 65-nm CMOS technology achieves an ENOB of 8.63 bits near the Nyquist input frequency at the sampling rate of 110MS/s. The power consumption is 7.9mW, resulting in 181.3fJ/conversion-step of Figure of Merit (FoM).**

Keywords—Analog to digital converter, pipelined ADC, SAR ADC, time-interleaved technique

I. INTRODUCTION

An ADC with a medium speed and a medium resolution is an essential component for 802.11/a/b/g wireless LAN systems and digital TV applications [1]. The pipelined ADC architecture is suitable to the sampling rate and the resolution than any other ADC type [2].

However, pipelined ADCs require power hungry op-amps with high gain-bandwidth to achieve good performance [3]. Furthermore, CMOS technology scaling simultaneously, coupled with lower supply voltage, causes problems in the design of amplifier [4]. Digital calibration [5], open-loop amplification [6] and comparator-based switched-capacitor (CBSC) circuits [7], [8] have been proposed to solve these limits.

Meanwhile, successive approximation register (SAR) converters have evident advantages from energy saving perspective. SAR ADCs can achieve low-power consumption, due to simple conversion procedures and the absence of power consuming op-amps. Moreover, SAR ADCs can be easily implemented in deep-submicron technologies because circuits of minimal analog complexity such as a comparator and switches are only used. However, it is difficult to operate SAR ADCs with a high conversion rate, due to the large number of decision cycles. Another challenge is the implementation of the accurate and small capacitor array. Because a large unit capacitance is required to minimize effects of capacitor mismatching, the total capacitance is typically larger than the value bound by the kT/C noise [9], [10]. To overcome these problems, SAR ADCs adopt digital error correction with additional circuits and redundancy cycle [11].

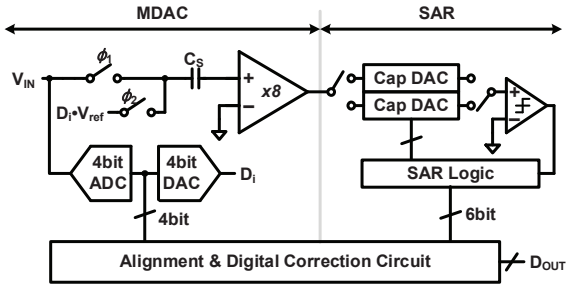

Fig. 1. Proposed ADC architecture

In this paper, to overcome the above problems, we propose the pipelined-SAR ADC which adopts an open-loop amplifier that replaces the high gain and wide bandwidth op-amp in the MDAC. Using an SAR ADC as the second stage can reduce the capacitor size. Furthermore, time-interleaving the SAR ADC improves the conversion rate. Our scheme has been verified through a 9-bit 110MS/s pipelined-SAR. Its power consumption is improved by using an open-loop amplifier in the MDAC, using scaled residue, and sharing the comparator in the time-interleaved SAR. The limitations of high conversion rate and large capacitor array in SAR ADC are alleviated by adopting a time-interleaved technique and using an MDAC structure in the first stage.

II. SYSTEM ARCHITECTURE

Our pipelined-SAR ADC consists of a 4-bit MDAC stage, a 6-bit SAR ADC and digital logic for bit alignment and digital error correction, as shown in Fig. 1. The 4-bit MDAC

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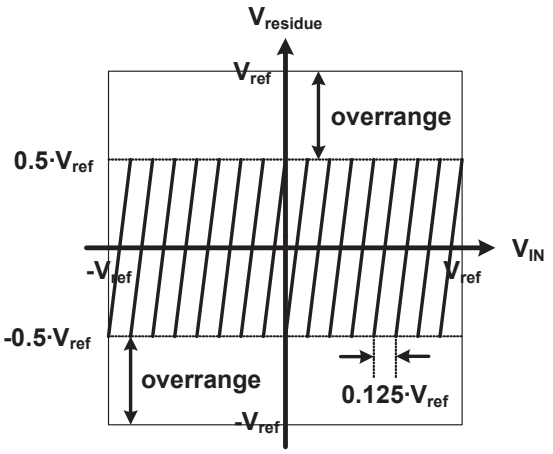


Fig. 2. Conversion characteristic of the 4-bit MDAC

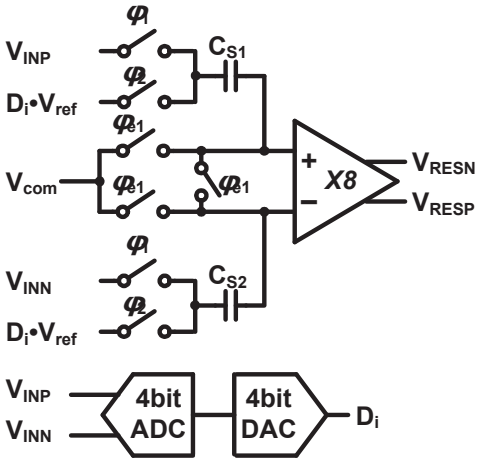


Fig. 3. Schematic diagram of MDAC

has a 1-bit redundancy for error correction. Fig. 2 shows transfer curves of the first stage. Due to scaled residue of the MDAC, the constraints of the output swing are relaxed. In the second stage, the time-interleaved SAR ADC consists of the two capacitor DACs and a shared comparator.

A. Multiplying DAC (MDAC)

To avoid the need for a high-gain and wide bandwidth op-amp, we adopt the open-loop amplifier in the MDAC, as shown in Fig. 3. Also, in order to eliminate the input signal dependency, the MDAC adopts the bottom plate sampling scheme in the sampling phase.

Fig. 4(a) shows the whole schematic diagram of the gain tunable differential amplifier. The first and second stages in the gain tunable amplifier use a differential amplifier with source degeneration. The final stage is a source follower amplifier that extends the bandwidth and shifts the DC level for the input range of the following SAR ADC.

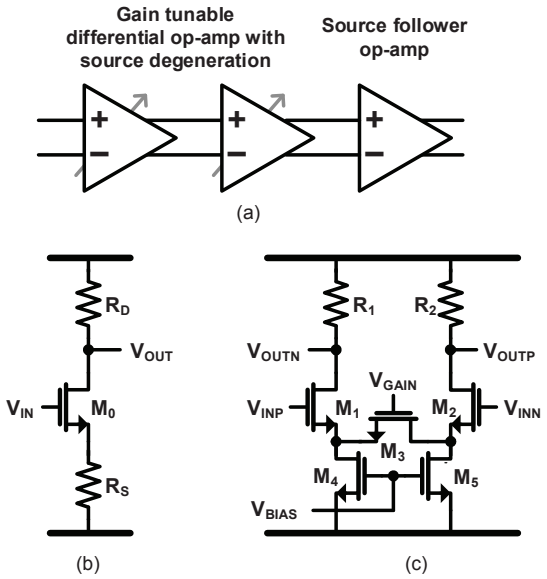


Fig. 4. Schematic diagrams of (a) Gain tunable amplifier, (b) common-source amplifier with source degeneration and (c) differential amplifier with source degeneration

In designing an open-loop amplifier for the MDAC, its linearity and gain attenuation must be carefully considered. First, in an MDAC that uses a closed-loop amplifier, the residue error is determined by the gain of the op-amp, and the mismatch of the sampling and feedback capacitors. In the MDAC with open-loop amplifier, however, the residue error is determined by the linearity of the op-amp. Therefore, it is extremely important that the linearity of the open-loop amplifier is improved in order to prevent performance degradation such as harmonic distortion due to the non-linear amplification. Fig. 4(b) is the schematic of a common source amplifier with source degeneration, and the operation equation is as follows:

$$V_{OUT} = -\frac{g_m R_D}{1 + g_m R_S} V_{IN},$$

where g_m is the transconductance of the input transistor (M_0), R_D is the load resistor, and R_S is the source degeneration resistor, Since most of the change in V_{IN} is seen across the R_S, it can boost the linearity of the amplifier. Although the gain of the amplifier is degraded, the gain needed in an open-loop amplifier of an MDAC is only 2 to power of the number of bits in MDAC. Fig. 4(c) shows the differential open-loop amplifier with source degeneration with linearity enhancement intended for the MDAC. The other point is that, due to charge sharing, the parasitic capacitance of the input node of the open-loop amplifier can be controlled by V_{GAIN}. Controlling the gate voltage of M_3 has the same effect as source degeneration resistor R_S.

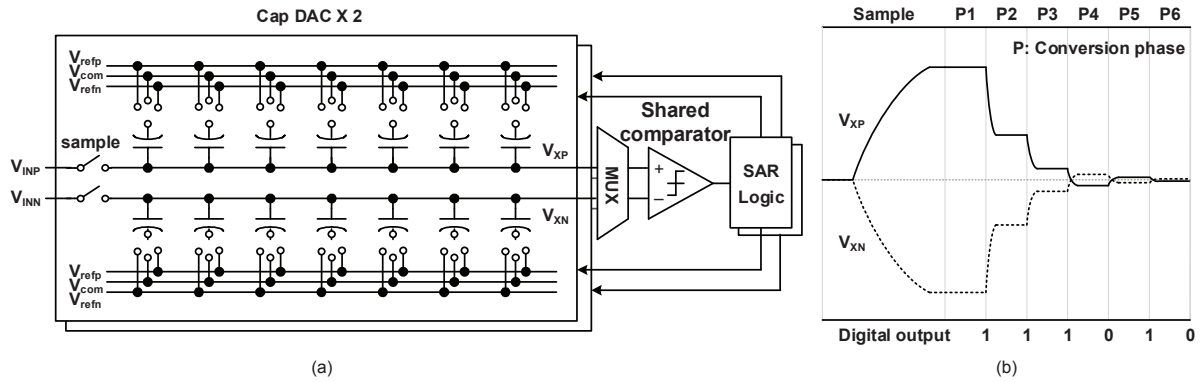


Fig. 5. (a) Schematic diagram of time-interleaved SAR ADC (b) Waveforms of V_{XP} and V_{XN}

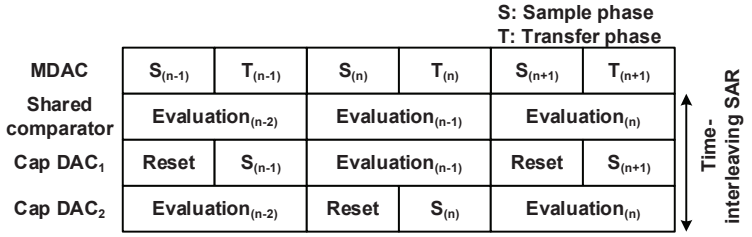


Fig. 6. Timing diagram of pipelined-SAR ADC

B. Time-interleaved SAR ADC with shared comparator

In conventional SAR ADCs, the primary sources of power consumption are the comparator, capacitor network, and the digital control circuit. To reduce power consumption, we adopt a shared comparator in the time-interleaved SAR ADC with two capacitor DACs as shown in Fig. 5(a). The power consumption of the capacitor network is reduced by the switching procedure of our capacitor DAC. Due to the output range of the MDAC, the reference voltages of the SAR are V_{REFP}, V_{COM} and V_{REFN}. In the sample phase, the bottom plates of the capacitors are connected to V_{INP} and V_{INN}, and the top plates of the capacitors are connected to V_{COM}.

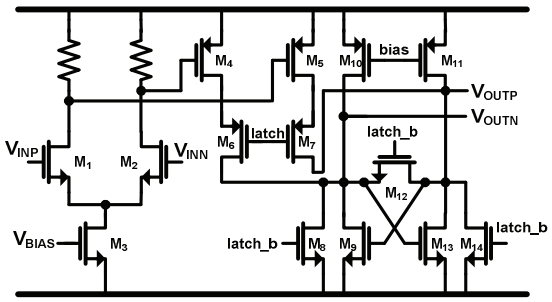


Fig. 7. Comparator in SAR ADC

According to the output of comparator, the top plates of the largest capacitor are connected to V_{REFP} or V_{REFN}. In this way, the SAR ADC decides the 6-bit digital output. Fig. 5(b) shows the waveforms of V_{XP} and V_{XN}.

The system clock frequency needs to be over 12 times higher than the clock frequency of the 4-bit MDAC. Because the first half cycle of system clock is used for sample phase, the SAR ADC should make the 6-bit conversion within the second half cycle. Therefore, it is important to reduce the power consumption of clock network. In the proposed SAR ADC, the frequency constraint of the ADC clock can be reduced by using an internal clock generator which adopts a gated ring oscillator.

Fig. 6 shows the timing diagram of the pipelined-SAR ADC including the MDAC and the time-interleaved SAR ADC. Two capacitor DACs alternately sample the residue of the MDAC stage during its transfer phase. After the evaluation phase, the capacitor DAC reset the charge of the analog MUX input to avoid memory effect. Therefore, total latency of the pipelined-SAR ADC is two cycles.

The comparator in the SAR ADC has several constraints such as meta-stability, static power consumption and kick-back noise. As shown in Fig. 7, the SAR ADC uses a dynamic comparator to reduce static power consumption. To avoid kick-back noise, it adopts a source follower scheme with M_4 and M_5.

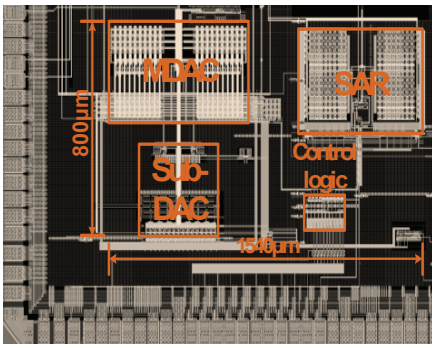
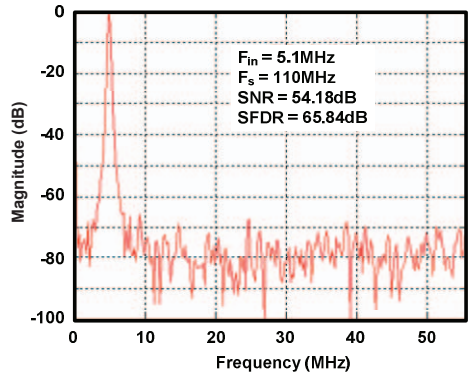
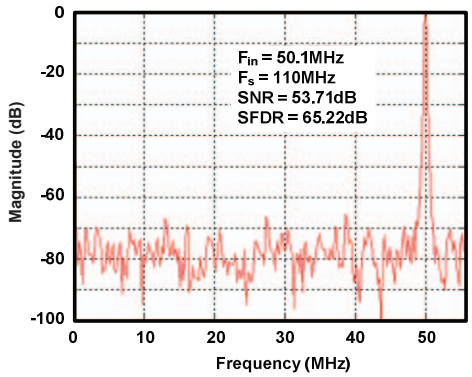


Fig. 8. Layout of pipelined-SAR ADC



(a)



(b)

Fig. 9. FFT plot of simulated data (a) F_{in} = 5MHz and (b) F_{in} = 50MHz at a sampling rate of 110MS/s

III. Simulation Results

Fig. 8 shows the layout of the test circuit and the pipelined-SAR ADC composed of the MDAC, the SAR and digital logic. This prototype is designed in 65nm CMOS technology.

Fig. 9(a) and (b) show the FFT plots of simulated data with F_{in} of 5.1MHz and F_{in} of 50.1MHz at a sampling rate of 110MS/s. The signal-to-noise ratio (SNR) and the spurious-free dynamic-range (SFDR) are 53.71dB and 65.22dB, respectively. With a near Nyquist-rate sinusoidal input, effective number of bits (ENOB) is 8.63 bits. Table I shows performance summary of the proposed pipelined-SAR ADC. Operating at an 110MS/s sampling rate, with a $1V_{P-P}$ range, it consumes 7.9mW at the supply voltage of 1.2V. Table II summarizes the performance of the proposed ADC and compares it with that of previous works incorporating pipelined-SAR architecture in terms of the ENOB and other metrics.

TABLE I. Performance Summary

Supply voltage	1.2V
Technology	65nm 1P6M CMOS
Resolution	9-bit
Sampling rate	110MS/s
Input range	$1V_{P-P}$
SNR	53.71 dB (F_{in}=50.1MHz)
SFDR	65.22 dB (F_{in}=50.1MHz)
Power consumption	7.9mW
Active area	0.6mm^2
FoM	181.3fJ/conversion-step

TABLE II. Comparison between the proposed ADC and other pipelined-SAR ADCs

Parameter	[4]	[12]	[13]	This work
Process (nm)	65	65	65	65
Resolution (bit)	12	10	9	9
Supply (V)	1.3	1.1	1.0	1.2
Power (mW)	3.5	1.21	3.14	7.9
Sampling rate (MS/s)	50	40	90	110
Area (mm^2)	0.16	0.06	0.11	0.6
FoM (fJ/conv.)	52	65	247	181.3
ENOB (bit)	10.4	8.9	7.14	8.63

IV. Conclusion

We propose a pipelined-SAR ADC using time-interleaved SAR with a shared comparator to reduce the power consumption. Also, using an open-loop amplifier in MDAC can avoid designing a high performance op-amp in deep-submicron processes and improve power consumption. The SNR and SFDR are 53.71dB and 65.22dB, respectively at 110MS/s. The prototype ADC achieves an ENOB of 8.63 bits at near Nyquist-rate, and a figure-of-merit of 181.3fJ/conversion-step. The ADC is designed in 65 nm CMOS.

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