Differentiating ASK Demodulator for Contactless Smart Cards Supporting VHBR

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***Abstract*—This brief proposes an amplitude shift keying (ASK) demodulator that uses switched-capacitor differentiators to make it compliant with the very high bit rate amendment to the ISO/IEC 14443 standard for contactless smart card applications. These differentiators detect transitions in modulated ASK signals with a carrier frequency of 13.56 MHz at data rates up to 6.78 Mb/s. The demodulator has been implemented in 0.18 μm CMOS technology. The total power consumption is under 350 μW. Measured results confirm correct operation, and it is further shown that this differentiating scheme allows the modulation index to be reduced to 2.56%.**

***Index Terms*—Amplitude shift keying (ASK) demodulator, contactless smart card, switched-capacitor differentiator, very high bit rate (VHBR).**

I. Introduction

THE demand for smart cards is growing rapidly, due to their wide range of applications. Smart cards are more durable and secure, and can store more data than magnetic cards. Amplitude shift keying (ASK) modulation is typically used for communication with smart cards that operate at this rather low data rate, mainly due to the simple architecture and low circuit complexity, and low power consumption [1]. The transfer of data by ASK modulation is standardized in ISO/IEC 14443, with a carrier frequency of 13.56 MHz. Early versions of the standard specified data bit rates in the range from 106 to 848 kb/s. However, the emergence of applications such as electronic passports and near-field communication devices, which require a faster transfer of data have caused the standard to be extended to include a very high bit rate (VHBR) amendment, which supports data rates up to 6.78 Mb/s.

Conventional ASK demodulators, which only use envelope-based demodulation [2], cannot run at these higher speeds, in part because of their sensitivity to amplitude noise [3], [4] and the increased intersymbol interference due to the band limited channel. The reduction in the modulation index to 10%, as specified for Type B cards in the ISO/IEC 14443 standard, will exacerbate the problem. The emergent alternative is the use of phase shift keying (PSK) modulation [5], [6]. However, PSK demodulators are complicated and require much more circuitry than ASK demodulators. The simplicity of ASK modulation can be retained if a new approach can be found to manage increased data rates.

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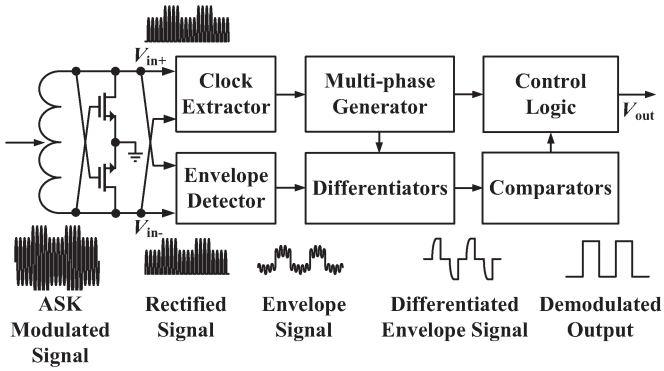

Fig. 1. Block diagram of the proposed differentiating ASK demodulator.

In this brief, we propose a differentiating ASK demodulator, shown in Fig. 1, that is compliant with the VHBR amendment to the ISO/IEC 14443 standard. These higher data rates are achieved by differentiating the envelope of the input ASK modulated signal in the demodulator using a switched capacitor, instead of comparing the envelope signal directly to a reference voltage, which is what happens in conventional designs.

II. Conventional ASK Demodulator

The advantages of ASK modulation include simple hardware, low power consumption, and ease in recovering the carrier. Its drawbacks are a low bit rate, low transmission power [7], and the problems caused by the varying average voltage of the ASK modulated signal [8]; a critical issue in contactless devices, which are often subject to widely varying channel conditions. Reducing the modulation index increases the overall power efficiency, because energy is supplied more steadily. However, a low modulation index requires the detection of very small variations in amplitude and is therefore challenging.

A conventional ASK demodulator consists of an envelope detector, an average detector, and a comparator. The envelope detector is made up of a diode and a low-pass filter. The ASK modulated signal is rectified by the diode, and then the low-pass filter generates the envelope of the signal. The average detector is basically another low-pass filter. The comparator compares the amplitude of the signal envelope with its average value and generates the demodulated ASK output.

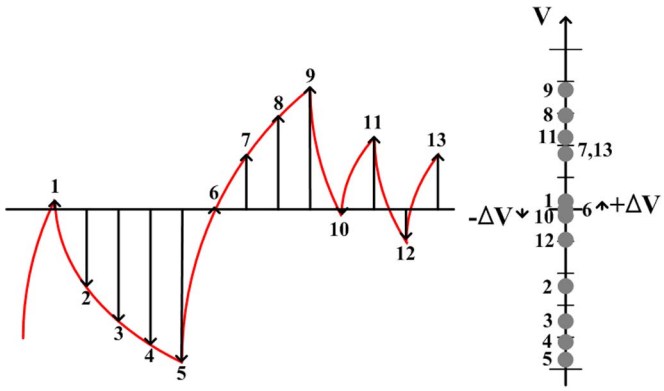

Fig. 2. Principle of the conventional ASK demodulation.

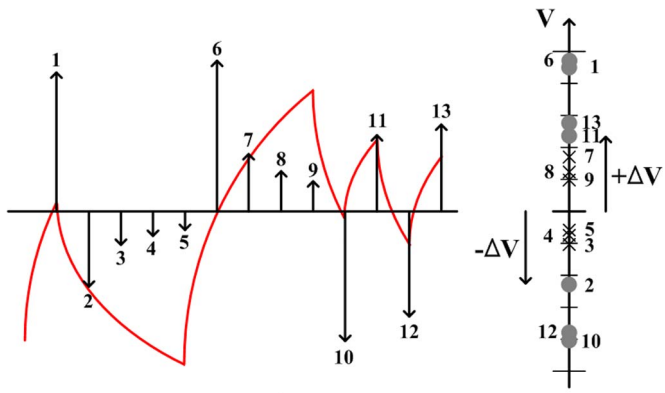

Fig. 3. Principle of the proposed differentiating ASK demodulation.

Fig. 2 shows the envelope of the ASK modulated signal and values sampled at a fixed time-step, labeled 0–13. When data bit rates are high, the envelope of the input signal will not have settled adequately due to the RC time constant, and thus, the slope is not steep. This small slope reduces the minimum voltage difference, i.e., ΔV, which has to be distinguished by the comparator. In the example of Fig. 2, the worst case occurs at sampling points 6 and 10, where sudden transitions occur after a long run of zeroes or ones. To discriminate the correct values at points 6 and 10, which are one and zero, respectively, would require an expensive comparator, and the demodulator itself would have to cope with more noise and an increased comparator offset.

To meet the requirements of the VHBR amendment, the comparator must be able to provide an output that is correct with an input difference range of a few millivolts, or else an amplifier must be inserted into the input stage. Both approaches involve greatly increased power, making them unsuitable for contactless smart cards, which have power limitations.

III. Differentiating ASK Demodulator

Our demodulator distinguishes the data signal from the differentiated input signal, rather than looking for small changes in the absolute magnitude of the input signal. Not only does this allow low modulation indexes and high data bit rates, it also relieves the varying average voltage issue.

Differentiating the signal relieves the requirements on the comparator, because it increases the voltage difference that has to be distinguished. In the differentiated envelope in Fig. 3, the values of ΔV at points 6 and 10 are much larger than those in Fig. 2. The worst case now occurs at the sampling points between the large voltage transitions, points 2 and 11, but even at these points ΔV is larger than the voltages obtained by directly comparing envelopes, allowing a more relaxed comparator or a lower modulation index.

As the length of the continuous data strings of zeros or ones increases, however, ΔV decreases (points 5 or 9). In our case, the maximum length of the long run is limited as defined in ISO 7816-3 standard (i.e., transmitting a Start Bit, 8-bit Data Bits, a Parity Bit, and 2-bit Guardtime). Regarding the maximum length of the long runs, the RC time constant of our demodulator has been designed, and it was sufficient for operation at VHBR.

Our differentiating ASK demodulator operates in three phases: sampling phase, idle phase, and differentiating phase. In sampling phase, the envelope of the input signal is sampled to a sampling capacitor with the bottom plate connected to a reference voltage. The sampled voltage is held in this capacitor throughout idle phase. An idle phase is necessary because multiphases are used in operating the differentiator. The use of multiphases is explained in the last paragraph of this section. In differentiating phase, the bottom plate switch is disconnected from the reference voltage, and the top plate of the sampling capacitor is connected to the input. The output voltage of the sampling capacitor is now the difference between the input voltage during sampling phase and the input voltage during differentiating phase. The three phases follow each other in sequence during the transmission period for a single bit. A new sampling phase starts immediately after the previous differentiating phase has concluded.

The recovered clock signal has a frequency of 13.56 MHz. If this clock was used to differentiate the envelope, sampling would only occur every two clock cycles, whereas differentiation occurs at every other cycle, which would mean that the transition might not be detected in the worst case, with a data pattern such as “0101. . .01.” Using two differentiators can solve this problem, because one can operate in sampling mode, whereas the other operates in differentiating mode, so that one channel at least always provides a correct value. Even so, the differentiated voltage may not be sufficiently large in VHBR operation with low modulation indexes, because the maximum voltage of these two channels is half the peak-to-peak amplitude of the envelope. To avoid this problem, we enhance the ability of the circuit to detect transitions by taking account of both edges of the clock signal. Sampling is done every two clock cycles as before, but differentiation occurs one and a half clock cycles after sampling, instead of just one clock cycle as before. Now, there are a total of three differentiators, and each has a dedicated comparator. The maximum amplitude of the differentiated voltage is now 50% larger than when it would be with two differentiators. We considered using four differentiators, but three are sufficient to ensure that at least one differentiator detects all the transitions, and the output voltage is 75% of the envelope peak-to-peak amplitude. Simple logic is used to detect which differentiator output has the most transitions, which are the total transitions in the ASK signal.

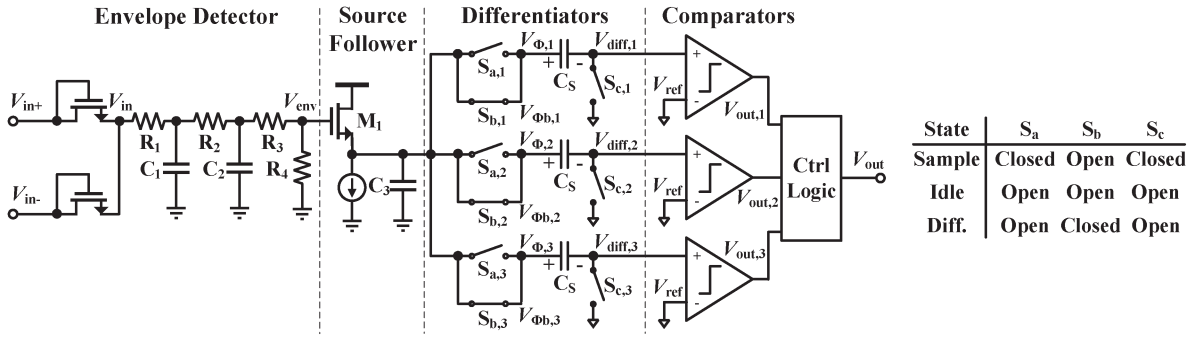

Fig. 4. Schematic of the core of the proposed differentiating ASK demodulator.

IV. Circuit Implementation

Fig. 4 is a schematic diagram of the core of our differentiating ASK demodulator, which consists of an envelope detector, the differentiators, and comparators. These blocks are implemented in different voltage domains. The input voltage level of a typical smart card ASK signal is approximately 4 to over 6 V. It is half-wave rectified by the off-chip rectifier into two signals $V_{\mathrm{in}+}$ and $V_{\mathrm{in}-}$ that have amplitudes of 2 to over 3 V and differ in phase by 180° as shown in Fig. 1. These signals are the inputs to our demodulator. The CMOS technology we used provided high-voltage transistors that operate with a supply voltage of 3.3 V, and our envelope detector is implemented with them. The remainder of the blocks, including the differentiators, comparators, logic, output drivers, and the clock extractor all operate with a supply voltage of 1.8 V. $V_{\mathrm{diff},1}$, $V_{\mathrm{diff},2}$, and $V_{\mathrm{diff},3}$ are the differentiated envelope signals of the three independent differentiators and $V_{\mathrm{out},1}$, $V_{\mathrm{out},2}$, and $V_{\mathrm{out},3}$ are the output signals of the respective comparators. V_{out} is the final demodulated output.

Fig. 5 shows the clock signals that controls the switches, and the node voltages of the core of the differentiating demodulator. For simplicity, only the first of the three differentiator and comparator pairs is considered. The input data is "0100001111" as an example. The envelope of the input signal, V_{env}, is sampled at phase $\Phi_{,1}$ and differentiated at phase $\Phi_{b,1}$. The resulting voltage $V_{\mathrm{diff},1}$ is connected to the comparator input. The arrows indicate the voltages that have been differentiated.

A. Envelope Detector

The envelope detector of the demodulator must be able to generate the envelope signal of the input by charging the capacitor when the amplitude of the carrier is large and discharging through a resistor when the carrier amplitude falls. VHBR uses a carrier of 13.56 MHz, and the bit rate of the modulated data ranges to 6.78 Mb/s at a 50% modulation rate. Since the maximum bit rate of the modulated data is close to the carrier frequency, a two-stage low-pass filter is used to reduce rippling in the envelope. A source follower has been included to buffer the output of the envelope detector.

B. Differentiator

The differentiator consists of a switched capacitor. As shown in Fig. 4, switches $S_{a,i}$ and $S_{b,i}$ connect the same nodes, and therefore could be implemented using a single switch. However, additional logic would be required to generate the timing from the multiphase clocks for toggling the switch; for simplicity,

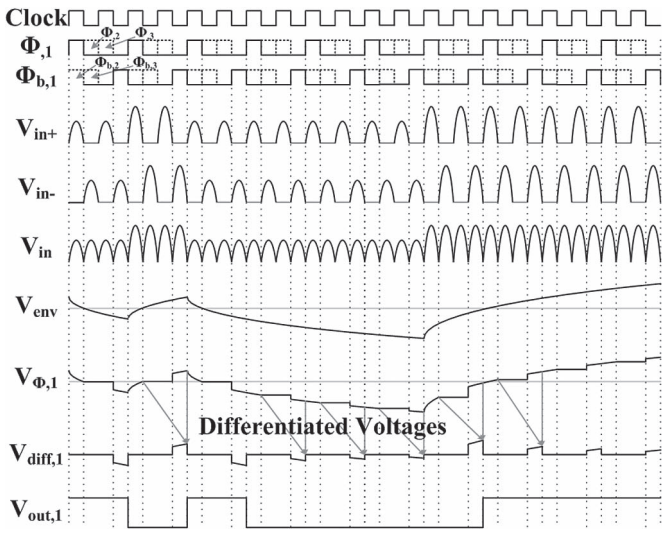

Fig. 5. Waveforms of the core of the differentiating ASK demodulator.

we used two identical switches instead. In the sampling phase, the sampling capacitor samples the source follower output with respect to the common-mode voltage of the comparator by closing switches $S_{a,i}$ and $S_{c,i}$ $(i = 1, 2, 3)$. The sampled charge Q_i $(i = 1, 2, 3)$ can be expressed by

$$Q_i = C_s(V_{\Phi,i} - V_{\mathrm{ref}}) \tag{1}$$

where $V_{\Phi,i}$ $(i = 1, 2, 3)$ is the output of the source follower during sampling phase Φ, V_{ref} is the common-mode voltage, and C_s is the capacitance of the sampling capacitor. This charge is held throughout the idle phase. During differentiating phase, $S_{a,i}$ and $S_{c,i}$ are opened and $S_{b,i}$ is closed $(i = 1, 2, 3)$, and the charge on the sampling capacitor can now be determined as

$$Q_i = C_s(V_{\Phi b,i} - V_{\mathrm{diff},i}) \tag{2}$$

where $V_{\Phi b,i}$ $(i = 1, 2, 3)$ is the output of the source follower during differentiating phase Φ_b, and $V_{\mathrm{diff},i}$ $(i = 1, 2, 3)$ is the output voltage of the differentiator. Since the charge is conserved, Q_i is unchanged, and therefore, the output voltage of the differentiator $V_{\mathrm{diff},i}$ can be expressed as

$$V_{\mathrm{diff},i} = V_{\Phi b,i} - V_{\Phi,i} + V_{\mathrm{ref}}. \tag{3}$$

We consider $V_{\mathrm{diff},i}$ to be the differentiated value of the output of the source follower, which tracks the envelope of the ASK signal. This differentiated output is related to the common-mode voltage by the comparator.

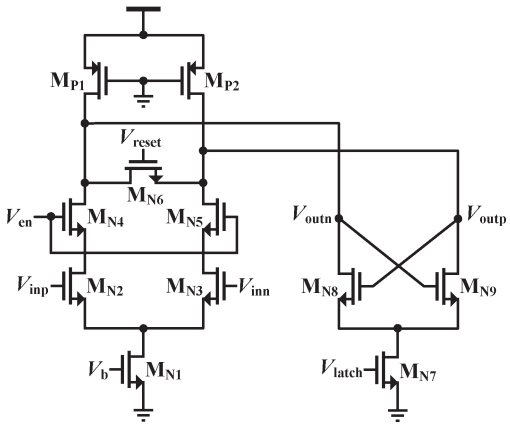

Fig. 6. Schematic of the dynamic latch comparator.

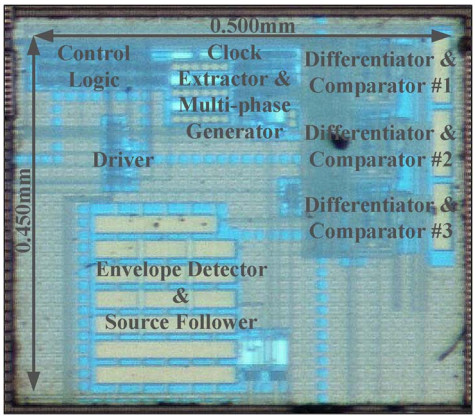

Fig. 7. Die photograph of the proposed ASK demodulator.

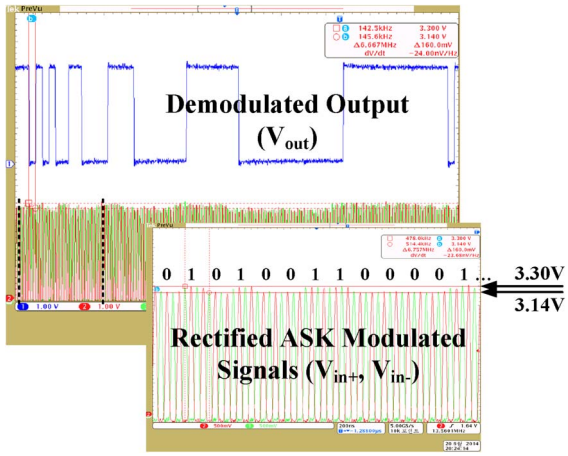

Fig. 8. Measured waveforms of the input and output signals of our differentiating demodulator.

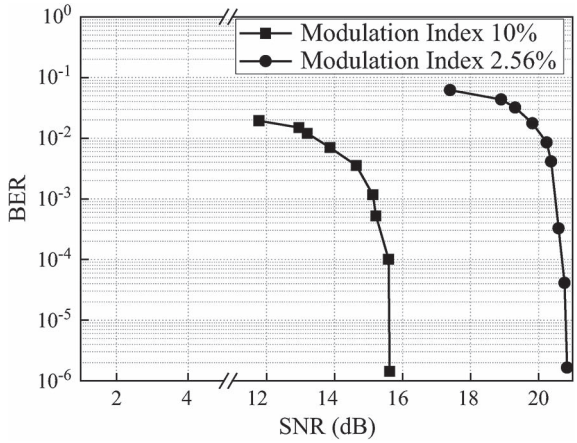

Fig. 9. Measured BER versus SNR plot of our differentiating demodulator.

C. Comparator

Fig. 6 is a schematic diagram of our comparator, which consumes more power than any other block in the core of the demodulator, and it is therefore critical to reduce its power consumption as far as possible if it is to be suitable for the strict power consumption regime of a contactless smart card. Our comparator has a dynamic latch structure, which offers fast operation, as well as low power consumption.

The dynamic latch of the comparator operates in two modes: reset and regeneration. When in reset mode, transistors M_{N4}, M_{N5}, and M_{N7} are all switched off by lowering $V_{\rm en}$ and $V_{\rm latch}$ to reduce power, and M_{N6} is turned on by reset signal $V_{\rm reset}$ to equalize the voltage at the output nodes to avoid memory effect. In regeneration mode, the difference between $V_{\rm inp}$ and $V_{\rm inn}$, the voltage at gates of M_{N2} and M_{N3}, causes in a difference in the voltage between the output nodes $V_{\rm outp}$ and $V_{\rm outn}$, and the latch will operate rapidly due to the positive feedback loop created through transistors M_{N8} and M_{N9}.

V. Experimental Results

Fig. 7 is a microphotograph of the die for the proposed ASK demodulator, which is implemented in a 0.18 μm CMOS technology, with an active area of 0.08 mm^2. The half-wave rectifier in Fig. 1 is assumed to be off-chip, and in our tests, we applied two synchronized signals representing the two half-wave rectified ASK modulated signals as the input. In order to test the operation of our demodulator with a wide range of modulation parameters and amplitude levels, signal generators were adopted. The carrier frequency of the modulated input is 13.56 MHz, and the data bit rate is 6.78 Mb/s for VHBR. The amplitude of the half-wave rectified signals is 3.3 V. The modulation index specified in ISO/IEC 14443 Type B is 10%, but we were able to run the demodulator at an index of 2.56%, which demonstrates its capability. Fig. 8 shows the measured waveforms of the input ASK modulated signals and that of the demodulated output. The input signals contain binary strings of 1, 1, 2, 4, 8, and 16 repeated zeroes or ones. Irrespective of string length, the correct demodulated signal is obtained. The measured power consumption of the chip from the 3.3-V high supply voltage, the 1.8-V analog, and digital supply voltages are, respectively, 36.05, 108.4, and 204.3 μW, for a total of 348.75 μW.

Bit error rate (BER) of the differentiating demodulator was measured using a 2^7-1 pseudorandom binary sequence data pattern. For reliable communication the BER should be less than 10^{-4} [6], [9]. No errors were observed in a data length of over 16 million bits, resulting in a BER of under 10^{-7} at a data rate of 6.78 Mb/s with a modulation index of 2.56%. Fig. 9 shows the obtained BER versus signal-to-noise ratio (SNR) plot for both modulation indexes of 2.56% and 10%. Measurements show an SNR of approximately 15.6 dB for a BER of 10^{-4}, and this satisfies the design specification of our application.

TABLE I
SPECIFICATIONS AND COMPARISON WITH PRIOR ASK DEMODULATORS

Reference	Year	Process (μm)	Data-rate (Mbps)	Carrier frequency (MHz)	Area (μm^2)	Power (μW)	Modulation index (%)	FoM[1] [10]	FoM[2] [11]	FoM[3] [12]	FoM[4] [13]	FoM[5] (this work)
[7]	2007	0.35	2	10	N/A	84	N/A	420	N/A	**42**	N/A	N/A
[2]	2008	0.18	1	2	468.35	336	5.26	672	95.06	336	**6.355**	17.67
[11]	2008	0.35	0.25	2	3025	1010	27	8080	4.63	4040	0.082	1090.8
[13]	2010	0.35	1.2	13.56	3300	306	N/A	3457.8	N/A	255	1.188	N/A
[10]	2011	0.18	1	2	105389	62	7.55	**124**	66.23	62	0.153	4.68
[12]	2012	0.35	1.356	13.56	3554.2	274	70	2740	1.43	202.06	1.392	141.45
[14]	2013	0.13	2	10	16800	105	N/A	525	N/A	52	1.134	N/A
This Work	2014	0.18	6.78	13.56	80000	348.75	2.56	697.5	**195.31**	51.44	0.243	**1.32**

1) FoM = Power(μW) × Carrier frequency(MHz) / Data-rate(Mbps)
2) FoM = Data-rate(kbps) / (Carrier frequency(MHz) × Modulation index(%))
3) FoM = Power / Data-rate(pJ/bit)
4) FoM = Data-rate(kbps) / (Power(mW) × Core area(μm^2))
5) FoM = (Power / Data-rate)(pJ/bit) × Modulation index

Table I compares the characteristics of this circuit with prior ASK demodulators, using various figures of merit (FoM). The best value of each FoM is highlighted in bold text. Prior FoM includes the product of power consumption and carrier frequency divided by the data rate, but neglects the modulation index [10]. An alternative formula is the data rate divided by both the carrier frequency and the modulation index; but this ignores power consumption [11]. However, another figure is obtained by dividing power consumption by the data bit rate; this disregards both the modulation index and the carrier frequency [12]. Reference [13] includes both the gate count and core area in the FoM, but due to the lack of information on gate count in other works, the gate count is omitted in our Table I. We define a new figure of merit that endeavors to include all relevant characteristics described by

$$\text{FoM} = \frac{\text{power}}{\text{data-rate}} \times \text{modulation index}. \tag{4}$$

Our demodulator can achieve a much higher data rate while coping with a much lower modulation index than other recent designs, and its power consumption is comparable with theirs.

VI. CONCLUSION

We have proposed a ASK demodulator that is compliant with the ISO/IEC 14443 Type B standard VHBR amendment for smart card applications. The use of switched-capacitor differentiators allows lower modulation indexes and higher data rates. The prototype has been implemented in 0.18 μm CMOS technology with a power supply of 1.8 V, except the envelope detector, which is supplied with 3.3 V. The power consumption is under 350 μW. Measured results confirm correct demodulation of ASK input signals even after long strings of ones or zeroes. The BER was measured to be below 10^{-7}. Our demodulator can operate at a modulation index of 2.56%, which is well below the 10% required by the standard. This suggests that it has potential for applications at higher bit rates and lower modulation indexes than current systems.

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