4-Slot, 8-Drop Impedance-Matched Bidirectional Multidrop DQ Bus With a 4.8-Gb/s Memory Controller Transceiver

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***Abstract*— In this paper, we introduce an impedance-matched bidirectional multidrop (IMBM) DQ bus, together with a 4.8-Gb/s transceiver for a memory controller that supports this bus. Reflective ISI is eliminated at each stub of the IMBM DQ bus by resistive unidirectional impedance matching. A prototype memory controller transceiver is designed and fabricated in a 0.13-μm CMOS process and operates with a 1.2-V supply voltage. Its effectiveness is shown on various multidrop channel configurations. At 4.8 Gb/s, this transceiver with a 4-slot, 8-drop IMBM DQ bus has an eye opening of 0.39 UI in TX mode and 0.58 UI in RX mode, at a threshold of 10^{-9} BER, whereas a comparable transceiver with a conventional 4-slot, 8-drop stub series terminated logic has no timing margin under the same test conditions. Our transceiver consumes 14.25 mW/Gb/s per DQ in TX mode, and 13.69 mW/Gb/s per DQ in RX mode.**

***Index Terms*— High-speed interface, impedance matching, memory controller, memory interface, memory transceiver, multidrop DQ bus, stubseries terminated logic.**

I. Introduction

THE MAIN memory of PCs and servers consists of dynamic random access memory (DRAM). Memory and processor traditionally communicate over a multidrop bus such as stub series terminated logic (SSTL) bus topology. Signal frequencies on such buses have gradually gone up in order to keep up with the growing speeds of integrated circuit. However, as the data-rates on these buses have increased, the maximum number of slots per channel has been reduced to preserve signal integrity. The key issue is that of inter-symbol interference (ISI), which is caused by signal reflections resulting from impedance mismatches at multidrop junctions and terminations. Reducing the number of slots per channel limits the memory handling capacity per channel and therefore high-capacity channels such as DDR2/3 memory buses [1] still use the SSTL bus topology, in spite of the reflections. The next generation of memory buses is likely to incorporate point-to-point bus topology [2], because a multidrop bus topology is hard to handle over 2 Gb/s [3]. However, point-to-point channels require too much printed circuit board (PCB) area to allow their use in high-capacity memory systems such as DRAM modules for personal computers and servers. This makes it necessary to find an alternative way of increasing the data transfer rate while maintaining the multidrop bus topology, and thus ISI caused by reflection is the key consideration. We expect a three- or four-connector module memory with six or eight ranks, at least, will be needed in next-generation multicore PCs, server, and workstation architectures. This implies that new approach is necessary to support both high-speed data rate and high memory capacity.

To fulfill demands on memory capacity per channel as well as high data-rate, daisy-chained point-to-point bus topologies such as fully buffered DIMM (FBDIMM) with an advanced memory buffer [4], [5] and a cascading memory architecture [6], [7] have been taken. However, these buses have an undesirably long latency. In some applications, reducing latency to achieve fast access to main memory of a PC or server has priority over the data throughput, because the CPU is idle until the first data arrives. An alternative way to make a significant reduction in channel reflection is impedance matching by means of a $2Z_0\Omega$ transmission line in the last part of the memory module [8], but this sort of matching can only be applied to a two-slot configuration. Configuring the PCB, so that the transmission lines are widely separated, can reduce reflections dramatically [9], but this scheme is also limited to two or three slots. Impedance-matching schemes [10], in which the characteristic impedances of the PCB traces are tuned, involve the use of wider PCB traces, making it difficult to route a wide parallel memory interface. In another approach, a decision feedback equalizer (DFE) is used to cancel the reflective ISI [11]. But many taps are required for the DFE, and it has a limitation of operation frequency.

In this paper, we introduce a new type of a multidrop bus, called an impedance-matched bidirectional multidrop (IMBM) DQ bus, for a main memory channel, together with a memory controller transceiver which is optimized for this bus. Because the IMBM DQ bus attenuates the amplitude of signals in inverse proportion to the number of modules, a new clocking

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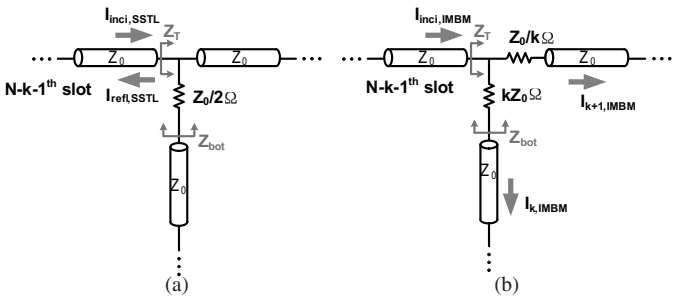

Fig. 1. Simplified stub model of (a) conventional SSTL DQ bus and (b) proposed IMBM DQ bus.

architecture is necessary to support the IMBM DQ bus. This combination can achieve data-transfer rates in the order of Gb/s without reflective ISI, while retaining the low latency of a multidrop bus.

The remainder of this paper is organized as follows. In Section II, we present the principles and design of the IMBM DQ bus. In Section III, we introduce our memory controller transceiver architecture and its circuit realization. In Section IV, we describe our measurement setup and provide experimental results from our prototype. Finally, we conclude this paper in Section V.

II. Impedance-Matched Bidirectional Multidrop DQ Bus

When a transmission line has an impedance discontinuity, a reflection wave occurs. In the case of a conventional SSTL DQ bus, a series resistor of $Z_0/2\Omega$ reduces the ringing and reflection, as shown in Fig. 1(a). But, this bus cannot suppress reflections entirely when there are more than two slots, because the reflection coefficient of an SSTL DQ bus has a nonzero value, which can be expressed as follows:

$$\Gamma_{\mathrm{SSTL}} = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{\left(Z_0 \| \left(Z_0 + \frac{Z_0}{2}\right)\right) - Z_0}{\left(Z_0 \| \left(Z_0 + \frac{Z_0}{2}\right)\right) + Z_0} = -\frac{1}{4}. \quad (1)$$

Thus a reflected signal $I_{\mathrm{refl,SSTL}}$ is generated at every stub, and these signals propagate across connectors repeatedly and cause overshooting or over damped responses, depending on the position of the module. As the data-rate increases, these reflection waves play a key part in generating ISI in an SSTL DQ bus.

Fig. 1(b) shows part of our IMBM DQ bus [12]. At the cost of the insertion of two resistors of appropriate values at each stub, the impedances are matched at the stubs without attempting to alter the characteristic impedances of the PCB traces. The use of emerging technologies such as embedded PCB resistors or film resistors may allow the extra resistors fit within a PCB trace and relax the PCB area overhead of ours. The reflection coefficient at each stub of an impedance-matched DQ bus can be expressed as follows:

$$\Gamma_{\mathrm{IMBM}} = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{\left(\left(Z_0 + \frac{Z_0}{k}\right) \| (Z_0 + kZ_0)\right) - Z_0}{\left(\left(Z_0 + \frac{Z_0}{k}\right) \| (Z_0 + kZ_0)\right) + Z_0} = 0. \quad (2)$$

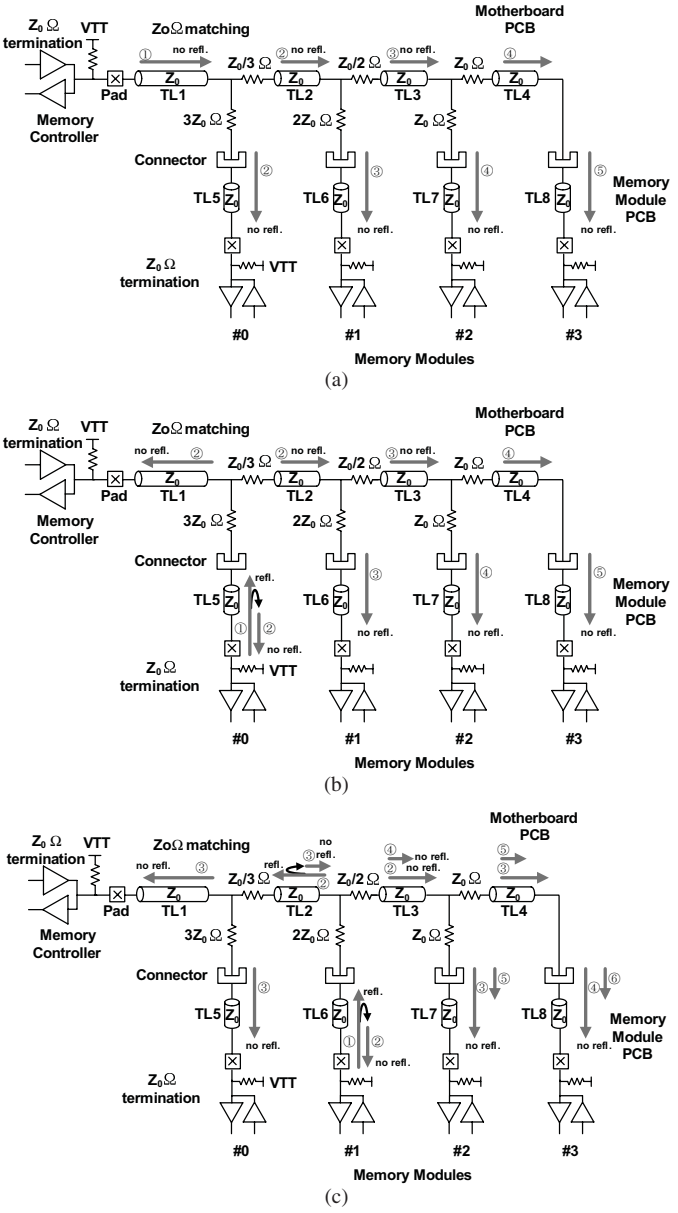

Fig. 2. Impedance-matched bidirectional multidrop (IMBM) DQ bus. (a) Write operation. (b) Read operation from module #0. (c) Read operation from module #1.

Thus we see that, at least in theory, an IMBM DQ bus does not generate a reflected signal at each stub. The ratio between $I_{\mathrm{k+1,IMBM}}$ and $I_{\mathrm{k,IMBM}}$ can be expressed as follows:

$$I_{\mathrm{k+1,IMBM}} : I_{\mathrm{k,IMBM}} = (Z_0 + kZ_0) : \left(Z_0 + \frac{Z_0}{k}\right) = k : 1. \quad (3)$$

This means that an IMBM DQ bus transmits an incident signal to every module with the same current, and allows an identical transfer response, regardless of the position of a module.

Fig. 2(a) shows an IMBM DQ bus. Resistors of Z_0, $Z_0/2$, $Z_0/3$, $2Z_0$, and $3Z_0\Omega$ match impedances in the left-to-right direction along the upper four transmission lines (TLs). Thus each memory module receives the same voltage from the memory controller, and the memory controller receives

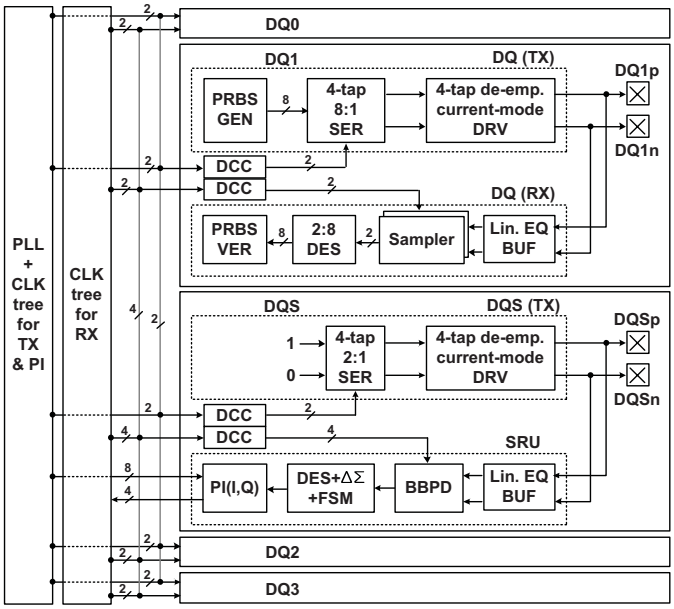

Fig. 3. Memory controller transceiver block diagram and its clocking architecture.

the same voltage from each memory module. To prevent reflections at the ends of the channel, the memory controller and the memory modules both have on-die-termination (ODT) resistors. Because the reflection coefficient from bottom sides of the stub is nonzero, as shown in (4), all modules in the IMBM DQ bus must turn on the termination resistors

$$\begin{aligned}\Gamma_{\text{IMBM,bot}} &= \frac{Z_{\text{bot}} - Z_0}{Z_{\text{bot}} + Z_0} \\ &= \frac{\left(kZ_0 + \left(Z_0 \| \left(\frac{Z_0}{k} + Z_0\right)\right)\right) - Z_0}{\left(kZ_0 + \left(Z_0 \| \left(\frac{Z_0}{k} + Z_0\right)\right)\right) + Z_0} \\ &= \left(\frac{k}{k+1}\right)^2. \end{aligned} \tag{4}$$

Although impedances are only matched in one direction, the IMBM DQ bus can cancel reflective ISI during the transmission of both write and read data. Because there is no reflection at the right-hand ends of the TLs (TL1, TL2, TL3, and TL4) on the motherboard during a write operation, as shown in Fig. 2(a), the data-stream being written from the memory controller to memory modules #0, #1, #2, and #3 is transmitted without reflections ignoring reflections due to parasitics. In write operation, maximum turn-around time ($T_{\text{turn\_around}}$) occurs when the write signal is sent from the controller to memory module #3. This time can be expressed as (5). T_d is the flight time of the signal passing through each TL

$$\begin{aligned}T_{\text{turn\_around,WR,\#3}} = {} & T_{d,TL1} + T_{d,TL2} \\ & + T_{d,TL3} + T_{d,TL4} + T_{d,TL5}. \end{aligned} \tag{5}$$

Since reflection does not occur in write operation, additional waiting time for the settling of reflections is unnecessary. Reading is performed in a different manner. A read operation from memory module #0 to the memory controller causes a reflection at the top end of TL5, as shown in Fig. 2(b), but this signal is absorbed by the ODT resistor of module #0. The read data are split at the stub, and the desired data signal flows from the right-hand end of TL1 to its left-hand end and eventually reaching the memory controller. Meanwhile, unwanted signals flow from left to right through TL2 and proceed towards memory modules #1, #2, and #3, causing no reflections, and are eventually absorbed by the ODT resistors. Thus, even though reflections do occur in an IMBM DQ bus during read operations, no reflective ISI arrives at the controller ignoring reflections due to parasitics. If data flow from memory module #1 to the memory controller during a read operation, as shown in Fig. 2(c), then a reflection occurs at the top of TL6; but this signal is absorbed by the ODT resistor as before. Again, the read data are split at the stub, and the desired data flow from right to left through TL2, where there is another reflection. This reflected signal goes rightward through TL2, where it too is absorbed by the ODT resistors. Thus the desired read signal arrives at the memory controller, while all the reflections are absorbed by the ODT resistors. Read operations from memory modules #2 and #3 behave similarly, and again there is no reflective ISI. In read operation, maximum turn-around time occurs when the read signal is sent from the memory module #3 to the controller. In this case, the controller should wait until the reflection signal at the left-side of TL2 disappears in the bus. This turn-around time can be expressed as (6). $T_{\text{d,CMD}}$ is the flight time of the command signals from the controller to the memory modules

$$\begin{aligned}T_{\text{turn\_around,RD,\#3}} = {} & T_{d,CMD} + (T_{d,TL8} + T_{d,TL4} \\ & + T_{d,TL3} + T_{d,TL2}) + T_{d,TL1}. \\ & + \max\{T_{d,TL1}, (T_{d,TL2} \\ & + T_{d,TL3} + T_{d,TL4} + T_{d,TL8})\}. \end{aligned} \tag{6}$$

In summary, the IMBM DQ bus generates no reflections during write operations, and the reflections that are generated during read operations do not reach the memory controller. Therefore, the IMBM DQ bus transmits and receives both read and write signals without reflective ISI. In addition, the IMBM DQ bus is tolerant to stub length variation. Since impedance is matched in the right-ward direction, additional time for the settling of reflections is not required with the exception of residual reflections due to parasitics. In the case of the SSTL DQ bus, stub resistors suppress reflections instead of fully eliminating them. Thus the signal behavior of the SSTL DQ bus depends on stub length. Both the SSTL DQ bus and the IMBM DQ bus are affected by characteristic impedance and series resistor value mismatch.

III. Memory Controller Transceiver

A. Memory Controller Transceiver Architecture

Fig. 3 shows the architecture of a memory controller transceiver designed to support the IMBM DQ bus. This transceiver includes four data (DQ) channels, a data strobe (DQS) channel, a PLL, and a clock tree. Each bidirectional DQ channel consists of a transmitter (TX) and a receiver (RX). The TX is made up of a PRBS generator for BER testing,

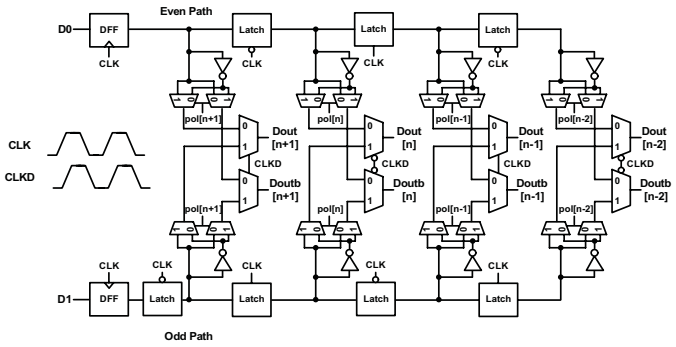

Fig. 4. Four-tap half-rate serializer with differential output.

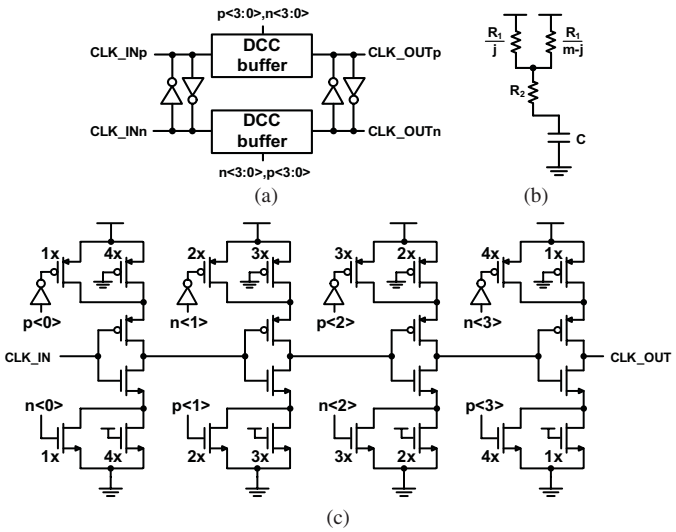

Fig. 5. (a) Overall DCC structure. (b) Simple equivalent model of the jth stage of the DCC buffer. (c) Schematic diagram of the DCC buffer.

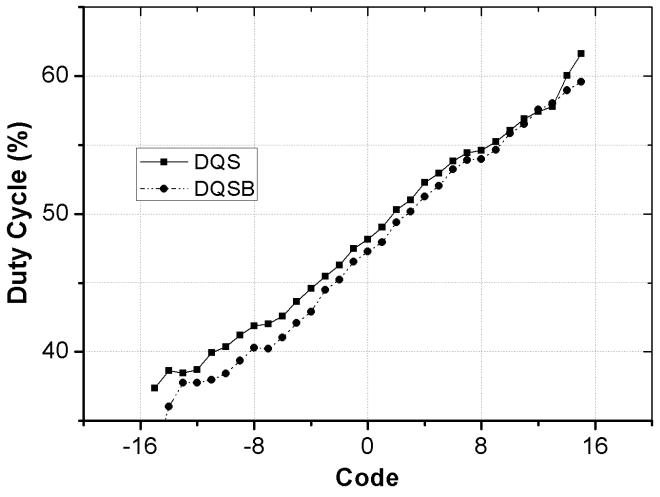

Fig. 6. Measured DCC linearity of a 2.4-GHz DQS signal.

a four-tap 8:1 serializer, and a current-mode driver to allow de-emphasis with four taps. The RX consists of a linear equalizing buffer [13], a sampler, a 2:8 deserializer, and a PRBS verifier. The PLL and clock trees provide a TX clock for the serializer and a multiphase clock for the strobe recovery

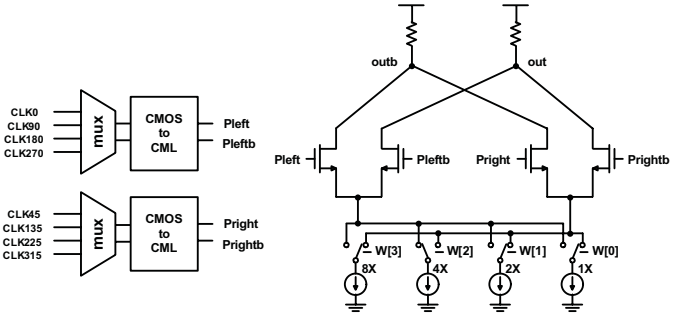

Fig. 7. Schematic diagram of the phase interpolator.

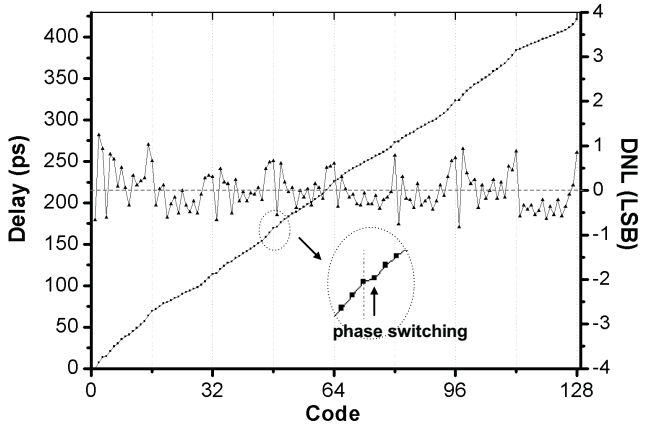

Fig. 8. Measured linearity of the phase interpolator.

unit (SRU) of the DQS block. The DQS channel generates a strobe signal with the same phase as the DQ write data. This strobe signal is used for timing recovery in the RX of a memory module. The IMBM DQ bus attenuates the voltage of signals in inverse proportion to the number of modules. Therefore, direct sampling of data using the received strobe are inadvisable.

Fig. 3 also shows the SRU and RX clocking architecture in detail. The SRU has a dual loop architecture for timing recovery [14]. In order to generate a sampling clock with the proper phase for every DQ, a phase interpolator and a half-rate bang-bang phase detector (PD) are used in the SRU. The central PLL generates multiphase clock signals, which are delivered by the clock tree to drive the phase interpolators. The SRU loop control block, which is composed of a deserializer, a first-order delta-sigma ($\Delta\Sigma$) modulator, and a finite-state machine, receives early and late information from the PD and then supplies the appropriate up or down control bit to the phase interpolator. The $\Delta\Sigma$ modulator dithers this control bit to prevent the entire strobe recovery loop from causing limit-cycle. Our memory controller transceiver does not have to track the frequency offset; this avoids the need for integrating control of the strobe recovery loop, and thus prevents the $\Delta\Sigma$ modulator from causing a stability problem. A duty-cycle corrector (DCC) is also used to adjust the sampling clock, which eliminates the distortion of the duty-cycle that would otherwise be caused by the clock tree and phase interpolator.

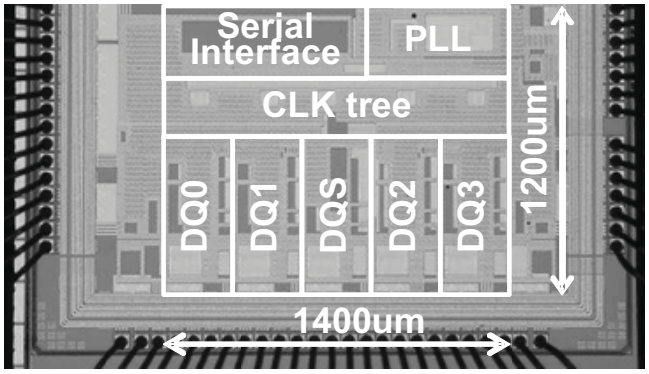

Fig. 9. Die photo of the memory controller transceiver implemented in 0.13-μm CMOS.

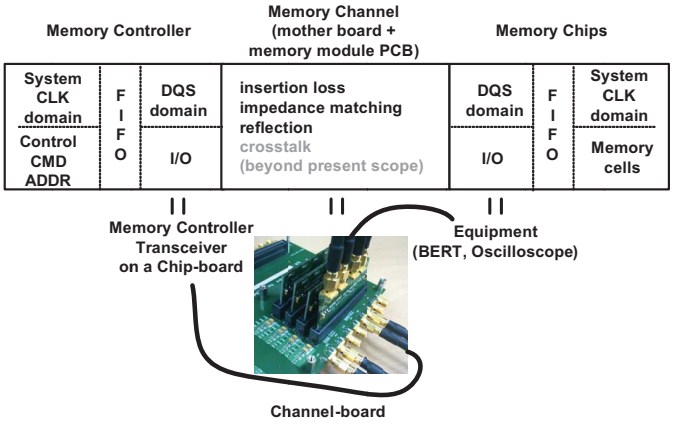

Fig. 10. Scope of this work.

All the DQ channels must receive the recovered sampling clock with the same phase, and so we use the shorting clock method [15] to reduce the on-chip clock skew. To eliminate skew between each DQ channel and the SRU, the sampling clock signal used in the PD traverses the clock tree in parallel with the recovered clock. This increases the loop latency of the entire SRU and the limit-cycle; however, the first-order $\Delta\Sigma$ modulator in this loop can cope with this extended latency, which thus has negligible effect on the jitter of the recovered clock signal.

B. Four-Tap Half-Rate Serializer and Driver

To compensate for the nonideal nature of the channels, the memory controller transceiver uses a linear equalizer in RX mode and performs de-emphasis in TX mode. To achieve the latter, as shown in Fig. 4, our serializer has a four-tap output and its driver has a separate component for each tap. Instead of using an XOR gate [16], we employ two intermediate multiplexers, which select their polarity while generating a negative output signal. The differential output signal is driven by the final multiplexers, which are in turn driven by the delayed clock signal CLKD, because cascaded multiplexers need a timing margin to operate at high speed. The four-tap serialized signal is then delivered to the four-tap current-mode driver. Equalization coefficients are controlled by means of the control signal tap weight.

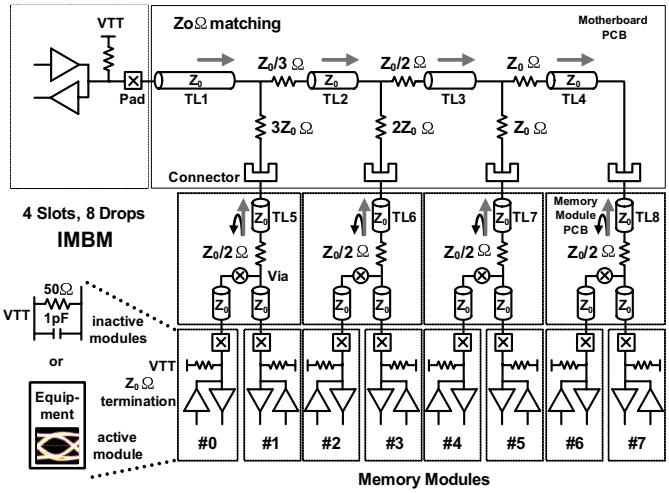

Fig. 11. Implemented 4-slot 8-drop IMBM DQ bus.

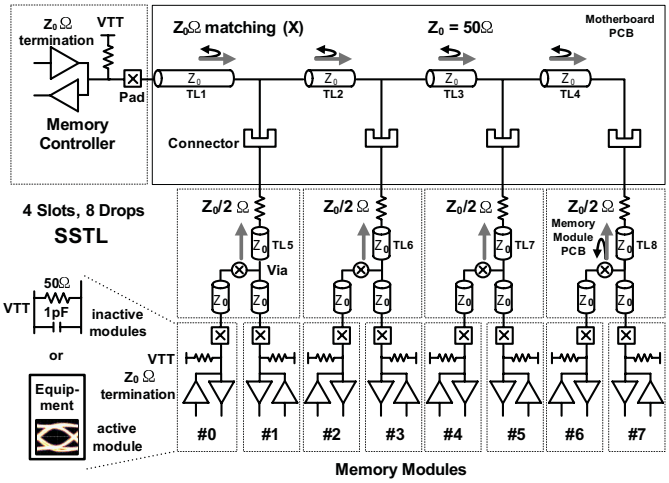

Fig. 12. Implemented 4-slot 8-drop SSTL DQ bus.

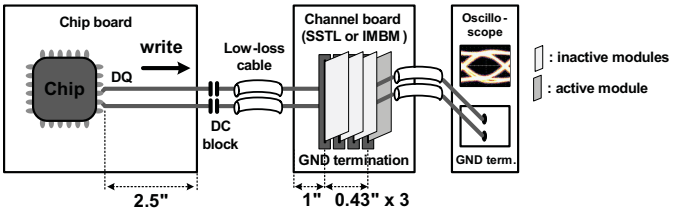

Fig. 13. Setup I for measuring the eye diagram and single-bit response.

C. DCC

Fig. 5 shows our DCC. To reduce its area and complexity, the controlled and uncontrolled transistors in the DCC buffer are separated as shown in Fig. 5(c). An equivalent circuit model of the jth stage of an $(m-1)$-stage DCC buffer is given in Fig. 5(b). The resolution of the DCC in the jth stage can then be expressed as follows:

$$\left(\frac{R_1}{m-j}+R_2\right)C-\left(\left(\frac{R_1}{j}\|\frac{R_1}{m-j}\right)+R_2\right)C = \frac{j}{m(m-j)}R_1C. \quad (7)$$

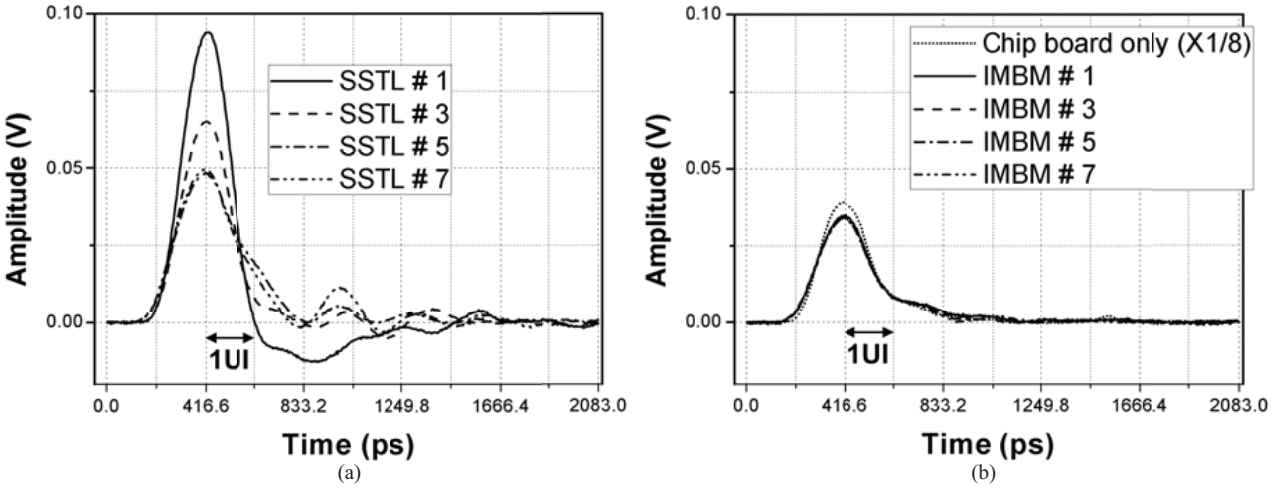

Fig. 14. Measured 4.8-Gb/s single-bit responses of (a) SSTL and (b) IMBM DQ bus.

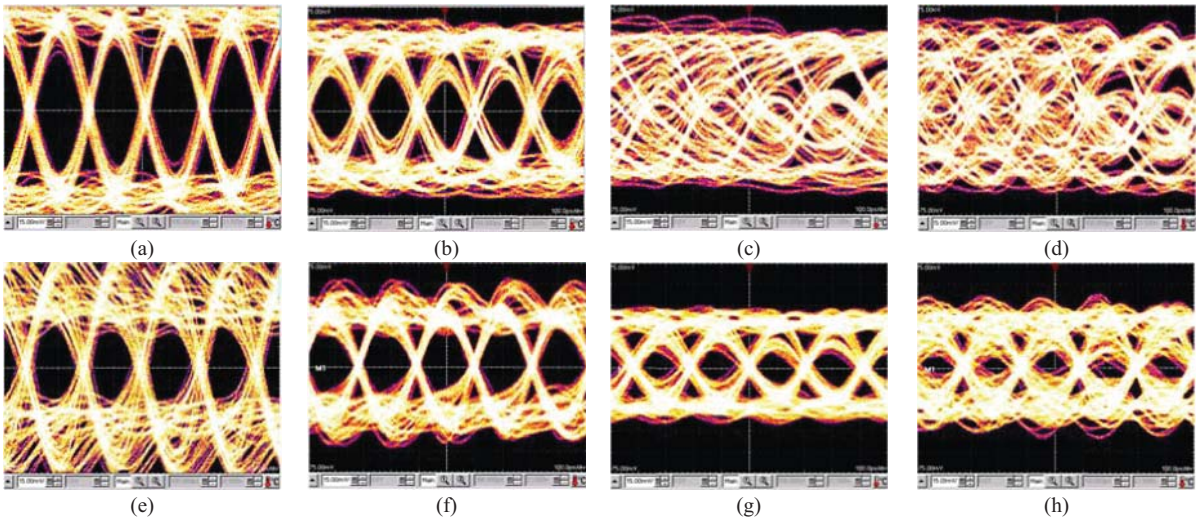

Fig. 15. Measured 4.8-Gb/s eye diagrams of an unequalized signal (a) #1, (b) #3, (c) #5, and (d) #7; a de-emphasized signal (e) #1, (f) #3, (g) #5, and (h) #7 at SSTL module.

In our design m is 5, and thus the resolutions of consecutive stages are 1/20, 2/15, 3/10, and 4/5. Because the ratios between successive resolutions are close to 2, the DCC buffer can achieve linearity despite its simple design and small area. Fig. 6 shows the measured DCC linearity curve for 2.4 GHz DQS and DQSB output signals. The DCC can cover from -42% to 38% of the duty cycle.

D. Phase Interpolator

There are two possible types of phase interpolator. In one type, the phase interpolator core and multiplexer are separated, while another type has an embedded multiplexer [17]. In this latter type, all the multiphases are simultaneously connected to the input pair of the phase interpolator. This reduces the effect of clock feed through on linearity, but it also increases the load on the output capacitance, which in turn limits the speed of this type of phase interpolator when there are more than eight phases coming from the PLL. In our SRU, we therefore use the phase interpolator shown in Fig. 7, which has a separate multiplexer for each of the eight phases, thus improving linearity. Clock feedthrough is normally considered to be the main source of nonlinearity, but actually it enhances the linearity of this design of phase interpolator, because it creates a mid-phase during multiphase switching. Fig. 8 shows the linearity curve of the phase interpolator as well as its DNL. We can see that the mid-phase occurs during phase switching, and the absolute value of the DNL does not exceed 1.

IV. Experimental Results

A prototype memory controller transceiver was designed and fabricated using a 0.13-μm CMOS process, and Fig. 9 is a microphotograph of the die. The transceiver, composed of four DQs and a DQS, occupies 1400 $\times$ 1200 μm. We implemented the transceiver chip as the I/O circuitry of a memory controller, and also constructed a test board, with a motherboard and memory module PCBs, as shown in Fig. 10. There are no actual memory chips in this setup: test equipment including a BERT and an oscilloscope plays their role. To

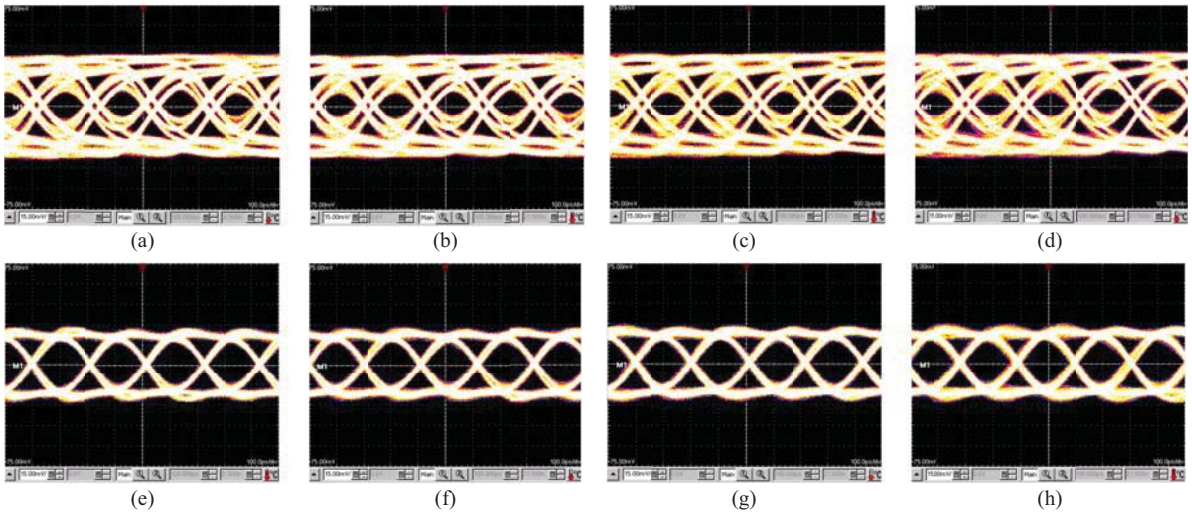

Fig. 16. Measured 4.8-Gb/s eye diagrams of an unequalized signal (a) #1, (b) #3, (c) #5, and (d) #7; a de-emphasized signal (e) #1, (f) #3, (g) #5, and (h) #7 at IMBM module.

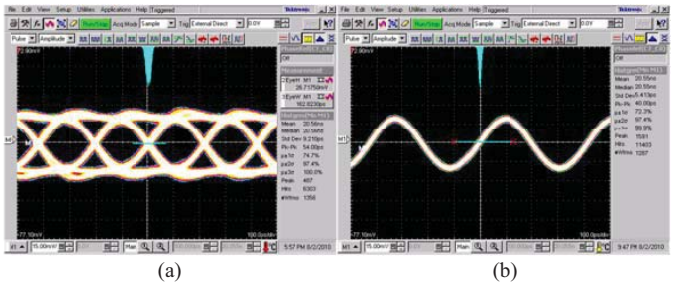

Fig. 17. Measured 4.8-Gb/s eye diagram and histogram of a de-emphasized (a) DQ signal and (b) DQS signal, both on the IMBM DQ bus.

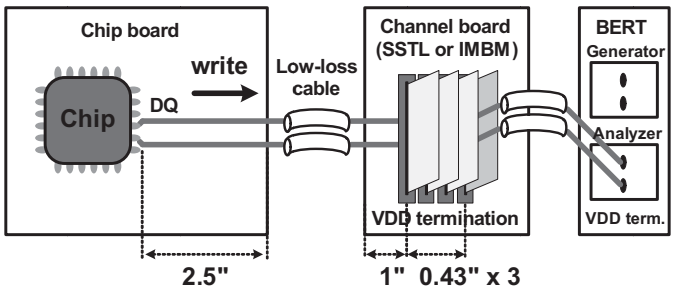

Fig. 18. Setup II for measuring the TX BER.

mimic the heavy load imposed by memory chips, inactive modules are modeled by passive 50 Ω resistors in parallel with 1-pF capacitors; whereas 50 Ω resistors alone were used in our previous experiments [12].

To facilitate a range of measurements, we implemented the chip- and channel-boards separately, using Nelco instead of FR4 to reduce insertion losses. MicroTCA [18] connectors are used on the channel board, since DDR2/3 connectors are not suitable for multigiga bit per second transmissions. The chip board has a 2.5-in trace and the channel board has a trace with a length between 1.43 and 2.29 in. The spacing of the connectors is 0.43 in. A block diagram and photograph of the actual 4-slot 8-drop double-sided IMBM DQ bus that we implemented is shown in Fig. 11.

To eliminate the reflections which occur in front of the vias (the through-hole paths to the other surface) in a memory module, $Z_0/2\Omega$ resistors are inserted. To compare the channel characteristic of the IMBM DQ bus with that of a conventional SSTL DQ bus, we implemented the latter with similar specifications, as shown in Fig. 12. For fairness, we assumed that every memory module in the conventional SSTL DQ bus has an ODT resistor.

A. Single-Bit Response and Eye Diagram

The single-bit response and eye diagram were both measured using an oscilloscope. Because the memory controller transceiver uses a CML-level signal during transmission, and an oscilloscope only provides ground termination, DC block and ground-terminated channel boards were used, as shown in Fig. 13.

Fig. 14(a) shows the 4.8-Gb/s single-bit response of a conventional SSTL DQ bus. Because of the reflections between connectors, this single-bit response varies greatly between module positions. The signal SSTL#1 through the first module has an overshooting response, and its second and third postcursors have large negative values. Conversely, signals SSTL #5 and #7 have over-damped responses, as though they were being transmitted through a very lossy channel. The first postcursor level is almost half the magnitude of the main cursor. Conversely, the single-bit response of the IMBM DQ bus is identical for all module positions, as shown in Fig. 14(b). The IMBM DQ bus attenuates the amplitude of signals by 1/8 times. The 1/8-scaled single-bit response of a signal passing through the chip board alone is very similar to that of the signals that go through the IMBM DQ bus, suggesting that there is little reflection generated in the IMBM DQ bus.

To check the timing and voltage margins, we obtained eye diagrams for both SSTL and IMBM DQ buses. The memory controller transceiver and chip board alone have considerable postcursor voltage levels, mainly caused by the capacitance of the package and pad. As a result, we used

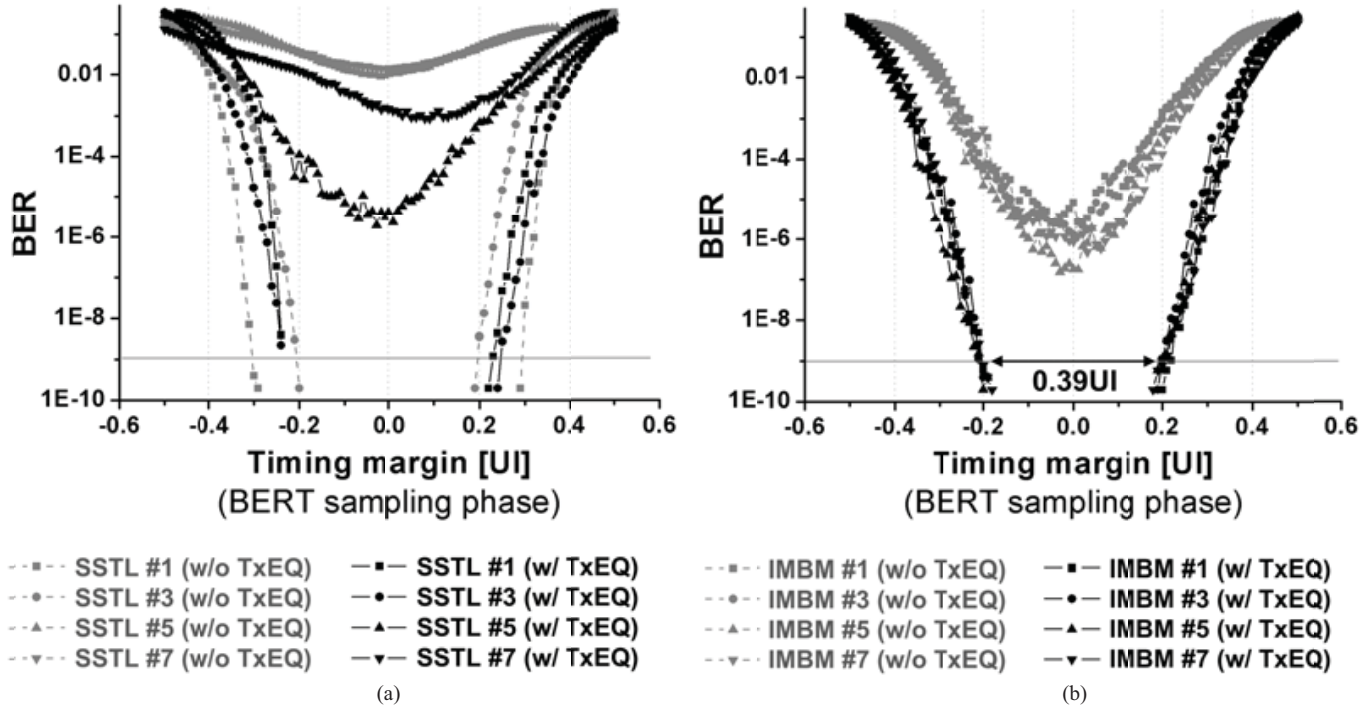

Fig. 19. Bathtub graph based on TX BER measurements of (a) SSTL and (b) IMBM signals.

TX de-emphasis to measure both unequalized and equalized signals. Equalization coefficients were chosen to cancel the ISI, which is not related to the reflections from each stub, but to the insertion loss of the PCB trace on the chip board, and the capacitive loading imposed by both the memory controller transceiver chip and the 1 pF loading capacitors. The coefficient of the precursor tap was set to 0, the main cursor tap was set to 1, the first postcursor tap was set to -0.33, and the second postcursor tap was set to -0.08. Fig. 15(a)–(d) show the measured eye diagrams of the SSTL DQ bus for a 4.8-Gb/s 2^7-1 PRBS data pattern. As might be predicted from the single-bit response of both the SSTL and IMBM DQ buses, modules #5 and #7 of the SSTL DQ bus have severely closed eye diagrams, whereas modules #1 and #3 have clean diagrams. With TX de-emphasis, modules #1 and #3 show over-boosted behavior because module #1 has negative postcursors and #3 has small postcursors. The eyes for modules #5 and #7 are enlarged, but the timing and voltage margins of the equalized signal are, respectively, only half the 1UI timing and signal levels, as shown in Fig. 15(e)–(h). Fig. 16 shows eye diagrams of write signals transmitted through the IMBM DQ bus. These diagrams are identical for all modules, allowing the memory controller transceiver to have the same TX equalization coefficients for all modules. With TX equalization, the IMBM DQ bus has a wide-open eye diagram and the voltage and timing margins are much greater than those of the SSTL DQ bus.

Fig. 17 shows the 4.8-Gb/s eye diagram and histogram of the de-emphasized DQ and DQS signals in the IMBM DQ bus. The DQS signal toggles every cycle and has less timing jitter than the DQ signal, which is random data. The measured jitter in the DQ signal is 9.21 ps_{rms}, and the jitter in the DQS signal is 5.41 ps_{rms}.

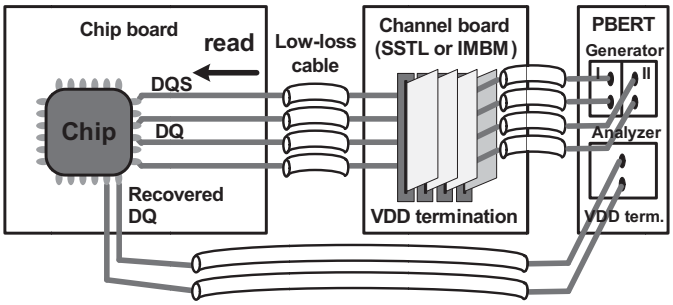

Fig. 20. Setup III for measuring the RX BER.

B. BER of Transmitted Signals

A further comparison between the SSTL and IMBM DQ bus was made by measuring the BER of transmitted signals, using the measurement setup shown in Fig. 18. Unlike an oscilloscope, a BERT (Agilent J-BERT N4903A) can provide a V_{DD}-level termination voltage, allowing us to dispense with the DC block and ground-terminated channel board.

The unequalized bathtub graph of Fig. 19(a) shows that the signal transmitted through SSTL modules #5 and #7 have no timing margin. This can be related to the single-bit response and the eye diagrams. The equivalent bathtub curve for the unequalized IMBM DQ bus has a BER that approaches 10^{-7} at the optimum sampling point. When the transceiver enables TX de-emphasis, the difference between the SSTL and IMBM results becomes more noticeable. The IMBM DQ bus achieves a BER of 10^{-9} with a timing margin of 0.39 UI, as shown in Fig. 19(b). However, some modules of the SSTL DQ bus do not reach a BER of 10^{-9} at any sampling positions, as we see in Fig. 19(a).

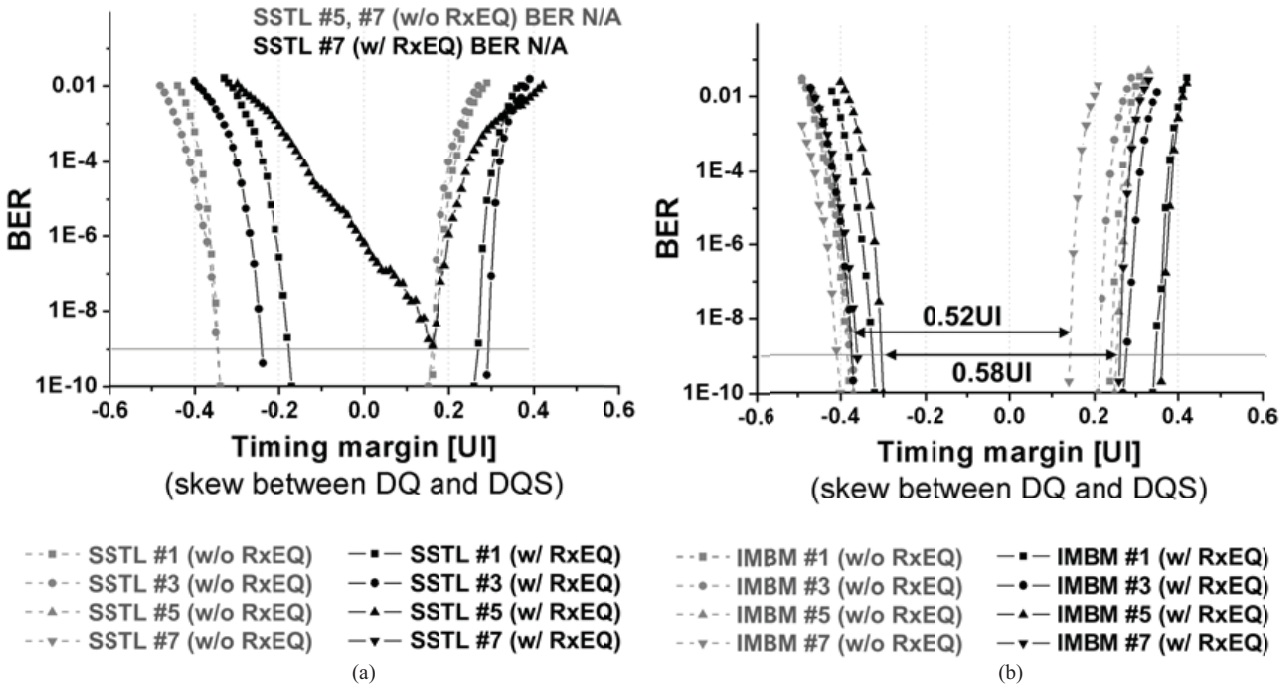

Fig. 21. Bathtub graph based on RX BER measurements of (a) SSTL and (b) IMBM signals.

C. BER of Recovered Signals

A memory interface channel is bidirectional. In write operations (the TX mode of the memory controller transceiver) data are transmitted from the chip board to the channel board. During read operations (the RX mode of the memory controller transceiver) data from the channel board are received by the chip board. To verify correct bidirectional operation of the IMBM DQ bus, we configured the RX measurement setup shown in Fig. 20. In RX mode, the transceiver extracts the phase information of every DQ signal with respect to the common DQS signal. Thus both the DQ and DQS signals must be generated and transmitted simultaneously by the BERT. The Agilent PBERT 81250 is a parallel BERT, which can handle both DQ and DQS signals, and so we used this instrument to measure the RX BER. If intentional skew between the generated DQ and DQS signals is asserted, we can draw a bathtub graph for the memory controller transceiver during RX mode that is similar to that for the TX BER results.

Fig. 21 shows bathtub graphs based on the measurement of RX BER for unequalized and equalized received signals. In RX mode, a linear equalizer is used, and the BER results generally indicate a larger timing margin than the TX BER results. This is because the PBERT has an ideal wide-bandwidth driver. Fig. 21(a) shows that data recovered from the unequalized SSTL DQ bus have many errors, originating in modules #5 and #7, which would not be acceptable in manual operation; this is similar to the TX results. However, the IMBM DQ bus has a timing margin of 0.52 UI when the BER is 10^{-9}, as shown in Fig. 21(b). When the memory controller transceiver turns on the linear equalizer and boosts the high-frequency gain, the SSTL DQ bus still has no timing margin; but the IMBM DQ bus has a timing margin of 0.58 UI.

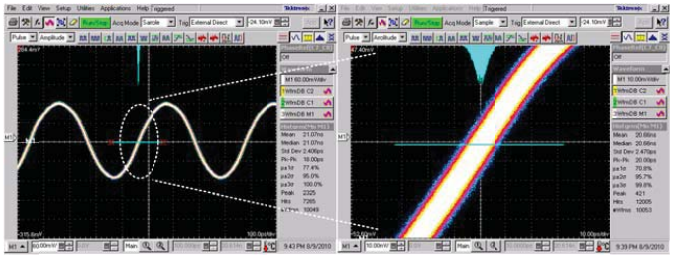

Fig. 22. Measured 4.8-Gb/s eye diagram and histogram of a recovered DQ signal with the pattern 10101010. . ., both on the IMBM DQ bus.

To check correct operation of the SRU, we measured the recovered clock jitter. The recovered clock pin was not assigned to the transceiver, and so we measured the jitter of the recovered clock signal by attempting to recover a 1010101010… data pattern. Fig. 22 shows the 4.8-Gb/s eye diagram and a histogram of the recovered DQ signal on the IMBM DQ bus. The measured jitter of the recovered clock is 2.47 ps_{rms}. The hunting jitter caused by the limit cycle is low, and the histogram shows a single Gaussian peak, rather than two. We attribute this to the use of a first-order $\Delta\Sigma$ modulator in the bang–bang loop of the SRU.

The memory controller transceiver is split into three different power domains: 1) the I/O circuits (driver and linear EQ buffer); 2) the analog circuits (PRBS generator, serializer, sampler, deserializer, PRBS verifier and clock trees); and 3) the remaining circuits. In TX mode at 4.8 Gb/s, the I/O domain consumes 39.5 mA/DQ and the analog domain consumes 17.5 mA/DQ. Thus the energy efficiency of the transceiver in TX mode is 14.25 mW/Gb/s/DQ. In RX mode, the I/O domain consumes 36 mA/DQ and the analog domain consumes 18.75 mA/DQ. The energy efficiency of each DQ of

TABLE I
PERFORMANCE SUMMARY

Process	0.13 μm 1P8M CMOS			
Connector	MicroTCA			
Package	TQFP 100p			
Data rate	4.8 Gb/s			
DQ bus	SSTL, 4 slots (8 drops)		IMBM, 4 slots (8 drops)	
Inactive modules	50 Ω only [12]	50 Ω ∥ 1 pF	50 Ω only [12]	50 Ω ∥ 1 pF
TX timing margin at 10-9 BER (w/o TxEQ)	Fail	Fail	Fail	Fail
TX timing margin at 10-9 BER (w/ TxEQ)	Fail	Fail	0.39 UI	0.39 UI
RX timing margin at 10-9 BER (w/o RxEQ)	Fail	Fail	0.61 UI	0.52 UI
RX timing margin at 10-9 BER (w/ RxEQ)	0.52 UI	Fail	0.73 UI	0.58 UI
Energy efficiency (at 4.8 Gb/s, per DQ)	14.24 mW/Gb/s (TX mode) 13.69 mW/Gb/s (RX mode)			

the memory controller transceiver is 13.69 mW/Gb/s/DQ. The performance of the transceiver chip and the channel board are summarized in Table I.

V. CONCLUSION

We proposed a new IMBM DQ bus, in which reflections at the stub of each channel are canceled by series resistors between the connectors. Our DQ bus canceled reflections unidirectionally, directly eliminating reflections during write operations; although reflections did occur during the read operation, they never reached the destination ports. This allowed our IMBM DQ bus to achieve bidirectional multiple gigabit per second data transmission rates with a multidrop configuration.

We also implemented a 4.8-Gb/s memory controller transceiver optimized to the IMBM DQ bus and IMBM channel board, and verified their effective operation by means of TX and RX BER measurements. We showed that reflective ISI is indeed eliminated in the IMBM DQ bus, and the signal integrity was much better than that observed in a conventional SSTL DQ bus. By applying TX de-emphasis and RX linear equalization to an 8-drop IMBM DQ bus, a timing margin of more than 0.39 UI with a BER of 10^{-9} can be achieved in both TX and RX modes. We fabricated the memory controller transceiver in a 0.13-μm standard CMOS process. In this form, it consumes 14.25 mW/Gb/s per DQ at 4.8 Gb/s in TX mode, and 13.69 mW/Gb/s per DQ at 4.8 Gb/s in RX mode.

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