Suhwan Kim, Seoul National University, Seoul Korea

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October 1, 2014

SUHWAN KIM (IEEE Senior Member) received the B.S. and M.S. degrees in Electrical Engineering and Computer Science from Korea University, Seoul Korea, in 1990 and 1992, respectively and the Ph.D. degree in Electrical Engineering and Computer Science from the University of Michigan, Ann Arbor MI, in 2001. From 1993 to 1999, he was with LG Electronics, Seoul Korea. From 2001 to 2004, he was a Research Staff Member in IBM T. J. Watson Research Center, Yorktown Heights NY. In 2004, Dr. Kim joined Seoul National University, Seoul Korea, where he is currently Tenured Professor of Electrical and Computer Engineering.

He has received the 1991 Best Student Paper Award of the IEEE Korea section. He has also received the Best Paper Award of the 2009 Korean conference on semiconductors and the Excellent Teaching Award of the College of Engineering, Seoul National University in 2010 and 2012. He received the Best Paper Award of the International Symposium on Low-Powr Electronics and Design (ISLPED'11). Recently, he received Shiyang Enerngineering Award (2013).

He served as a guest editor for IEEE Journal of Solid-State Circuits. He has also served as the general co-chair and technical program chair for the IEEE International SOC Conference. He has multiple times participated on the technical program committee of the IEEE International SOC Conference (SOCC), the International Symposium on Low-Power Electronics and Design (ISLPED), the IEEE Asian Solid-State Circuits Conference (A-SSCC), and the IEEE International Solid-State Circuits Conference (ISSCC). He is a Senior Member of IEEE.

His research interests include low-power integrated circuit and systems, Sensor Readout Integrated Circuit (ROIC), serial I/O interface and clocking, digitally calibrated analog and mixed-signal integrated circuits, and device/circuit co-design opportunities. Until now, Dr. Kim has published more than **165** papers in international and local/regional refereed journals and conferences, and his accumulated citation number (Google Scholar, September 2014) is **1,299**. Also Dr. Kim holds **45** (*including **17** US patents*) issued patents.

Energy-Recovery Circuits + Low-Power Digital Circuits and Architecture: Dr. Kim has made one of exceptional contributions to research in the field of low-power integrated circuits, specifically high-speed enery-recovery (*adiabatic* or *charge-recovery*) circuits and resonant clocking that offer an alternative approach to the reduction of dynamic energy dissipation. The charge-recovery multiplier designed, fabricated, and experimentally confirmed its correct operation for clock rates up to 140MHz made him receive the **First Prize** (operational category) in the VLSI design contest of the 2001 ACM/IEEE design automation conference (**DAC'01**). Most recently, Dr. Kim's research on "Bitline Techniques with Dual Dynamic Nodes for Low-Power Register Files," was published in IEEE Transactions on Circuits and Systems-I.

Power Gating and Power-Mode Transition Noise: For the first time ever (**ISLPED'03, ISLPED'04**), Dr. Kim introduced and analyzed the ground bounce noise due to power mode transition in power gating. Also, he has proposed and experimentally proved the effectiveness of his several novel power gating structures in which sleep transistors are turned on in a non-uniform manner. Nowadays, worldwide major semiconductor companies including TI, Intel, IBM, AMD, and SAMSUNG recognize the seriousness of the noise problem and adopt the variations of Dr. Kim's power gating structures to solve it in their commercial products. Most recently, Dr. Kim's research on "Power-Gating Noise Minimization by Three-

Step Wake-up Partition," was published in IEEE Transactions on Circuits and Systems-I.

High-Speed Serial I/O Circuits and Clocking: As CMOS technology continues to advance, the computing capabilities of integrated circuits are expanding dramatically. This brings demand for serial I/O interface. The development of the high-speed I/O circuits and clocking systems to be compatible with deep submicron CMOS technologies is one of Dr. Kim's major research interests. Recent research on"4.8Gb/s Impedance-Matched Bi-Directional Multi-Drop Transceiver for High Capacity Memory Interface" present at **ISSCC'11**. With the reseach on "A Low-Power Referenceless Clock and Data Recovery Circuit with Clock-Edge Modulation for Biomedical Sensor Applications", Dr. Kim has received the **Best Paper Award** at **ISLPED'11**. Most Recently, Dr. Kim's reseach on "A 4-Slot, 8-Drop Impedance-Matched Bidirectional Multi-Drop DQ Bus with a 4.8-Gb/s Memory Controller Transceiver," was published in IEEE Transactions on Components, Packaging and Manufacturing Technology.

Low-Power Low-Noise Analog Circuit: Since 2008, Dr. Kim has worked on ReadOut Integrated Circuits for various sensors. In 2010, Dr. Kim published "Biosensor System-on-a-chip including CMOS-based Signal Processors and 64 Carbon Nanotube-based Sensors for the Detection of a Neurotransmitter" in Lab on a Chip. Dr. Kim's reseach on "Integrating metal-oxide-decorated CNT networks with a CMOS readout in a gas sensor" experimentally demonstrated an innovated sensor system, which CNT-Network, CNT Sensor Array structure, ROIC circuit, and I/O interface are integrated on a single-die. Recently, "Detection and Identification of Breast Cancer Volatile Organic Compounds Biomarkers Using Highly-Sensitive Single Nanowire Array on a Chip" and "A Highly Selective Chemical Sensor Array Based on Nanowire Array / Nanostructure for Gas Identification," were published in Journal of Biomedical Nanotechnology and in Sensor and Actuator: B - Chemical (SnAB), respectively. Most Recently, Dr. Kim's reseach on "A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM," was published in IEEE Journal of Solid-State Circuits.

PROFESSIONAL EXPERIENCE

Seoul National University, Seoul Korea
Professor of Electrical Engineering, March 2013~present
Associate Professor of Electrical Engineering, March 2008~February 2013
Assistant Professor of Electrical Engineering, March 2004~February 2008
Hyundia KEFICO-Hyundia AUTRON (Hyndia Motor Group), Korea
Advisory Consultant, March 2013~February 2014
SK Hynix Inc., Korea
Principal Consultant of Mobile DRAM Development Division, January 2012~August 2012
IBM T. J. Watson Research Center, Yorktown Heights NY
Research Staff Member, February 2001~February 2004
University of Michigan, Ann Arbor MI
Research Assistant,
Advanced Computer Architecture Laboratory, September 1997~February 2001
LG Electronics Institute of Technology, Seoul Korea
Research Engineer, October 1993~May 1999

Suhwan Kim, Seoul National University, Seoul Korea

EDUCATION:

University of Michigan, Ann Arbor MI,
Ph.D. Electrical Engineering, December 2000
Dissertation: *True Single-Phase Adiabatic Circuitry for High-Performance, Low-Energy VLSI*
Korea University, Seoul Korea
M.S. Electrical Engineering, February 1992
Thesis: *Extended Fuzzy Clusterting Algorithm and Its Applications*
B.S. Electrical Engineering and Computer Science, February 1990

HONORS AND AWARD:

1. SINYANG Faculty Achievement Award, College of Enginneering, Seoul National University, December, 2013.
2. Faculty Recognition Award, SK Hynix, January 2013.
3. Excellent Teaching Award, College of Enginneering, Seoul National University, March 2012.
4. Best Paper Award, International Symposium on Low-Power Electronics and Design (sponsored by ACM, IEEE, SIGA, IEEE Circuits and Systems Society (CAS), IEEE Solid-State Circuits Society (SSCS), IEEE Electron Device Society (EDS), SPS, EiC), August 2011.
5. Outstanding Faculty Achievement Award, Electrical Engineering, Seoul National University, March 2010.
6. Excellent Teaching Award, College of Enginneering, Seoul National University, March 2010.
7. Best Stundet Paper Award (Hyunjoong Lee, Ph.D. candidate supervised), IEEE Seoul Section, December, 2009
8. System-on-a-Chip (SoC) Design Contest Award Winner (with J.-K. Woo and S.-H. Ahn), Ministry of Knowledge Economy, Korea, November 2009.
9. Best Paper Award, Korean Conference on Semiconductors, February 2009.
10. Faculty Recognition Award, System LSI Division, Samsung Electronics' Semiconductor Business, January 2007.
11. Recognition Award, IEEE International SOC Conference, September 2003.
12. IBM Invention Achievement Awards, March and August 2003.
13. First Prize in VLSI Design Contest: Operational Category of the 2001 ACM/IEEE Design Automation Conference, June 2001. (To submit a design to operational category, the design should be implemented and tested on silicon. Proof of implementation in the form of die-photographs and measurement data must be supplied.)
14. Best Student Paper Award, IEEE Korea Section, December 1991.

PROFESSIONAL ACTIVITIES:

1. Guest Editor, IEEE Journal of Solid-State Circuits, November 2007.
2. Vice Chair, Asian Solid-State Circuits Conference, 2006.
3. General Co-Chair (2007),
   Steering Committee Chair (2008), and
   Tutorial Chair (2003, 2004), IEEE International SOC Conference.
4. Technican Program Chiars (2005, 2006), IEEE International SOC Conference.
5. Program Committee Member:
   - *ISSCC*: IEEE International Solid-State Circuits Conference, 2008 and 2009.

- *ISLPED*: IEEE International Symposium on Low Power Electronics and Design, 2003, 2004, 2005, 2006, and 2009, 2011, 2012.
- *SOCC*: IEEE International SOC Conference (formerly IEEE International ASIC/SOC Conference), 2001~2014.
- *A-SSCC*: Asian Solid-State Circuits Conference, 2006.

6. Referee for the Journals:
   - IEEE Journal of Solid-State Circuits, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems-I and –II.
   - ACM Transactions on Design Automiation of Electronic Systems.
   - IBM Journal of Research and Development.
   - EURASIP Journal on Advances in Signal Processing.
   - IEEE Electronics Letters.
   - IEEE Transactions on Instrumentation & Measurement.

UNIVERSITY SERVICE

1. Department Vice Chair (Electrical and Computer Engineering), Setember 2012~August 2014
2. Steering Committee (Inter-University Semiconductor Research Center), Setember 2012~August 2014
3. Editorial Board Member (College of Engineering)
4. University Admission Selection Committee Member
5. Council Member of the Association of Faculty of Engineering
6. Brain Korea 21 (BK21 and BK21 PLUS) Information Technology Program Committee Member
7. Faculty Search Committee Member (Electrical and Computer Engineering)
8. Industry Partner Program Committee Member (Electrical and Computer Engineering)

PROFESSIONAL SOCIETIES

1. Senior Member, Institute of Electrical and Electronics Engineers (IEEE)
2. Member of IEEE Circuits and Systems Society
3. Member of IEEE Solid-State Circuits Society
4. Life Member, Institute of Electronics Engineers of Korea (IEEK)
5. 2013~2014-IEEK Board of Directors
6. Life Member, Korea Information and Communication Society (KICS)

U.S. PATENTS:

Issued

1. H.-W. Lee, G.-O. Jung, S. Kim, A.-R. Kim, and R. Singh, “Domino logic circuits and pipelined domino logic circuits”, US 8,542,033, September 24, 2013.
2. D.-K. Jeong, S. Kim, W.-Y. Shin, and D.-H. Lim, "Bi-Directional Multi-Drop Memory System," US 8,195,855, June 5, 2012.
3. H. Lee, Y. S. Kim, and S. Kim, “Operational Amplifier,” US 7,714,656, May 11, 2010.
4. S. Kim and C.-J. Choi, “Semiconductor device using power gating,” US 7,705,627, Apr. 27, 2010.
5. C.-J. Choi and S. Kim, “Semiconductor integrated circuit device and power control method

thereof," US 7,659,773, Fab. 9, 2010.
6. C.-J. Choi and S. Kim, "Power Control Circuit for Semiconductor IC," US 7,643,368, Jan. 5, 2010.
7. S. Kim, J.-K. Woo, and H. Yang, "Multi-Channel Pipelined Signal Converter," US 7,495,596, Feb. 24, 2009.
8. S. Kim, D. Knebel, and S. V. Kosonocky, "Charge Recycling Power Gate," US 7,486,108, Feb. 3, 2009.
9. S. Kim, P. Sandon, T. E. Cook, I. R. Govett, and S. V. Kosonocky, "Machine Code Builder Derived Power Consumption Reduction," US 7,185215, Feb. 27, 2007.
10. S. Kim, S. V. Kosonocky, and D. Knebel, "Charge Recycling Power Gate," US 7,138,825, Nov. 21, 2006.
11. S. Kim and S. V. Kosonocky, "Performance Increase Technique for Use in a Register File having Dynamically Boosted Wordlines," US 6,977,519, Jan. 17, 2006.
12. S. Kim, S. V. Kosonocky, A. Bhavnagarwala, and D. R. Knebel, "Digital Logic with Reduced Leakage," US 6,977,519, Dec 20, 2005.
13. S. Kim, S. V. Kosonocky, and D. Knebel, "Non-Abrupt Switching of Sleep Transistor of Power Gate Structure," US 6,876,252, April 5, 2005.
14. C.-H. Min, S. Kim, S.-J. Min, and S. Bae, "Method for Decoding MPEG Standard Video Bit Stream," US 6,118,818, 2000.
15. S. Kim and S. Bae, "High Speed Variable Length Decoder," US 5,949,356, 1999.
16. S. Kim and S. Bae, "High Speed Variable Length Decoder," US 5,781,135, 1998.
17. S. Kim and S. Bae, "Bit-Pattern Detector," US 5,748,688, 1998.

Published

16. K.-D. Kim, S. Kim, G.-M. Hong, "Integrated Circuit with Ring Oscillator," Pub. No. US 2014/0132360 A1, May 15, 2014: Foreign Application Priority Data: Nov. 14, 2012 (KR) – 10-2012-0128985.
17. J.-H. Kim, D.-Y. Shin, and S. Kim, " Semiconductor Device," Pub. No. US 2014/0146852 A1, May 29, 2014: Foreign Application Priority Data: Nov. 13, 2012 (KR) – 10-2012-0134048.
18. S. Kwon, Y. Park, and S. Kim, "Optical Identification Tag, Reader and System," Pub. No. US 2010/0096447 A1, April 22, 2010.
19. J. H. Choi, J. H. Seo, S. Kim, J. W. Kwon, and J. S. Kim, "Driving A Light Scanner," Pub. No. US 2009/0278824 A1, November 12, 2009: : Foreign Application Priority Data: July 21, 2008, 2012 (KR) – 10-2008-0070498.
20. S. Kim, S.V. Kosonocky, and P. A. Sandon, "A Method and Apparatus for Controlling Power Consumption in An Integrated Circuit," Pub. No. US 2006/0064606 A1, March 23, 2006.
21. S. Kim and S. V. Kosonocky, "An Integrated Circuit having Parallel Execution Units with Differing Execution Latencies," Pub. No. US 2004/0225868 A1, November 11, 2004.

INTERNATIONAL PUBLICATIONS:

Accumulated Citations=1299 (Google Scholar, September 2014)

Journals

1. A. Kavala, W. Bae, S. Kim, G.-M. Hong, H. Chi, S. Kim, and D.-K. Jeong, "A PVT-compensated 2.2 to 3.0 GHz Digitally Controlled Oscillator for All-Digital PLL," Journal of Semiconductor

Technology and Science, vol. 14, no. 4, pp. 484-494, August 2014.
2. J.-K. Woo, T. Kim, and S. Kim, "A Comparator-Based Cyclic Analog-to-Digital Converter with Multi-level Input Tracking Boosted Preset Voltage," Analog Integrated Circuits and Signal Processing, Published online: 09 September 2014.
3. J.-K. Woo, H. Lee, H.-C. Kim, D.-K. Jeong, and S. Kim, “1.2V 10-bit 75MS/s Pipelined ADC with Phase-Dependent Gain-Transition CDS,” IEEE Transactions on Very Large Scale Integration VLSI Systems, vol. 22, no. 3, pp. 585-592, March 2014.
4. D. Shim, H. Jeong, H. Lee, C. Rhee, D.-K. Jeong, and S. Kim, "A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM," IEEE Journal of Solid-State Circuits, vol. 48, no. 10, pp. 2550-2557, October 2013.
5. Y. Xu, H. Lee, Y. Hu, J. Huang, S. Kim, and M. Yun, "Detection and Identification of Breast Cancer Volatile Organic Compounds Biomarkers Using Highly-Sensitive Single Nanowire Array on a Chip," Journal of Biomedical Nanotechnology, vol. 9, pp. 1164-1172, July 2013.
6. Y. Hu, H. Lee, S. Kim, and M. Yun, "A Highly Selective Chemical Sensor Array Based on Nanowire Array / Nanostructure for Gas Identification," Sensor and Actuator: B - Chemical (SnAB), vol. 181, pp. 424-431, May 2013.
7. W.-Y. Shin, G.-M. Hong, H. Lee, J.-D. Han, K.-S. Park, D.-H. Lim, S. Kim, D. Shim, J.-H. Chun,D.-K. Jeong, and S. Kim, "A 4-Slot, 8-Drop Impedance-Matched Bidirectional Multi-Drop DQ Bus with a 4.8-Gb/s Memory Controller Transceiver," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 3, no. 5, pp. 858-869, May 2013..
8. R. Singh, G.-M. Hong, and S. Kim, "Bitline Techniques with Dual Dynamic Nodes for Low-Power Register Files," IEEE Transactions on Circuits and Systems-I, vol. 60, no. 4, pp. 965-974, April 2013.
9. S. Kim, J.-K. Woo, W.-Y. Shin, G.-M. Hong, H. Lee, H. Lee, and S. Kim, "A 10Mbps, 0.8pJ/bit, Referenceless Clock and Data Recovery Circuit for Optically Controlled Neural Interface System," IEEE Transactions on Circuits and Systems-II, vol. 60, no. 1, pp. 6-10, January 2013.
10. H. Kim, S. Kim, and Y. Hong, “Frequency Dependency of Multi-Layer OLED Current Density-Voltage Shift and Its Application to Digitally-Driven AMOLED,” Journal of the Optical Society of Korea (JOSK), vol. 16, issue 2, pp. 181-184 (2012).
11. R. Singh, G. M. Hong, M. Kim, J. Park, W.-Y. Shin, and S. Kim, "Static-switching pulse domino: A switching-aware design technique for wide fan-in dynamic multiplexers," Integration, the VLSI Journal, vol. 45, no. 3, pp. 253-262, June 2012 **[Special Issue of GLSVLSI 2011: Current Trends on VLSI and Ultra Low-Power Design]**.
12. G. M. Hong, W.-Y. Shin, D. Shin, J.-H. Park, M.-O. Kim, and S. Kim, "'High-Speed Phase Rotator using Resistive Interpolation for a 3.75-6.9Gb/s Serial-Link Receiver," accepted for publication in IEE Electronics Letters, vol.48, no.8, pp.429-430, April 2012.
13. R. Singh, J.-K. Woo, H. Lee, S. Y. Kim, and S. Kim, “Power-Gating Noise Minimization by Three-Step Wake-up Partition,” IEEE Transactions on Circuits and Systems-I, vol. 59, no. 4, pp.749-762, April 2012.
14. H. Lee, S. Lee, Y. J. Park, D. Perello, D.-H. Kim, S.-H. Hong, M. Yun, and S. Kim, "Integrating metal-oxide-decorated CNT networks with a CMOS readout in a gas sensor," Sensors, 2012, 12(3), 2582-2597.
15. S. Kim, H. Lee, H. Lee, J.-K. Woo, J. Cheon, H. Y. Kim, Y. J. Park and S. Kim, “Optical Failure Analysis Technique in Deep Submicron CMOS Integrated Circuits,” Journal of Semiconductor Technology and Science, vol. 11, no. 4, December 2011.
16. D.-Y. Shin, H. Lee, and S. Kim, “Improving the Accuracy of Capacitance-to-Frequency Converter by Accumulating Residual Charges,” IEEE Transactions on Instrumentation and Measurement, vol. 60, no. 12, December 2011.

17. M. Kim, H. Lee, J.-K. Woo, N. Xing, M.-O. Kim, and S. Kim, “A Low-Cost and Low-Power Time-to-Digital Converter Using Triple-Slope Time-Stretching,” IEEE Transactions on Circuit and System-II, vol. 58, no. 3, pp. 169-173, March 2011.
18. D.-Y. Shin, H. Lee, and S. Kim, “A Delta-Sigma Interface Circuit for Capacitive Sensors with an Automatically Calibrated Zero Point,” IEEE Transactions on Circuit and System-II, vol. 58, no. 2, pp. 90-94, February 2011.
19. H. Song, D.-S. Kim, D.-H. Oh, S. Kim, and D.-K. Jeong, “A 1.0-4.0Gb/s All-Digital CDR with 1.0-ps Resolution DCO and Adaptive Proportional Gain Control,” IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp.424-434, February 2011.
20. N. Xing, J.-K. Woo, W.-Y. Shin, H. Lee, and S. Kim, “A 14.6 ps Resolution, 50 ns Input-Range Cyclic Time-to-Digital Converter using Fractional Difference Conversion Method,” IEEE Transactions on Circuits and Systems-I, vol. 57, no. 12, pp.3064-3072, December 2010.
21. D.-S. Kim, H. Song, T. Kim, S. Kim, and D.-K. Jeong, “A 0.3–1.4 GHz All-Digital Fractional-N PLL with Adaptive Loop Gain Controller,” IEEE Journal of Solid-State Circuits, vol. 45, no. 11, pp.2300-2311, November 2010.
22. H. Lee, J.-K. Woo, and S. Kim, “Charge Amplifier with Enhanced Frequency Response for SPM-Based Data Storage,” IEEE Transactions on Circuits and Systems-II, vol. 57, no. 9, pp. 691-695, September 2010.
23. W.-Y. Shin, M. Kim, G.-M. Hong, and S. Kim, “A Fast-Acquisition PLL using Split Half-Duty Sampled Feedback Loop Filter,” IEEE Transactions on Consumer Electronics,vol. 56, no. 3, August 2010.
24. S. Lee, H. Lee, J.-K. Woo, and S. Kim, “A Low-Voltage Bandgap Reference with Output-Regulated Current Mirror in 90nm CMOS,” IEE Electronics Letters, vol.46, no.14, pp.976-977, July 2010.
25. H. Lee, J.-K. Woo, and S. Kim, “A CMOS Differential-Capacitance-to-Frequency Converter Utilizing Repetitive Charge Integration and Charge Conservation,” IEE Electronics Letters, vol.46, no.8, pp.567-569, April 2010.
26. N. Xing, W.-Y. Shin, D.-K. Jeong, and S. Kim, “A High-Resolution Time-to-Digital Converter utilizing Fractional Difference Conversion Scheme,” IEE Electronics Letters, vol.46, no.6, pp.398-400, March 2010.
27. D.-Y. Shin, J.-K. Woo, Y. Hong, and S. Kim, “Quantitative evaluation of image sticking on displays with different gradual luminous variation,” Journal of SID, Journal of SID, vol. 18, no 3, pp.228-234, March 2010.
28. B. Y. Lee, S. M. Seo, D. J. Lee, M. Lee, J. Lee, J.-H. Cheon, E. Cho, H. Lee, I.-Y. Chung, Y. J. Park, S. Kim, and S. Hong, “Biosensor System-on-a-chip including CMOS-based Signal Processors and 64 Carbon Nanotube-based Sensors for the Detection of a Neurotransmitter,” Lab on a Chip, vol. 10, pp. 894-898, March 2010.
29. D.-Y. Shin, J.-K. Woo, Y. Hong, and S. Kim, “Reducing image sticking in AMOLED displays with time-ratio grayscale by analog calibration,” Journal of SID, vol. 17, no 9, pp.705-713, September 2009.
30. H.-W. Lee, H. Lee, J.-K. Woo, W.-Y. Shin and S. Kim, “A Low-Power Register File with Dual-Vt Dynamic Bit-Lines driven by CMOS Bootstrapped Circuit,” Journal of Semiconductor Technology and Science, vol. 9, no. 3, pp.148-152, Sept. 2009.
31. J.-K. Woo, D.-Y. Shin, D.-K. Jeong, and S. Kim, “High-Speed 10-bit LCD Column Driver with a Split DAC and a Class-AB Output Buffer,” IEEE Transactions on Consumer Electronics, vol. 55, no. 3, pp.1431-1438, August 2009.
32. H. Song, S. Kim, and D.-K. Jeong, “A Reduced-Swing Voltage-Mode Driver for Low-Power Multi-Gb/s Transmitters,” Journal of Semiconductor Technology and Science, vol. 9, no. 2, pp.104-109, June 2009.

33. Y.-D. Kim, H.-S. Ahn, S. Kim, and D.-K. Jeong, “A High-Speed Range-Matching TCAM for Storage-Efficient Packet Classification,” IEEE Transactions on Circuits and Systems-I, vol. 56, no. 6, pp.1221-1230, June 2009.
34. J.-H. Lee, S. Kim, and D.-K. Jeong, “A Combined Clock and Data Recovery Circuit with Adaptive Cancellation of Data-Dependent Jitter,” Journal of Semiconductor Technology and Science, vol. 8, no. 3, pp.193-199, September 2008.
35. H.-W. Lee, H. Lee, J.-K. Woo, W.-Y. Shin, and S. Kim, “Power-Gating Structure with Virtual Power-Rail Monitoring Mechanism,” Journal of Semiconductor Technology and Science, vol. 8, no. 2, pp.134-138, June. 2008.
36. S. Kim, C. Choi, D.-K. Jeong, S. V. Kosonocky, and S. Park, “Reducing Ground Bounce Noise and Stabilizing the Data Retention Voltage of Power Gating Structures,” IEEE Transactions on Electron Devices, vol. 55, no. 1, pp.197-205, Jan. 2008. [Special Issue on Device Technologies and Circuits Techniques for Power Management].
37. S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, and M. C. Papaefthymiou, “A Multi-Mode Power Gating Structure for Low-Voltage Deep-Submicron CMOS ICs,” IEEE Transactions on Circuits and Systems-II, vol. 54, no. 7, pp. 586-590, July 2007.
38. H. Jeong, B.-J. Yoo, C. Han, S.-Y. Lee, K.-Y. Lee, S. Kim, D.-K. Jeong, and W. Kim, “A 0.25μm CMOS 1.9-GHz PHS RF Transceiver with a 150-kHz Low-IF Architecture,” IEEE Journal of Solid-State Circuits, vol.42, no.6, pp.1318-1327, June 2007.
39. J.-K. Woo, D.-K. Jeong, and S. Kim, “A Fast-Locking CDR Circuit with Autonomously Reconfigurable Mechanism,” IEE Electronics Letters, vol.43, no.11, pp.624-626, May 2007.
40. V. Visvesh, M. C. Papaefthymiou, S. V. Kosonocky, and S. Kim, “On-Chip Synchronous Communication between Clock Domains with Quotient Frequencies,” IEE Electronics Letters, vol. 43, no. 9, pp.497-499, April 2007.
41. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, “Charge-Recovery Computing in Silicon,” IEEE Transactions on Computers, vol. 54, no. 6, pp.651-659, June 2005. **[Special Section on Energy Efficent Computing]**.
42. J.-S. Ahn, D.-K. Jeong, and S. Kim, “Fast Three-Dimensional Programmable Two-Selector,” IEE Electronics Letters, vol. 40, no. 18, pp.1098-1099, September 2004.
43. S. Hong, S.-S. Chin, S. Kim, and W. Hwang, “Power Reduction Technique in Coefficient Multiplications through Multiplier Characterization,” Journal of VLSI Signal Processing, vol. 38, no. 2, pp.101-113, September 2004.
44. J.-O. Plouchart, N. Zamdmer, J. Kim, M. Sherony, Y. Tan, A. Ray, M. Talbi, L. F. Wagner, K. Wu, N. E. Lustig, S. Narasimha, P. O'Neil, N. Phan, M. Rohn, J. Strom, D. M. Friend, S. V. Kosonocky, D. R. Knebel, S. Kim, K. A. Jenkins, and M. M. Rivier, “Application of an SOI 0.12μm CMOS Technology to SoCs with Low-Power and High-Frequency Circuits,” IBM Journal of Research and Development, vol. 47, no. 5/6, pp.611-629, September/November 2003.
45. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, “Fine-Grain Real-Time Reconfigurable Pipelining,” IBM Journal of Research and Development, vol. 47, no. 5/6, pp.599-609, September/November 2003 **[Special Issue on Power-Efficient Computer Technologies]**.
46. S. Kim and C. H. Ziesler, “A Clockless Future of Systems on Chip,” Design & Test of Computers: Special Issue on Clockless VLSI Design, vol. 20, no. 6, November/December 2003.
47. S. Kim, C. H. Ziesler and M. C. Papaefthymiou, “A True Single-Phase Energy-Recovery Multiplier,” IEEE Transactions on Very Large Scale Integration Systems, vol. 11, no. 2, pp. 194-207, April 2003.
48. S. V. Kosonocky, A. J. Bhavnagarwala, K. Chin, G. D. Gristede, A.-M. Haen, W. Hwang, M. B. Ketchen, S. Kim, D. R. Knebel, K. W. Warren, and V. Zyuban, “Low-Power Circuits and Technology for Wireless Digital Systems,” IBM Journal of Research and Development, vol. 47, no. 2/3, pp.283-298, March/May 2003 **[Special Issue on Communication Technologies]**.

49. S. Hong, S. Kim, and W. E. Stark, “Low-Power Application-Specific Parallel Array Multiplier Design for DSP applications,” VLSI Design: An International Journal of Custom-Chip Design, Simulation, and Testing, vol. 14, no. 3, pp.287-298, October 2002.
50. S. Kim and M. C. Papaefthymiou, “True Single-Phase Adiabatic Circuitry,” IEEE Transactions on Very Large Scaling Integration Systems, vol. 9, no. 1, pp.52-63, February 2001.
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