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October 1, 2012

SUHWAN KIM received the B.S. and M.S. degrees in Electrical Engineering and Computer Science from Korea University, Seoul Korea, in 1990 and 1992, respectively and the Ph.D. degree in Electrical Engineering and Computer Science from the University of Michigan, Ann Arbor MI, in 2001. From 1993 to 1999, he was with LG Electronics, Seoul Korea. From 2001 to 2004, he was a Research Staff Member in IBM T. J. Watson Research Center, Yorktown Heights NY. In 2004, Dr. Kim joined Seoul National University, Seoul Korea, where he is currently an Associate Professor of Electrical Engineering. His research interests include low-power integrated circuit and systems, Sensor Readout Integrated Circuit (ROIC), serial I/O interface and clocking, digitally calibrated analog and mixed-signal integrated circuits, and device/circuit co-design opportunities. Until now, Dr. Kim has published more than **130** papers in international and local/regional refereed journals and conferences, holds **43** (*including **16** US patents*) registered patents.

1998 ~ present (Energy-Recovery Circuits + Low-Power Digital Circuits and Architecture): Dr. Kim has made one of exceptional contributions to research in the field of low-power integrated circuits, specifically high-speed enery-recovery (*adiabatic* or *charge-recovery*) circuits and resonant clocking that offer an alternative approach to the reduction of dynamic energy dissipation. The charge-recovery multiplier designed, fabricated, and experimentally confirmed its correct operation for clock rates up to 140MHz made him receive the **First Prize** (operational category) in the VLSI design contest of the 2001 ACM/IEEE design automation conference (**DAC'01**). Most recently, Dr. Kim's research on "Bitline Techniques with Dual Dynamic Nodes for Low-Power Register Files," was accepted to be published in **IEEE Transactions on Circuits and Systems-I**.

2002 ~ present (Power Gating and Power-Mode Transition Noise): For the first time ever (**ISLPED'03, ISLPED'04**), Dr. Kim introduced and analyzed the ground bounce noise due to power mode transition in power gating. Also, he has proposed and experimentally proved the effectiveness of his several novel power gating structures in which sleep transistors are turned on in a non-uniform manner. Nowadays, worldwide major semiconductor companies including TI, Intel, IBM, AMD, and SAMSUNG recognize the seriousness of the noise problem and adopt the variations of Dr. Kim's power gating structures to solve it in their commercial products. Most recently, Dr. Kim's research on "Power-Gating Noise Minimization by Three-Step Wake-up Partition," was published in **IEEE Transactions on Circuits and Systems-I**, April 2012.

2001 ~ present (Serial I/O Circuits and Clocking): As CMOS technology continues to advance, the computing capabilities of integrated circuits are expanding dramatically. This brings demand for serial I/O interface. The development of the high-speed I/O circuits and clocking systems to be compatible with deep submicron CMOS technologies is one of Dr. Kim's major research interests. Recent research on"4.8Gb/s Impedance-Matched Bi-Directional Multi-Drop Transceiver for High Capacity Memory Interface" present at **ISSCC'11**. With the reseach on "A Low-Power Referenceless Clock and Data Recovery Circuit with Clock-Edge Modulation for Biomedical Sensor Applications", Dr. Kim has received the **Best Paper Award** at **ISLPED'11**.

2008 ~ present (Readout Integrated Circuits: R, C, and Time): Readout Circuit is the most critical part of a sensor system. Since 2008, Dr. Kim has worked on **ReadOut Integrated Circuits** for Bio-Chemical

sensors. In 2010, Dr. Kim published "Biosensor System-on-a-chip including CMOS-based Signal Processors and 64 Carbon Nanotube-based Sensors for the Detection of a Neurotransmitter" in Lab on a Chip. Recently published Dr. Kim's reseach on "Integrating metal-oxide-decorated CNT networks with a CMOS readout in a gas sensor" experimentally demonstrated an innovated sensor system, which **CNT-Network, CNT Sensor Array structure, ROIC circuit, and I/O interface are integrated on a single-die**.

He has received the 1991 **Best Student Paper Award** of the IEEE Korea section. He has also received the **Best Paper Award** of the 2009 Korean conference on semiconductors and the **Excellent Teaching Award** of the College of Engineering, Seoul National University in 2010 and 2012. Recently, he received the **Best Paper Award** of the International Symposium on Low-Powr Electronics and Design (**ISLPED'11**).

He served as a guest editor for IEEE Journal of Solid-State Circuits. He has also served as the general co-chair and technical program chair for the IEEE International SOC Conference. He has multiple times participated on the technical program committee of the IEEE International SOC Conference (**SOCC**), the International Symposium on Low-Power Electronics and Design (**ISLPED**), the IEEE Asian Solid-State Circuits Conference (**A-SSCC**), and the IEEE International Solid-State Circuits Conference (**ISSCC**). He is a Senior Member of IEEE.

PROFESSIONAL EXPERIENCE

Seoul National University, Seoul Korea
Associate Professor of Electrical Engineering, March 2008~present
Assistant Professor of Electrical Engineering, March 2004~February 2008
IBM T. J. Watson Research Center, Yorktown Heights NY
Research Staff Member, February 2001~February 2004
University of Michigan, Ann Arbor MI
Research Assistant,
Advanced Computer Architecture Laboratory, September 1997~February 2001
LG Electronics Institute of Technology, Seoul Korea
Research Engineer, October 1993~May 1999

EDUCATION:

University of Michigan, Ann Arbor MI,
Ph.D. Electrical Engineering, December 2000
Dissertation: *True Single-Phase Adiabatic Circuitry for High-Performance, Low-Energy VLSI*
Korea University, Seoul Korea
M.S. Electrical Engineering, February 1992
Thesis: *Extended Fuzzy Clusterting Algorithm and Its Applications*
B.S. Electrical Engineering and Computer Science, February 1990

Suhwan Kim, Seoul National University, Seoul Korea

HONORS AND AWARD:

1. Excellent Teaching Award, College of Enginneering, Seoul National University, March 2012.
2. Best Paper Award, International Symposium on Low-Power Electronics and Design (sponsored by ACM, IEEE, SIGA, IEEE Circuits and Systems Society (CAS), IEEE Solid-State Circuits Society (SSCS), IEEE Electron Device Society (EDS), SPS, EiC), August 2011.
3. Best M.S. Thesis Award (Nan Xing, M.S. student supervised), Electrical Engineering, Seoul National University, August 2010.
4. Outstanding Achievement Award, Electrical Engineering, Seoul National University, March 2010.
5. Excellent Teaching Award, College of Enginneering, Seoul National University, March 2010.
6. Best M.S. Thesis Award (Manho Kim, M.S. student supervised), Electrical Engineering, Seoul National University, February 2010.
7. Best Stundet Paper Award (Hyunjoong Lee, Ph.D. candidate supervised), IEEE Seoul Section, December, 2009
8. System-on-a-Chip (SoC) Design Contest Award Winner (with J.-K. Woo and S.-H. Ahn), Ministry of Knowledge Economy, Korea, November 2009.
9. Best Paper Award, Korean Conference on Semiconductors, February 2009.
10. Faculty Recognition Award, System LSI Division, Samsung Electronics' Semiconductor Business, January 2007.
11. Recognition Award, IEEE International SOC Conference, September 2003.
12. IBM Invention Achievement Awards, March and August 2003.
13. First Prize in VLSI Design Contest: Operational Category of the 2001 ACM/IEEE Design Automation Conference, June 2001. (To submit a design to operational category, the design should be implemented and tested on silicon. Proof of implementation in the form of die-photographs and measurement data must be supplied.)
14. Best Student Paper Award, IEEE Korea Section, December 1991.

PROFESSIONAL ACTIVITIES:

1. Guest Editor, IEEE Journal of Solid-State Circuits, November 2007.
2. Vice Chair, Asian Solid-State Circuits Conference, 2006.
3. General Co-Chair (2007),
   Steering Committee Chair (2008), and
   Tutorial Chair (2003, 2004), IEEE International SOC Conference.
4. Technican Program Chiars (2005, 2006), IEEE International SOC Conference.
5. Program Committee Member:
   - *ISSCC*: IEEE International Solid-State Circuits Conference, 2008 and 2009.
   - *ISLPED*: IEEE International Symposium on Low Power Electronics and Design, 2003, 2004, 2005, 2006, and 2009, 2011, 2012.
   - *SOCC*: IEEE International SOC Conference (formerly IEEE International ASIC/SOC Conference), 2001~2011,2012.
   - *A-SSCC*: Asian Solid-State Circuits Conference, 2006.
6. Referee for the Journals:
   - IEEE Journal of Solid-State Circuits, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems-I and –II.
   - ACM Transactions on Design Automiation of Electronic Systems.
   - IBM Journal of Research and Development.
   - EURASIP Journal on Advances in Signal Processing.

- IEEE Electronics Letters.
- IEEE Transactions on Instrumentation & Measurement.

UNIVERSITY SERVICE

1. Vice Chair (Electrical and Computer Engineering), Setember 2012
2. Steering Committee (Inter-university Semiconductor Research Center), Setember 2012
3. Editorial Board Member (Engineering), Septebmer 2012
4. University Admission Selection Committee Member
5. Council Member of the Association of Faculty of Engineering
6. Brain Korea 21 (BK21) Information Technology Program Committee Member
7. Faculty Search Committee Member (Electrical Engineering)
8. Industry Partner Program Committee Member (Electrical Engineering)

TEACHING

Course Taught

1. Logic Design
2. Digital System Design
3. Computer Architecture
4. Analog Integrated Circuits for Communication System
5. Deep Submicron Analog and RF Circuit Design
6. Digital Integrated Circuits
7. Microelectronics
8. Analog Integrated Circuits
9. Advanced Digital Integrated Circuits

Course Development or Significantly Revised

1. Digital System Design Laboratory Manual (Developed, Spring 2005)
2. Analog Integrated Circuits (Developed, Spring 2005)
3. Logic Design Laboratory Manual (Revised, Fall 2004)
4. Microelectronics (Revised, Fall 2008)

PROFESSIONAL SOCIETIES

1. Senior Member, Institute of Electrical and Electronics Engineers (IEEE)
2. Life Member, Institute of Electronics Engineers of Korea (IEEK)
3. Life Member, Korea Information and Communication Society (KICS)

PATENTS:

Issued

1. D.-K. Jeong, S. Kim, W.-Y. Shin, and D.-H. Lim, "Bi-Directional Multi-Drop Memory System," US 8,195,855, June 5, 2012.
2. H. Lee, Y. S. Kim, and S. Kim, “Operational Amplifier,” US 7,714,656, May 11, 2010.
3. S. Kim and C.-J. Choi, “Semiconductor device using power gating,” US 7,705,627, Apr. 27, 2010.

4. C.-J. Choi and S. Kim, "Semiconductor integrated circuit device and power control method thereof," US 7,659,773, Fab. 9, 2010.
5. C.-J. Choi and S. Kim, "Power Control Circuit for Semiconductor IC," US 7,643,368, Jan. 5, 2010.
6. S. Kim, J.-K. Woo, and H. Yang, "Multi-Channel Pipelined Signal Converter," US 7,495,596, Feb. 24, 2009.
7. S. Kim, D. Knebel, and S. V. Kosonocky, "Charge Recycling Power Gate," US 7,486,108, Feb. 3, 2009.
8. S. Kim, P. Sandon, T. E. Cook, I. R. Govett, and S. V. Kosonocky, "Machine Code Builder Derived Power Consumption Reduction," US 7,185215, Feb. 27, 2007.
9. S. Kim, S. V. Kosonocky, and D. Knebel, "Charge Recycling Power Gate," US 7,138,825, Nov. 21, 2006.
10. S. Kim and S. V. Kosonocky, "Performance Increase Technique for Use in a Register File having Dynamically Boosted Wordlines," US 6,977,519, Jan. 17, 2006.
11. S. Kim, S. V. Kosonocky, A. Bhavnagarwala, and D. R. Knebel, "Digital Logic with Reduced Leakage," US 6,977,519, Dec 20, 2005.
12. S. Kim, S. V. Kosonocky, and D. Knebel, "Non-Abrupt Switching of Sleep Transistor of Power Gate Structure," US 6,876,252, April 5, 2005.
13. C.-H. Min, S. Kim, S.-J. Min, and S. Bae, "Method for Decoding MPEG Standard Video Bit Stream," US 6,118,818, 2000.
14. S. Kim and S. Bae, "High Speed Variable Length Decoder," US 5,949,356, 1999.
15. S. Kim and S. Bae, "High Speed Variable Length Decoder," US 5,781,135, 1998.
16. S. Kim and S. Bae, "Bit-Pattern Detector," US 5,748,688, 1998.

Filed and Published

16. H.-W. Lee, G.-O. Jung, S. Kim, A.-R. Kim, and ahul, "Domino Logic Circuits and Pipelined Domino Logic Circuits," Pub. No. US 2012/0139584 A1, June 07, 2012.
17. S. Kwon, Y. Park, and S. Kim, "Optical Identification Tag, Reader and System," Pub. No. US 2010/0096447 A1, April 22, 2010.
18. J. H. Choi, J. H. Seo, S. Kim, J. W. Kwon, and J. S. Kim, "Driving A Light Scanner," Pub. No. US 2009/0278824 A1, November 12, 2009.
19. S. Kim, S.V. Kosonocky, and P. A. Sandon, "A Method and Apparatus for Controlling Power Consumption in An Integrated Circuit," Pub. No. US 2006/0064606 A1, March 23, 2006.
20. S. Kim and S. V. Kosonocky, "An Integrated Circuit having Parallel Execution Units with Differing Execution Latencies," Pub. No. US 2004/0225868 A1, November 11, 2004.

GRADUATED STUDENTS:

Ph.D. Theses Supervised

1. Hyunjoon Lee, *A Study on Interface Circuits for CMOS-Integrable Bio-Chemical Sensors*, August 2012 (Postdoctoral Research Fellow, Seoul National University).
2. Jong-Kwan Woo, *Holistic Design Exploration on Pipeline Analog-to-Digital Converter*, February 2011 (Postdoctoral Research Fellow, University of Michigan, Ann Arbor).
3. Dong Yong Shin, *Reducing Image Sticking in AMOLED Displays with Time-Ratio Grayscale by Analog Calibration*, February 2011 (Samsung Mobile Display).

M.S. Theses Supervised

1. Rahul Singh, Circuit Techniques for Noise Robustness in Deep Submicron Digital Design,

August 2011 (Samsung Electronics).
2. Sungwon Yim, Verilog-AMS Modeling of Flyback PFC Converter, August 2011 (pursuing a Ph.D. degree, Seoul National University).
3. Sanghoon Lee, Low-Voltage Bandgap Reference Circuit with Output-Regulated Current Mirror in a Deep-Submicron Technology, February 2011 (GCT Semiconductor)
4. Gi-Moon Hong, *A High Speed Phase Rotator using Simple Resistive Interpolation*, February 2011 (pursuing a Ph.D. degree, Seoul National University).
5. Seung-In Na, Low Noise Amplifier for Neural Recording System, February 2011 (pursuing a Ph.D. degree, Seoul National University).
6. Nan Xing, *A High-Resolution Wide Input-Range Cyclic Time-to-Digital Converter Using Fractional Difference Conversion Method*, August 2010 (Samsung Electronics).
7. Hyongmin Lee, *A High Resolution Time-to-Digital Converter Using Open-loop Delay-Locked Loop*, February 2010 (Ph.D. program in my research group).
8. Sungho Ahn, *A Comparator based Switched Capacitor Cyclic Analog-to-Digital Converter*, February 2010 (Hynix Semiconductor).
9. Manho, *A High Resolution Capacitance Deviation-to-Digital Converter Utilizing Dual-Slope Time-Stretcher*, February 2010 (Samsung Electronics).
10. Joowon Park, *Modeling and design of the ΔΣ ADC circuit suitable for large-scale CNT sensor array*, February 2009 (SK Telecom).
11. Hyongwook Lee, *Study on peak current minimization during active mode transition of power gating circuirs*, August 2008 (Samsung Electroncis).
12. Heebum Lee, *Wideband Multi-bit Continuous-Time ∑△ Modulator with Adaptive Quantization Level*, February 2008 (Hynix Semiconductor).
13. Han Yang, *Low Power Pipelined ADC with Partially Opamp-Sharing and Partially Opamp-Switching*, February 2008 (Samsung Electronics).
14. Changjun Choi, *A Power Gating Structure to Stabilize Data-Retention Voltage in Deep-submicron CMOS Technology*, August 2007 (Samsung Electronics).
15. Hyunjoon Lee, *Design of the CMOS Charge Amplifier Circuit for the Detection of MEMS Cantilever Signal*, February 2007 (Postdoctoral Research Fellow, Seoul National University).

INTERNATIONAL PUBLICATIONS:

~~*Accumulated Citations=447 (Google Scholar, September 2010)*~~
Accumulated Citations=812 (Google Scholar, September 2012)

Journals

1. S. Kim, J.-K. Woo, W.-Y. Shin, G.-M. Hong, H. Lee, H. Lee, and S. Kim, "A 10Mbps, 0.8pJ/bit, Referenceless Clock and Data Recovery Circuit for Optically Controlled Neural Interface System," accepted for publication in IEEE Transactions on Circuits and Systems-II.
2. W.-Y. Shin, G.-M. Hong, H. Lee, J.-D. Han, K.-S. Park, D.-H. Lim, S. Kim, D. Shim, J.-H. Chun,D.-K. Jeong, and S. Kim, "A 4-Slot, 8-Drop Impedance-Matched Bidirectional Multi-Drop DQ Bus with a 4.8-Gb/s Memory Controller Transceiver," accepted for publication in IEEE Transactions on Components, Packaging and Manufacturing Technology.
3. R. Singh, G.-M. Hong, and S. Kim, "Bitline Techniques with Dual Dynamic Nodes for Low-Power Register Files," accepted for publication in IEEE Transactions on Circuits and Systems-I.
4. H. Kim, S. Kim, and Y. Hong, “Frequency Dependency of Multi-Layer OLED Current Density-Voltage Shift and Its Application to Digitally-Driven AMOLED,” Journal of the Optical Society

of Korea (JOSK), vol. 16, issue 2, pp. 181-184 (2012).

5. R. Singh, G. M. Hong, M. Kim, J. Park, W.-Y. Shin, and S. Kim, "Static-switching pulse domino: A switching-aware design technique for wide fan-in dynamic multiplexers," Integration, the VLSI Journal, vol. 45, no. 3, pp. 253-262, June 2012 **[Special Issue of GLSVLSI 2011: Current Trends on VLSI and Ultra Low-Power Design]**.
6. G. M. Hong, W.-Y. Shin, D. Shin, J.-H. Park, M.-O. Kim, and S. Kim, "'High-Speed Phase Rotator using Resistive Interpolation for a 3.75-6.9Gb/s Serial-Link Receiver," IEE Electronics Letters, vol.48, no.8, pp.429-430, April 2012.
7. R. Singh, J.-K. Woo, H. Lee, S. Y. Kim, and S. Kim, "Power-Gating Noise Minimization by Three-Step Wake-up Partition," IEEE Transactions on Circuits and Systems-I, vol. 59, no. 4, pp.749-762, April 2012.
8. H. Lee, S. Lee, Y. J. Park, D. Perello, D.-H. Kim, S.-H. Hong, M. Yun, and S. Kim, "Integrating metal-oxide-decorated CNT networks with a CMOS readout in a gas sensor," Sensors, 2012, 12(3), 2582-2597.
9. S. Kim, H. Lee, H. Lee, J.-K. Woo, J. Cheon, H. Y. Kim, Y. J. Park and S. Kim, "Optical Failure Analysis Technique in Deep Submicron CMOS Integrated Circuits," Journal of Semiconductor Technology and Science, vol. 11, no. 4, December 2011.
10. D.-Y. Shin, H. Lee, and S. Kim, "Improving the Accuracy of Capacitance-to-Frequency Converter by Accumulating Residual Charges," IEEE Transactions on Instrumentation and Measurement, vol. 60, no. 12, December 2011.
11. M. Kim, H. Lee, J.-K. Woo, N. Xing, M.-O. Kim, and S. Kim, "A Low-Cost and Low-Power Time-to-Digital Converter Using Triple-Slope Time-Stretching," IEEE Transactions on Circuit and System-II, vol. 58, no. 3, pp. 169-173, March 2011.
12. D.-Y. Shin, H. Lee, and S. Kim, "A Delta-Sigma Interface Circuit for Capacitive Sensors with an Automatically Calibrated Zero Point," IEEE Transactions on Circuit and System-II, vol. 58, no. 2, pp. 90-94, February 2011.
13. H. Song, D.-S. Kim, D.-H. Oh, S. Kim, and D.-K. Jeong, "A 1.0-4.0Gb/s All-Digital CDR with 1.0-ps Resolution DCO and Adaptive Proportional Gain Control," IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp.424-434, February 2011.
14. N. Xing, J.-K. Woo, W.-Y. Shin, H. Lee, and S. Kim, "A 14.6 ps Resolution, 50 ns Input-Range Cyclic Time-to-Digital Converter using Fractional Difference Conversion Method," IEEE Transactions on Circuits and Systems-I, vol. 57, no. 12, pp.3064-3072, December 2010.
15. D.-S. Kim, H. Song, T. Kim, S. Kim, and D.-K. Jeong, "A 0.3–1.4 GHz All-Digital Fractional-N PLL with Adaptive Loop Gain Controller," IEEE Journal of Solid-State Circuits, vol. 45, no. 11, pp.2300-2311, November 2010.
16. H. Lee, J.-K. Woo, and S. Kim, "Charge Amplifier with Enhanced Frequency Response for SPM-Based Data Storage," IEEE Transactions on Circuits and Systems-II, vol. 57, no. 9, pp. 691-695, September 2010.
17. W.-Y. Shin, M. Kim, G.-M. Hong, and S. Kim, "A Fast-Acquisition PLL using Split Half-Duty Sampled Feedback Loop Filter," IEEE Transactions on Consumer Electronics,vol. 56, no. 3, August 2010.
18. S. Lee, H. Lee, J.-K. Woo, and S. Kim, "A Low-Voltage Bandgap Reference with Output-Regulated Current Mirror in 90nm CMOS," IEE Electronics Letters, vol.46, no.14, pp.976-977, July 2010.
19. H. Lee, J.-K. Woo, and S. Kim, "A CMOS Differential-Capacitance-to-Frequency Converter Utilizing Repetitive Charge Integration and Charge Conservation," IEE Electronics Letters, vol.46, no.8, pp.567-569, April 2010.
20. N. Xing, W.-Y. Shin, D.-K. Jeong, and S. Kim, "A High-Resolution Time-to-Digital Converter utilizing Fractional Difference Conversion Scheme," IEE Electronics Letters, vol.46, no.6,

pp.398-400, March 2010.
21. D.-Y. Shin, J.-K. Woo, Y. Hong, and S. Kim, “Quantitative evaluation of image sticking on displays with different gradual luminous variation,” Journal of SID, Journal of SID, vol. 18, no 3, pp.228-234, March 2010.
22. B. Y. Lee, S. M. Seo, D. J. Lee, M. Lee, J. Lee, J.-H. Cheon, E. Cho, H. Lee, I.-Y. Chung, Y. J. Park, S. Kim, and S. Hong, “Biosensor System-on-a-chip including CMOS-based Signal Processors and 64 Carbon Nanotube-based Sensors for the Detection of a Neurotransmitter,” Lab on a Chip, vol. 10, pp. 894-898, March 2010.
23. D.-Y. Shin, J.-K. Woo, Y. Hong, and S. Kim, “Reducing image sticking in AMOLED displays with time-ratio grayscale by analog calibration,” Journal of SID, vol. 17, no 9, pp.705-713, September 2009.
24. H.-W. Lee, H. Lee, J.-K. Woo, W.-Y. Shin and S. Kim, “A Low-Power Register File with Dual-Vt Dynamic Bit-Lines driven by CMOS Bootstrapped Circuit,” Journal of Semiconductor Technology and Science, vol. 9, no. 3, pp.148-152, Sept. 2009.
25. J.-K. Woo, D.-Y. Shin, D.-K. Jeong, and S. Kim, “High-Speed 10-bit LCD Column Driver with a Split DAC and a Class-AB Output Buffer,” IEEE Transactions on Consumer Electronics, vol. 55, no. 3, pp.1431-1438, August 2009.
26. H. Song, S. Kim, and D.-K. Jeong, “A Reduced-Swing Voltage-Mode Driver for Low-Power Multi-Gb/s Transmitters,” Journal of Semiconductor Technology and Science, vol. 9, no. 2, pp.104-109, June 2009.
27. Y.-D. Kim, H.-S. Ahn, S. Kim, and D.-K. Jeong, “A High-Speed Range-Matching TCAM for Storage-Efficient Packet Classification,” IEEE Transactions on Circuits and Systems-I, vol. 56, no. 6, pp.1221-1230, June 2009.
28. J.-H. Lee, S. Kim, and D.-K. Jeong, “A Combined Clock and Data Recovery Circuit with Adaptive Cancellation of Data-Dependent Jitter,” Journal of Semiconductor Technology and Science, vol. 8, no. 3, pp.193-199, September 2008.
29. H.-W. Lee, H. Lee, J.-K. Woo, W.-Y. Shin, and S. Kim, “Power-Gating Structure with Virtual Power-Rail Monitoring Mechanism,” Journal of Semiconductor Technology and Science, vol. 8, no. 2, pp.134-138, June. 2008.
30. S. Kim, C. Choi, D.-K. Jeong, S. V. Kosonocky, and S. Park, “Reducing Ground Bounce Noise and Stabilizing the Data Retention Voltage of Power Gating Structures,” IEEE Transactions on Electron Devices, vol. 55, no. 1, pp.197-205, Jan. 2008. [Special Issue on Device Technologies and Circuits Techniques for Power Management].
31. S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, and M. C. Papaefthymiou, “A Multi-Mode Power Gating Structure for Low-Voltage Deep-Submicron CMOS ICs,” IEEE Transactions on Circuits and Systems-II, vol. 54, no. 7, pp. 586-590, July 2007.
32. H. Jeong, B.-J. Yoo, C. Han, S.-Y. Lee, K.-Y. Lee, S. Kim, D.-K. Jeong, and W. Kim, “A 0.25μm CMOS 1.9-GHz PHS RF Transceiver with a 150-kHz Low-IF Architecture,” IEEE Journal of Solid-State Circuits, vol.42, no.6, pp.1318-1327, June 2007.
33. J.-K. Woo, D.-K. Jeong, and S. Kim, “A Fast-Locking CDR Circuit with Autonomously Reconfigurable Mechanism,” IEE Electronics Letters, vol.43, no.11, pp.624-626, May 2007.
34. V. Visvesh, M. C. Papaefthymiou, S. V. Kosonocky, and S. Kim, “On-Chip Synchronous Communication between Clock Domains with Quotient Frequencies,” IEE Electronics Letters, vol. 43, no. 9, pp.497-499, April 2007.
35. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, “Charge-Recovery Computing in Silicon,” IEEE Transactions on Computers, vol. 54, no. 6, pp.651-659, June 2005. **[Special Section on Energy Efficent Computing]**.
36. J.-S. Ahn, D.-K. Jeong, and S. Kim, “Fast Three-Dimensional Programmable Two-Selector,” IEE Electronics Letters, vol. 40, no. 18, pp.1098-1099, September 2004.

37. S. Hong, S.-S. Chin, S. Kim, and W. Hwang, “Power Reduction Technique in Coefficient Multiplications through Multiplier Characterization,” Journal of VLSI Signal Processing, vol. 38, no. 2, pp.101-113, September 2004.
38. J.-O. Plouchart, N. Zamdmer, J. Kim, M. Sherony, Y. Tan, A. Ray, M. Talbi, L. F. Wagner, K. Wu, N. E. Lustig, S. Narasimha, P. O'Neil, N. Phan, M. Rohn, J. Strom, D. M. Friend, S. V. Kosonocky, D. R. Knebel, S. Kim, K. A. Jenkins, and M. M. Rivier, “Application of an SOI 0.12μm CMOS Technology to SoCs with Low-Power and High-Frequency Circuits,” IBM Journal of Research and Development, vol. 47, no. 5/6, pp.611-629, September/November 2003.
39. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, “Fine-Grain Real-Time Reconfigurable Pipelining,” IBM Journal of Research and Development, vol. 47, no. 5/6, pp.599-609, September/November 2003 **[Special Issue on Power-Efficient Computer Technologies]**.
40. S. Kim and C. H. Ziesler, “A Clockless Future of Systems on Chip,” Design & Test of Computers: Special Issue on Clockless VLSI Design, vol. 20, no. 6, November/December 2003.
41. S. Kim, C. H. Ziesler and M. C. Papaefthymiou, “A True Single-Phase Energy-Recovery Multiplier,” IEEE Transactions on Very Large Scale Integration Systems, vol. 11, no. 2, pp. 194-207, April 2003.
42. S. V. Kosonocky, A. J. Bhavnagarwala, K. Chin, G. D. Gristede, A.-M. Haen, W. Hwang, M. B. Ketchen, S. Kim, D. R. Knebel, K. W. Warren, and V. Zyuban, “Low-Power Circuits and Technology for Wireless Digital Systems,” IBM Journal of Research and Development, vol. 47, no. 2/3, pp.283-298, March/May 2003 **[Special Issue on Communication Technologies]**.
43. S. Hong, S. Kim, and W. E. Stark, “Low-Power Application-Specific Parallel Array Multiplier Design for DSP applications,” VLSI Design: An International Journal of Custom-Chip Design, Simulation, and Testing, vol. 14, no. 3, pp.287-298, October 2002.
44. S. Kim and M. C. Papaefthymiou, “True Single-Phase Adiabatic Circuitry,” IEEE Transactions on Very Large Scaling Integration Systems, vol. 9, no. 1, pp.52-63, February 2001.
45. S. Kim, S.-W. Kim and T. Rhee, “An Extended Fuzzy Clustering Algorithm and Its Application,” Journal of Circuits, Systems, and Computers, vol. 5, no. 2, pp.239-259, April 1995.

Conferences

46. H. Lee, J.-K. Woo, S. Kim, and M. Kim, “Dififerential Capacitance-to-Digital Converter Utilizing Time-Domain Manipulation of Intermediate Signals,” In Proceedings of the 54nd Midwest Symposium on Circuits and Systems, pp. 1 – 4, August 2011.
47. S. Kim, J.-K. Woo, W.-Y. Shin, G. Hong, H. Lee, H. Lee, S. Kim, “A Low-Power Referenceless Clock and Data Recovery Circuit with Clock-Edge Modulation for Biomedical Sensor Applications,” In Proceedings of International Symposium on Low Power Electronics and Design, pp. 347 – 350, August 2011 **[Best Paper Award, ISLPED'11**] .
48. J.-K. Woo, S. Kim, H. Lee, and S. Kim, “A Comparator-Based Cyclic Analog-to-Digital Converter with Boosted Preset Voltage,” In Proceedings of International Symposium on Low Power Electronics and Design, pp. 199 – 204, August 2011.
49. H. Lee, H. Lee, J.-K. Woo, S. Kim, and S. Kim, “A CMOS Readout Integrated Circuit with Wide Dynamic Range for a CNT Bio-Sensor,” In Proceedings of International Symposium on Low Power Electronics and Design, pp. 357 – 360, August 2011.
50. R. Singh, J.-C. Son, U. Cho, G. Jung, M.-S. Kim, H. Lee, and S. Kim, “A Static-Switching Pulse Domino Technique for Statistical Power Reduction of Wide Fan-in Dynamic Gates,” In Proceedings of the Great Lake Symposium on VLSI, pp. 127-132, May 2011.
51. W.-Y. Shin, G.-M. Hong, H. Lee, J.-D. Han, K.-S. Park, D.-H. Lim, S. Kim, J.-H. Chun, D.-K. Jeong, S. Kim, “A 4.8Gb/s Impedance-Matched Bi-Directional Multi-Drop Transceiver for High Capacity Memory Interface,” to be published in Proceedings of the IEEE International Solid-

State Circuits Conference, February 20-24 2011.

52. J. C. Kao, W.-H. Ma, S. Kim, and M. Papaefthymiou, "2.07 GHz Floating-Point Unit with Fine-Grain Resonant-Clock Logic," to be published in Proceedings of the IEEE Asian Solid-State Conference, November 8-10 2010.
53. J.-D. Han, W.-Y. Shin, W.-S. Choi, J.-H. Chun, S. Kim, and D.-K. Jeong, "A 5-Gb/s Digitally Controlled 3-Tap DFE Receiver for Serial Communications," to be published in Proceedings of the IEEE Asian Solid-State Conference, November 8-10 2010.
54. R. Singh, A.-R. Kim, and S. Kim, "Footer Voltage Feedforward Domino Technique for Wide Fan-In Dynamic Logic," In Proceedings of the IEEE International SoC Conference, pp. 224-229, September 27-29 2010.
55. J.-K. Woo, H. Lee, S. Ahn, and S. Kim, "A High Resolution Fast-Conversion Readout Circuit for Differential Capacitive Sensors," In Proceedings of the IEEE International SoC Conference, pp. 44-47, September 27-29 2010.
56. R. Singh, A.-R. Kim, and S. Kim, "A Three-Step Power-Gating Turn-on Technique for Controlling Ground Bounce Noise," In Proceedings of the 2010 International Symposium on Low Power Electronics and Design, pp. 171-176, August 18-20 2010.
57. B. Lee, S. Seo, M. Sung, D. Lee, M. Lee, J. Lee, J. Cheon, E. Cho, H. Lee, I. Chung, Y. Park, S. Kim and S. Hong, "Integration of Uniform Arrays of Carbon Nanotube-Based Biosensors and CMOS Signal-Processing Circuits into a System-on-a-Chip," 217th Electrochemical Society (ECS) Meeting, April 25-30, 2010.
58. B. Y. Lee, et. al. "Scaling Behavior of Carbon Nanotube-based Biosensors Integrated on CMOS Signal-processing Circuits," APS March Meeting 2010.
59. D.-S. Kim, H. Song, T. Kim, S. Kim, and D.-K. Jeong, "A 1.35GHz All-Digital Fractional-N PLL with Adaptive Loop Gain Controller and Fractional Divider," In Proceedings of the IEEE Asian Solid-State Conference, pp. 161-164, November 16-18 2009.
60. M. Kim, N. Xing, D.-Y. Shin, H. Lee, and S. Kim, "A High Resolution Capacitance Deviation-to-Digital Converter utilizing Time Stretching," In Proceedings of the IEEE International SoC Conference, pp. 83-86, September 2009.
61. N. Xing, H. Song, D.-K. Jeong, and S. Kim, "A PVT-Insensitive Time-to-Digital Converter using Fractional Difference Vernier Delay Lines," In Proceedings of the IEEE International SoC Conference, pp. 43-46, September 2009.
62. D.-Y. Shin, J.-K. Woo, Y. Hong, S. Kim, "Quantification of Image Sticking for Images with Different Long-Range Non-Uniformity," In Proceedings of the 2009 International Symposium, Seminar, and Exhibition, pp.1386-1388, June 2009.
63. J.-K. Woo, D.-Y. Shin, W.-J. Choe, D.-K. Jeong, S. Kim, "A 10-Bit Column Driver with Split-DAC Architecture," In Proceedings of the 2008 SID International Symposium, Seminar, and Exhibition, pp. 892-895, May 2008.
64. D.-Y. Shin, J.-K. Woo, Y. Hong, S. Kim, "A New Hybrid Analog-Digital Driving Method to Improve AMOLED Lifetime," In Proceedings of the 2008 SID International Symposium, Seminar, and Exhibition, pp. 1196-1199, May 2008.
65. J.-K. Kim, J. Kim, S.-Y. Lee, S. Kim, and D.-K. Jeong, "A 26.5-37.5 GHz Frequency Divider and a 73-GHz-BW CML Buffer in 0.13 μm CMOS," In Proceedings of the IEEE Asian Solid-State Circuits Conference, pp. 148-151, November 2007.
66. M.-S. Hwang, S.-Y. Lee, J.-K. Kim, S. Kim, and D.-K. Jeong, "A 180-Mb/s to 3.2-Gb/s, Continuous-Rate, Fast-Locking CDR without Using External Reference Clock," In Proceedings of the IEEE Asian Solid-State Circuits Conference, pp. 144-147, November 2007.
67. H. Kim, S. Kim, S. W. Chang, D. Lee, D. S. Jeong, H. K. Chung, and Y. Hong, "Frequency Dependence of OLED Voltage Shift Degradation," In Proceedings of the International Meeting on Information Display, pp. 1108-1111, August 2007.

68. D.-H. Oh, D.-S. Kim, S. Kim, D.-K. Jeong, W. Kim, "A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO," In Proceedings of the IEEE International Solid-State Circuits Conference, pp.222-223, February 2007.
69. J.-K. Woo, H. Lee, W.-Y. Shin, H. Song, D.-K. Jeong and S. Kim, "A Fast-Locking CDR circuit with an Autonomously Reconfigurable Charge Pump and Loop Filter," In Proceedings of the IEEE Asian Solid-State Circuits Conference, pp. 411-414, November 2006
70. Y.-D. Kim, H.-S. Ahn, J.-Y. Park, S. Kim, and D.-K. Jeong, "A Storage- and Power-Efficient Range-Matching TCAM for Packet Classification," In Proceedings of the IEEE International Solid-State Circuits Conference, pp.21-23, February 2006.
71. V. S. Sathe, J.-Y. Chueh, J. Kim, C. H. Ziesler, S. Kim, and M. C. Papaefthymiou, "Fast Efficient, Recovering, and Irreversible," In Proceedings of the ACM International Conference on Computing Frontiers, pp. 407-413, May 2005.
72. V. S. Sathe, C. H. Ziesler, M. C. Papaefthymiou, S. Kim, and S. V. Kosonocky, "A Synchronous Interface for SoCs with Multiple Voltage and Clock Domains," In Proceedings of the IEEE International SOC Conference, September 2004.
73. S. Kim, S. V. Kosonocky, D. R. Knebel, and K. Stawiasz, "Experimental measurement of a novel power gating structure with intermediate power saving mode," In Proceedings of the 2004 International Symposium on Low Power Electronics and Design, pp. 20-25, August 2004.
74. S.-S. Chin, S. Hong, and S. Kim, "Usage of Application-Specific Switching Activity for Energy Minimization of Arithmetic Units," In Proceedings of the IEEE Computer Annual Symposium on VLSI, February, 2004.
75. C. H. Ziesler, J. Kim, M. C. Papaefthymiou, and S Kim, "Energy Recovery Design for Low-Power ASICs," In Proceedings of IEEE International SOC Conference, pp. 424-427, September 2003.
76. S. Kim, S. V. Kosonocky, D. R. Knebel, K. Stawiasz, D. Heidel, and M. Immediato, "Minimizing Inductive Noise in System-On-a-Chip with Multiple Power Gating Structures," In Proceedings of the 29th European Solid-State Circuits Conference, pp. 635-638, September 2003.
77. S. Kim, S. V. Kosonocky, and D. R. Knebel, "Understanding and Minimizing Ground Bounce In Mode Transition of Power Gating Structures," In Proceedings of the 2003 International Symposium on Low Power Electronics and Design, pp. 22-25, August 2003.
78. S. Hong, S.-S. Chin, S. Kim, and W. Hwang, "Multiplier Architecture Power Consumption Characterization for Low-Power DSP Applications," In Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems, pp.741-744, September 2002.
79. S. Kim, Y. Shin, S. V. Kosonocky and W. Hwang, "Long-Term Power Minimization of Dual-Vt CMOS circuits," In Proceedings of the 15th Annual 2002, IEEE International ASIC/SOC Conference, pp.323-327, September 2002.
80. S. Kim *et al.*, "A Resonant Clock Generator for Single-Phase Adiabatic Systems," In Proceedings of the 2001 International Symposium on Low Power Electronics and Design, pp. 159-164, August 2001.
81. S. Kim, C. H. Ziesler and M. C. Papaefthymiou, "A True Single-Phase 8-bit Adiabatic Multiplier," In Proceedings of the 38th Design Automation Conference, pp.758-763, June 2001. **[DAC Student Design Contest Award Winner (First Prize)]**
82. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, "Design, Verification, and Test of A True Single-Phase Adiabatic Multiplier, In Proceedings of the 2001 Conference on Advanced Research in VLSI, pp.42-58, March 2001.
83. S. Kim, C. H. Ziesler, and M. C. Papaefthymiou, "A Reconfigurable Pipelined IDCT for Low-Energy Video Processing," In Proceedings of the 13th Annual 2000 IEEE International ASIC/SOC Conference, pp. 13-17, September 2000.

84. S. Kim and M. C. Papaefthymiou, “Reconfigurable Low Energy Multiplier for Multimedia System Design,” In Proceedings of the 2000 IEEE Computer Society Annual Workshop on VLSI, pp.129-134, April 2000.
85. S. Kim and M. C. Papaefthymiou, “Low-Energy Adder Design with Single-Phase Source-Coupled Adiabatic Logic,” In Proceedings of the 1999 International Workshop on Power and Timing Modeling, Optimization and Simulation, pp.93-102, October 1999.
86. S. Hong, S. Kim, M. C. Papaefthymiou, and W. E. Stark, “Low-Power Parallel Multiplier Design for DSP applications through Coefficient Optimization,” In Proceedings of the 12th Annual 1999 IEEE International ASIC/SOC Conference, pp.286-290, September 1999.
87. S. Kim and M. C. Papaefthymiou, “Single-Phase Source-Coupled Adiabatic Logic,” In Proceedings of the 1999 International Symposium on Low Power Electronics and Design, pp.97-99, August 1999.
88. S. Kim *et al*., “Comprehensive Energy vs. Complexity Analysis of VLSI FFT Architecture for Low Energy Wireless Communication Applications,” In Proceedings of the 42nd Midwest Symposium on Circuits and Systems, pp.313-316, August 1999.
89. S. Kim and M. C. Papaefthymiou, “Pipelined DSP Design with True Single-Phase Energy-Recovering Logic Style,” In Proceedings of the IEEE Alessandro Volta Memorial Workshop on Low Power Design, pp.135-143, March 1999.
90. S. Kim and M. C. Papaefthymiou, “True Single-Phase Energy-Recovering Logic for Low-Power, High-Speed VLSI,” In Proceedings of the 1998 International Symposium on Low Power Electronics and Design, pp.167-172, August 1998.

Technical Reports

91. S. Kim *et al*., “Comparison of Active Well Bias to Supply Voltage Scaling for Leakage Control," In IBM Research Report: RC22759, 2003.
92. S. Kim, S. V. Kosonocky and D. R. Knebel, “Ground Bounce and Ground Bounce Reduction Techniques of Power Gate Structure,” In IBM Research Report: RC22694, 2003
93. S. Kim, Y.-S. Shin, S. V. Kosonocky and W. Hwang, “Design Methodology for Optimizing Dynamic and Standby Power in Dual-Vt CMOS circuit,” In IBM Research Report: RC22496, 2002.
94. S. Kim *et al*., “Programming-Based Mixed Custom/Semi-Custom Design Methodology for Low-Power, High-Performance VLSI,” In IBM Research Report: RC22342, 2002.

PH.D. COMMITTEE SERVED ON:

1. A Study on Interface Circuits for CMOS-Integrable Bio-Chemical Sensors, August 2012.
2. Design of Low-Power Digital-Readout Interface for Capacitve Microphones, August 2011.
3. The Low Power Design for an H.264/AVC Baseline Decoder Using Block Caches and Clock Gating, February 2011.
4. A Multidrop Bus Design Scheme with Resistor-Based Impedance Matching on Nonuniform Impedance Lines, February 2011.
5. A Low-Voltage Gain-Transition CDS Based Pipelined ADC, February 2011.
6. Reducing Image Sticking in AMOLED Displays with Time-Ratio Grayscale by Analog Calibration, February 2011.
7. Design of fully integrated CMOS 40-Gb/s serial link transceiver, August 2009.
8. High-accuracy clock synchronization system over packet switched networks, August 2009.
9. Study on the design of wide range CDR without a external reference clock, June 2009.
10. Study on design of all-digital phase-locked loop, August 2009.

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11. Storage- and power-efficient range-matching ternary content addressable memory for packet classification, June 2008.
12. Design of ethernet switch architecture for bandwidth provision of broadband access networks, February 2008.
13. Low-power design of a physical layer chip over unshielded twisted pair copper cable, February 2008.
14. Clock-edge modulated serial link technique for mobile displays, August 2007.
15. Cost-effective methods to provide quality of service in packet networks, August 2007.
16. A single chip triple-band CMOS RF Transceiver for W-CDMA, February 2007.
17. Efficient high-speed network storage architecture over ethernet for home networks, February 2006.
18. Circuit techniques for low phase noise and reduced spur in frequency synthesizers, February 2006.
19. Low-jitter design techniques of fractional-N frequency systhesizers using multi-phase clocks, February 2006.
20. Design of shared-memory architecture for single-chip gigabit ethernet switch of 100 Gbps aggregate bandwidth, February 2005.